RH850/U2A

Clock Supply

R01AN4593ED0140
Rev 1.40
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Introduction

This document describes the clock supply on the RH850/U2A microcontrollers.

It should be used in conjunction with the corresponding RH850/U2A series user's manual.

Target Device

This application note is intended to describe the clock supply on the RH850/U2A series.

In this document, the RH850/U2A-EVA device R7F702Z19AEDBG is employed to implement the example application. Still, the concept described in this document applies also to other members of the RH850/U2A series.

The RH850/U2A-EVA series has following variants:

RH850/U2A-EVA	FBGA-516	R7F702Z19AEDBG
		R7F702Z19BFDBG
RH850/U2A16	FBGA-516	R7F702300EBBG-C
		R7F702300AEBBG-C
	FBGA-373	R7F702300EBBB-C
		R7F702300AEBBB-C
	FBGA-292	R7F702300EABA-C
		R7F702300AFABA-C
RH850/U2A8	FBGA-373	R7F702301EBBA-C
		R7F702301AEBBA-C
	FBGA-292	R7F702301EABG-C
		R7F702301 AFABG-C
RH850/U2A6	FBGA-292	R7F702302FABB-C
	HLQFP-176	R7F702302FAFK-C
	FBGA-156	R7F702302FABD-C
	HLQFP-144	R7F702302FAFM-C

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1. Background

The clock control supervises the clock signals and ensures various start-ups and stabilization times.

The clock tree distributes the clock signals from generator to all the elements that need it, and provides a general overview of the clock generation and control system.

This document includes the related function blocks:

- Clock controller
- Stand-by controller
- Clock monitor
- Interrupt controller

2. Reference Documents

This chapter contains information about the device reference documentation.

2.1 User’s Manual

The Hardware User’s Manual provides information about the functional and electrical behavior of the device.

At the release time of this document the following manual version is available:

RH850/U2A User’s Manual (Rev.1.10): R01UH0864EJ0110

3. General Features

The clock controller of RH850/U2A microcontrollers has the following features.

- 5 On-chip clock oscillators:
  - Main oscillator (Main OSC)
  - High speed internal oscillator (HS IntOSC)
  - Low speed internal oscillator (LS IntOSC)
  - Phase Locked Loop (PLL)
  - High voltage internal oscillator (HV IntOSC)
- Fine management of clock supply to peripheral modules
- On-chip clock monitor that detects clock anomalies when the Main oscillator, High speed internal oscillator, Low speed internal oscillator or PLL are in use
- Clock output (FOUT)

3.1 Clock Sources

The clocks generated from clock oscillators and output to CPU, Bus, and peripherals are clock sources. Table 3-1 shows the list of clock sources, and the typical working frequencies of them:

Table 3-1 List of Clock Sources[*1]

Clock Name	Symbol	Clock frequency (MHz)	Clock Source
High voltage internal oscillator	CLK_HVIOSC	16	
Low speed internal oscillator	CLK_LSIOSC	0.24	
High speed internal oscillator	CLK_HSIOSC	200	
Main oscillator	CLK_MOSC	16, 20, 24, 40	
Internal OSC clock	CLK_IOSC	0.24	CLK_LSIOSC
		200	CLK_HSIOSC
PLL	CLK_PLL	800, 640, 480	CLK_MOSC
	CLK_PLLO	800, 640, 480 or 400, 320, 240[*2]	CLK_PLL
System clock	CLK_SYS	0.24, 200	CLK_IOSC
		800, 640, 480 or 400, 320, 240	CLK_PLLO

Notes: 1. For detailed information please refer to *Section 4*.
2. The output frequency of the PLL depends on the selection of clock divider.
Please notice that within this output frequency, the maximal applicable CPU / system clock is 400, 320 or 240 MHz.

3.2 Clocks and related Modules

Table 3-2 shows the general information of clocks and related modules.

Table 3-2 Clocks and related Modules

Clock Symbol	Max. Frequency (MHz)			Operation / Communication / Count	Register access / Bus
CLK_MOSC	40			DMON, RHSIF L1 (internal)	
CLK_HVIOSC	16			VMON	
CLK_CPU	400	320	240	INTC1, INTC2	
CLK_SBUS	200	160	80		System Bus
CLK_HBUS	100	80	80	INTIF, sDMAC, DTS, RHSIF L1, RHSIF L2	H-BUS, sDMAC, DTS, ENTB, RHSIF L1, RHSIF L2, FLXA, INTC2
CLK_UHSB	160	160	160	RSCFD RAM, PSI5S, GTM	
CLK_HSB	80	80	80	SFMA, MMCA, SCI3, FLXA, RSENT, PST5, PSI5S, CXPI, OSTM, TAUD, TAUJ0, TAUJ1, TSG3, TAPA, TPBA, ENCA, PIC, ECM, KCRC	SFMA, MMCA, MSPI, RLIN3, RSCFD, CXPI, OSTM, GTM, WDTB 0 to 3, SWDTA, KCRC, RSENT, PSI5, PSI5S
CLK_LSB	40	40	40	EINT, OTS, RHSIF L1 (internal), PWM-Diag	VMON, DMON, OTS, RTCA0, ADCJ1, WDTBA, RIIC, CLMA 0 to 9
CLK_LPS	10			LPS	
CLK_MSPI	80			MSPI	
CLK_RLIN3	80			RLIN3	
CLK_RCANOSC	40			RSCFD	
CLKA_WDT	0.24			WDTBA	
CLK_WDT	10			WDTB0 to 3, SWDTA	
CLKA_TAUJ	80			TAUJ2, TAUJ3	
CLKA_RTCA	2.5			RTCA	
CLKA_ADC	40			ADCJ2	ADCJ2
CLK_ADC	40			ADCJ0, ADCJ1	
CLK_ECMCNT	10			ECM (delay count)	

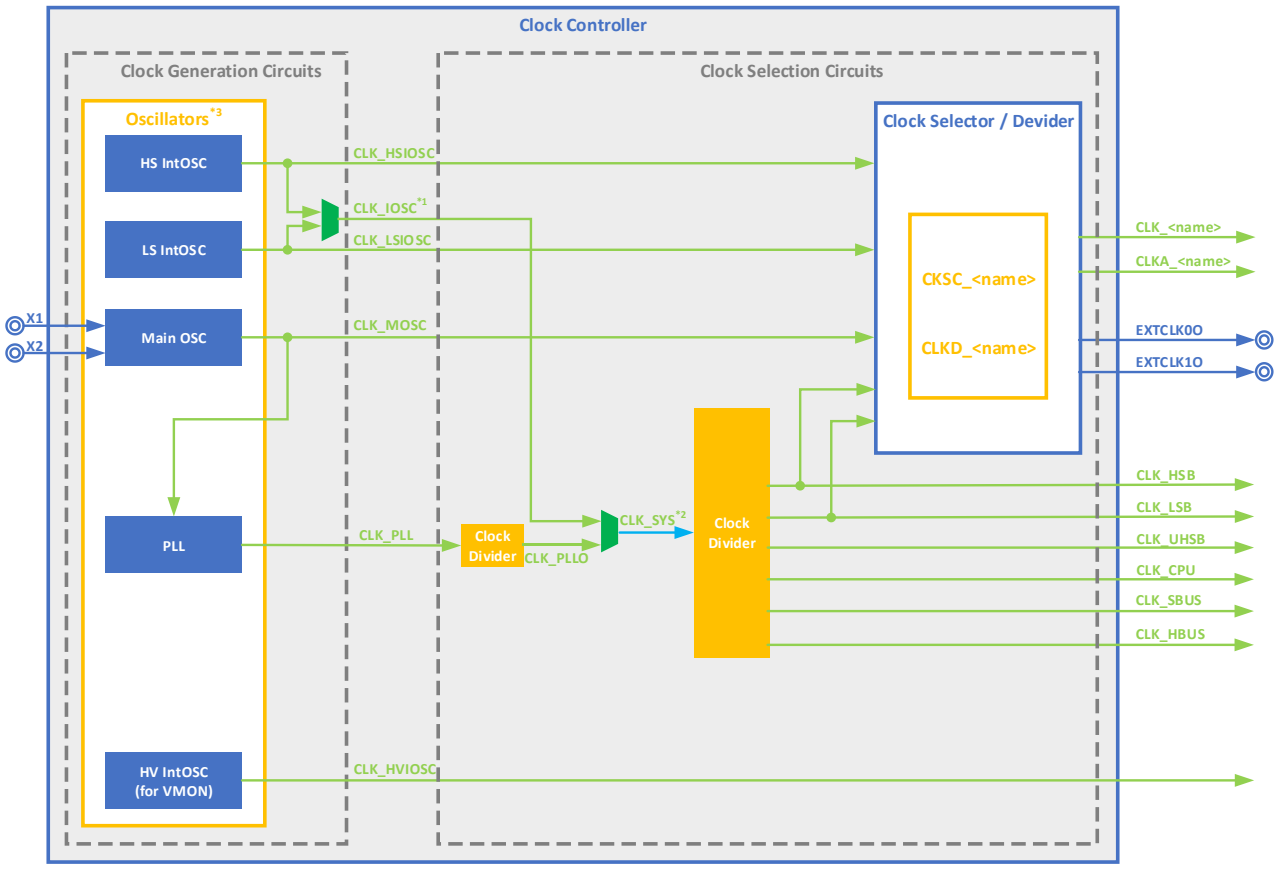
Note: The peripherals described in this table are related to different devices, please refer to HW User's Manual *R01UH0864EJxxxx Section 1.2 'Features'* for details.

4. Detailed Description

The clocks are generated from 5 oscillators, via a clock selector, the selected clocks are supplied to CPU system and peripherals.

The clock controller has 2 external quartz inputs for main oscillator. Meanwhile, selected clock sources can also be output via the 2 external outputs.

Figure 4-1 shows the block diagram of clock generation and general structure of the clock controller.



Notes: 1. Internal OSC clock (CLK_IOSC) is used as startup clock for System clock (CLK_SYS).
The clock source of CLK_IOSC is normally CLK_HSIOSC.
When the CLK_HSIOSC stops in chip standby mode, the clock source is switched to CLK_LSIOSC.

2. When the CLK_PLL is selected as CLK_SYS, the frequency can be configured by option byte and CLKD_PLLC register. For detailed information, please refer to *Section 4.1*.

3. For further information of oscillators, please refer to HW User's Manual *R01UH0864EJxxxx Section 13.4 'Clock Oscillators'*.

Figure 4-1 Block Diagram of Clock Controller

4.1 Clock Supply for CPU System

Referring to Table 3-2 and Figure 4-1, the system clock CLK_SYS is derived from PLL clock CLK_PLLO and CLK_IOSC.

The divided clock CLK_CPU provides the clock for CPU and RAM.

CLK_SBUS and CLK_HBUS provide the individual clock for system bus and AXI/AHB bus.

CLK_UHSB, CLK_HSB, CLK_LSB provide the clock for the peripherals without dedicated clock selectors.

The configuration of these clocks is described in *Section 5.2 'Configuration of CPU Clock'*.

4.2 Clocks for Peripherals

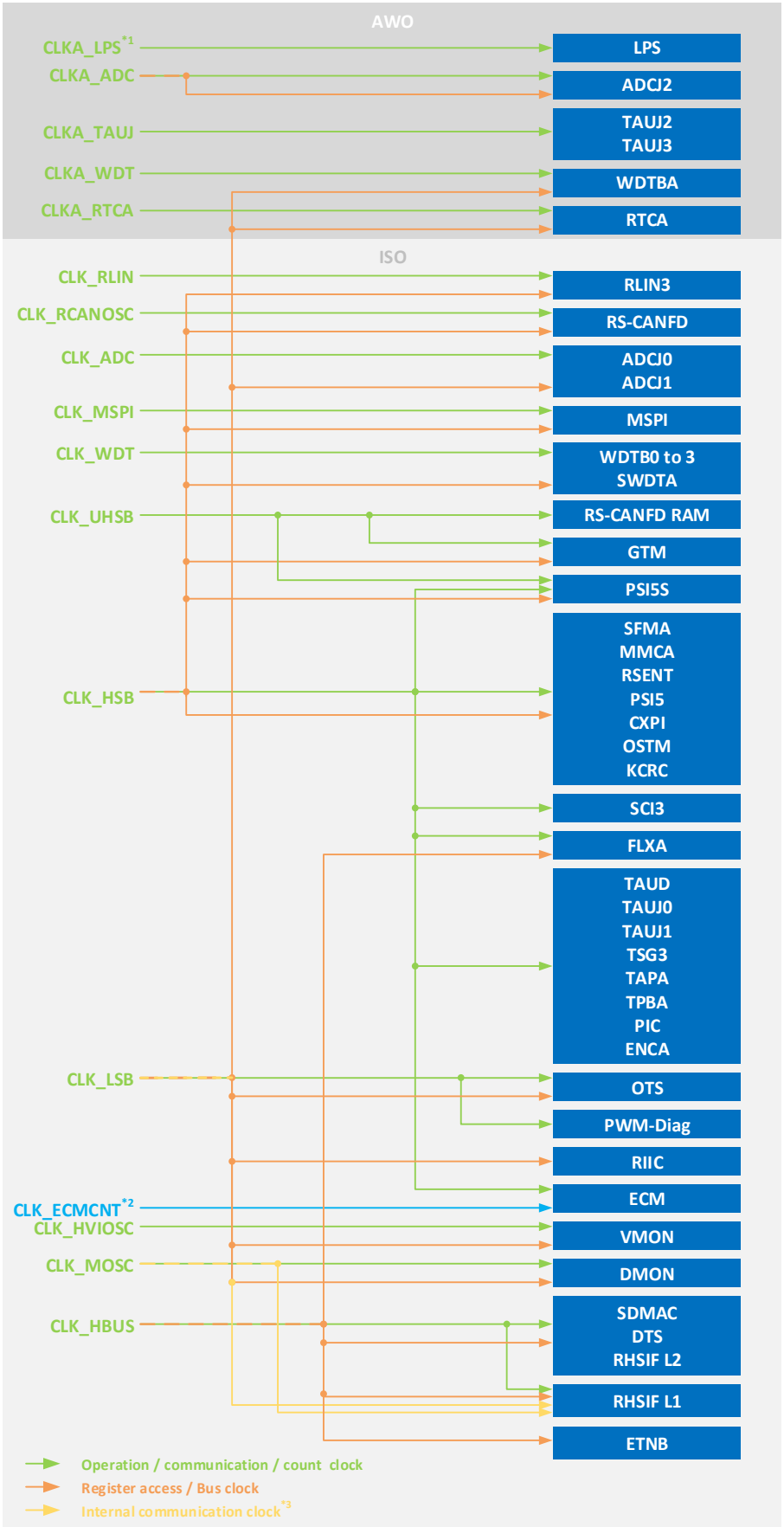
According to Figure 4-1, the clock sources or their divided clocks are connected to the clock selector control, in which the dedicated peripheral clocks are selected, divided and output as CLKA_<name> or CLK_<name> signals.

Meanwhile, other peripherals are supplied by CPU system clocks.

Figure 4-2 shows the clock supply of peripherals.

The clocks are supplied to peripherals as:

- Operation, communication or count clock;
- Register access or bus clock;
- Internal communication or delay clock.



Notes: 1. CLKA_LPS is identical to CLK_IOSC with the following exceptions.
The LPS operation clock CLKA_LPS is supplied by CLK_HSIOSC/20, if HS IntOSC is stable.

2. This clock is used for ECM delay timer and clear mask timer logics.
3. For detailed information, please refer to HW User's Manual *R01UH0864EJxxxx Section 29.5 'Datalink Layer (L1)'*.
4. The peripherals described in this diagram depend on the device configuration, please refer to HW User's Manual *R01UH0864EJxxxx* for further information.

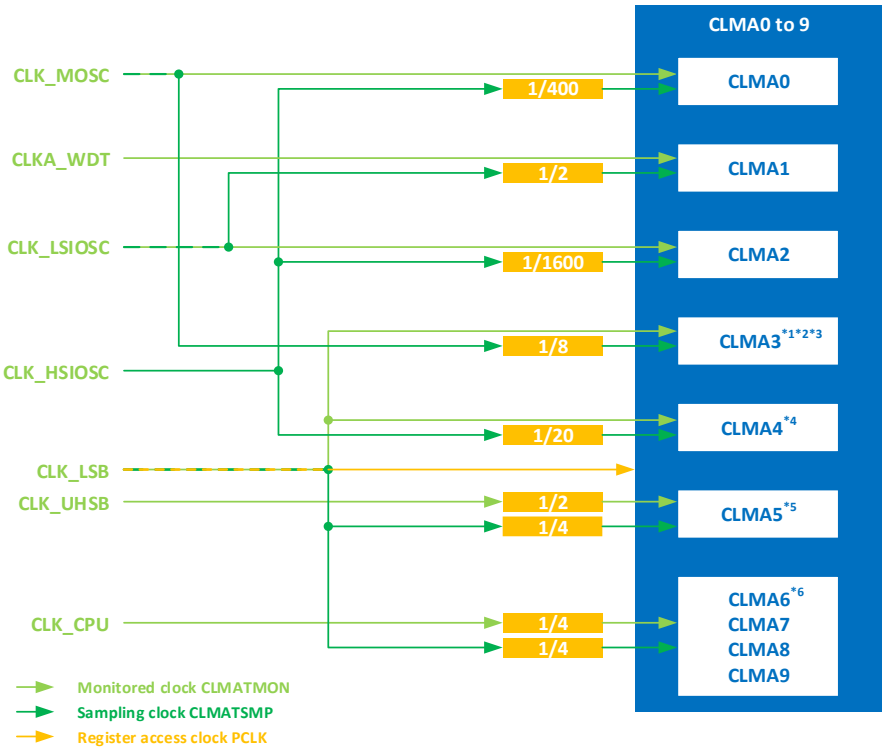
Figure 4-2 Clock Supply for Peripherals and Buses

4.3 Clocks for Clock Monitor

Clock monitor (CLMA) detects frequency abnormalities in the monitored clock, the clock supply to CLMA includes 3 types of clocks:

- Monitored clock CLMATMON
- Sampling clock CLMATSMP
- Register access clock PCLK

Figure 4-3 shows the mentioned clocks for CLMA.



Notes: 1. CLMA3 can be used when the source of CLK_SYS is CLK_PLLO.
2. CLMA3 needs to execute a special flow after reset release, please refer to HW User's Manual *R01UH0864EJxxxx Section 14.7.1 'Notes on CLMA3 after Reset Release'*.
3. When CLK_PLLO is selected as CLK_SYS, the PLL lock loss error status can be detected by CLMA3.
4. CLMA4 can be used when the source of CLK_SYS is CLK_IOSC.
5. CLMA5 monitors the GTM main clock.
6. CLMA6 monitors the CPU checker clock of PE0.
   CLMA7 monitors the CPU checker clock of PE1.
   CLMA8 monitors the CPU checker clock of PE2.
   CLMA9 monitors the CPU checker clock of PE3.

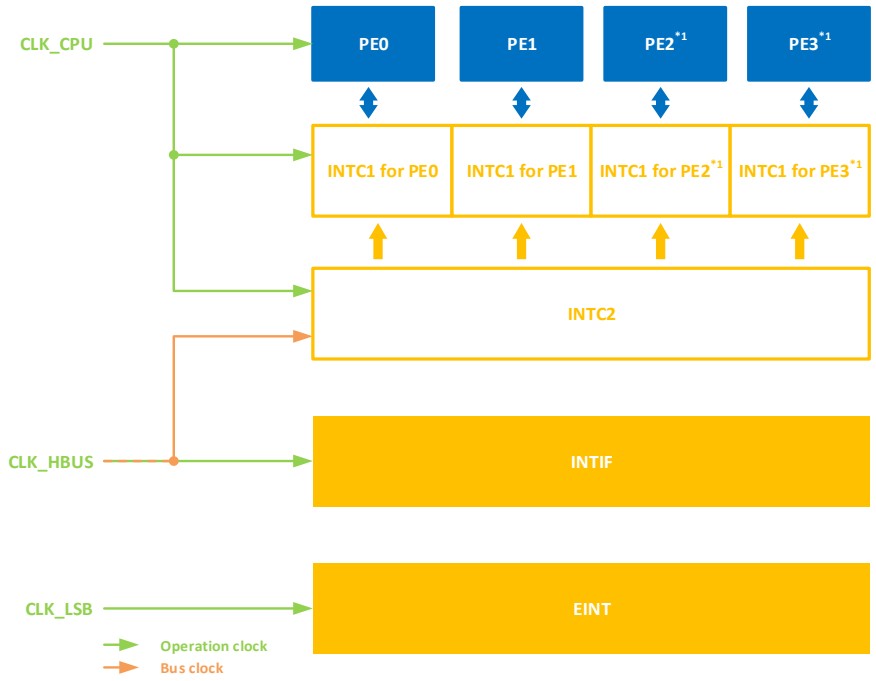
Figure 4-3 Clock Supply of Clock Monitor (CLMA)

4.4 Clocks for Interrupt Control and Handling

The RH850/U2A devices includes following interrupt units:

- INTC1, exclusive interrupt controller to each CPU
- INTC2, a common interrupt controller for all CPUs
- INTIF, peripheral interrupt / TPTM interrupt control function
- EINT, external interrupt / SW interrupt / NMI control function

The clock supply of the interrupt units is shown in Figure 4-4.



Notes: 1. This Figure includes some device dedicated modules, please refer to HW User's Manual for Details.

Figure 4-4 Clock Supply of Interrupt Controller

4.5 Clock Output

As is shown in Figure 4-1, the external outputs EXTCLK0O and EXTCLK1O are supplied to output selected clock sources as follows:

- CLK_MOSC
- CLK_HSB
- CLK_LSIOSC
- CLK_HSIOSC/20

A certain configuration of clock selector and Pin functions are required in this case, for detailed settings please refer to *Section 5.4 'Configuration for Clock Output'*.

5. Configuration

5.1 Configuration of Oscillators

Table 5-1 lists the registers which are used to configure the oscillators. Please notice that the clock registers are write protected, Register CLKKCPROT1 should be set before any other configuration.

Table 5-1 Register Setting of Oscillators

Register Name	Bit Name	Position	Description	Set Value
CLKKCPROT1	KCE	0	Enable key code of clock controller registers	1_B
MOSCE	MOSCDISTRG	1	Disable Main OSC	1_B
	MOSCENTRG	0	Enable Main OSC	1_B
MOSCSTPM*1	MOSCSTPMSK	0	Mask the stop request of Main OSC in standby mode	1_B
HSOSCSTPM*1	HSOSCSTPMSK	0	Mask the stop request of HS IntOSC in standby mode	1_B
PLLE	PLLDISTRG	1	Disable PLL	1_B
	PLLENTRG	0	Enable PLL	1_B
PLLSTPM*1	PLLSTPMSK	0	Mask the stop request of PLL in standby mode	1_B

Notes: 1. The stop mask registers determine the stop or continue operation of the oscillator in chip standby mode. This is described in *Section 6* '*Clock supply in Standby Mode'*.
2. To configure these registers, the key code protection register CLKKCPROT1 must be set to $A5A5A501_H$.

To select the frequency of main oscillator, the option byte MOSC_FREQ[2:0] should be set:

Table 5-2 Selection of Main OSC frequency using Option Byte

Option Byte	Bit Name	Position	Description	Set Value
OPBT10	MOSC_FREQ[2:0]	26 to 24	Select 16 MHz as Main OSC frequency	000_B
			Select 20 MHz as Main OSC frequency	001_B
			Select 24 MHz as Main OSC frequency	010_B
			Select 40 MHz as Main OSC frequency	011_B
			Setting prohibited	$1xx_B$

5.2 Configuration of CPU Clock

Table 5-3 shows the configuration and related operation frequency of the clocks for CPU system.

Table 5-3 Clock Setting of CPU System

Clock	CLK_IOSC (MHz)						CLK_PLLO (MHz)					
	CLK_LSIOSC			CLK_HSIOSC								
Settings	CKSC_CPUC.CPUCLKSCSID[*2]											
	1_B						0_B					
	Option Byte CKDIVMD[*1]											
	11_B	10_B	$0X_B$	11_B	10_B	$0X_B$	11_B		10_B		$0X_B$	
							CLKD_PLLC.PLLCLKDCSID[2:0][*2]					
							001_B	010_B	001_B	010_B	001_B	010_B
CLK_CPU	0.12	0.12	0.12	100	100	100	400	200	320	160	240	120
CLK_SBUS	0.06	0.06	0.04	50	50	33.3	200	100	160	80	80	40
CLK_HBUS	0.03	0.03	0.04	25	25	33.3	100	50	80	40	80	40
CLK_UHSB	0.048	0.06	0.08	40	50	66.7	160	80	160	80	160	80
CLK_HSB	0.024	0.03	0.04	20	25	33.3	80	40	80	40	80	40
CLK_LSB	0.012	0.015	0.02	10	12.5	16.7	40	20	40	20	40	20

Notes: 1. The CKDIVMD[1:0] bits are located in OPBT11, bit 31 to 30. For further information, please refer to HW User's Manual *Section 51.12 'Configuration Setting Area (Option Bytes, Reset Vector)'*.

2. To configure these register bits, the key code protection register CLKKCPROT1 must be set to $A5A5A501_H$.

5.3 Configuration of Peripheral Clocks

5.3.1 Configuration of Dedicated Peripheral Clocks

The clock for dedicated peripheral can be selected using clock selector control register CKSC_<name>C. The selected clocks are provided directly to the corresponding peripherals, or in some case via clock divider control CLKD_<name>C.

The actual clock setting can be read from status register CKSC_<name>S.

Table 5-4 lists the registers for the dedicated Peripherals.

Table 5-4 Clock Setting of Dedicated Peripherals

Clock Name	Register Name	Bit Name	Selection	Set Value
CLKA_WDT	CKSC_AWDTC	AWDTSCSID	CLK_LSIOSC	0_B
			CLK_LSIOSC/128*2	1_B
CLKA_TAUJ	CKSC_ATAUJC	ATAUJSCSID[1:0]	CLK_LSIOSC	00_B
			CLK_HSIOSC/20*2	01_B
			CLK_MOSC	10_B
			CLK_HSB	11_B
CLKA_RTCA	CKSC_ARTCAC	ARTCASCSID	CLK_MOSC/16	0_B
			CLK_LSIOSC*2	1_B
CLKA_ADC	CKSC_AADCC	AADCSCSID[1:0]	CLK_MOSC*4	00_B
			CLK_HSIOSC/20*2	01_B
			CLK_LSB	10_B
	CLKD_AADCC	AADCDCSID	Selection/1	1_B
			Selection/2	0_B
CLKA_LPS	-	-	CLK_LSIOSC or CLK_HSIOSC/20*1	-
CLK_WDT	CKSC_WDTC	WDTSCSID	CLK_HSIOSC/20	0_B
			CLK_HSIOSC/640*2	1_B
CLK_RLIN	CKSC_RLINC	RLINSCSID[1:0]	CLK_MOSC	00_B
			CLK_HSB*2	01_B
			CLK_MOSC/4	10_B
			CLK_MOSC/8	11_B
CLK_RCANOSC	CKSC_RCANC	RCANSCSID[1:0]	CLK_MOSC*2	01_B
			CLK_MOSC/2	10_B
			CLK_MOSC/4	11_B
CLK_ADC	CKSC_ADCC	ADCSCSID	CLK_LSB	0_B
			CLK_LSB/2*2	1_B
CLK_MSPI	CKSC_MSPIC	MSPISCSID	CLK_MOSC	0_B
			CLK_HSB*2	1_B
CLK_ECMCNT	-	-	CLK_HSIOSC/20	-

Notes: 1. When CLK_HSIOSC stops in chip standby mode, CLKA_LPS is CLK_LSIOSC. In other cases, CLKA_LPS is CLK_HSIOSC/20.

2. This clock configuration is the initial setting of the related register.
3. To configure these registers, the key code protection register CLKKCPROT1 must be set to A5A5A501H.
4. The CLK_MOSC can be selected only when its frequency is 16MHz, 20MHz, or 24MHz. For details, please refer to the HW User's Manual *R01UH0864EJxxxx* and the related Technical Notification *TN-RH8-B0410A/E*.

5.3.2 Configuration of the Clock Connection to Peripherals

To enable the clock connections to the peripherals, the bits MSR_ <name>.MS_<name>_n should be configured.

If the clock connection to a peripheral is disabled, the peripheral is set to module standby mode, in this case, register access is prohibited. Therefore, please always enable the clock connections before the peripheral configuration.

For detailed information, please refer to *Section 6.2 'Module Standby Mode'* in this document.

MSR registers do not cover the clock connection settings of LPS, PIC, ECM, DCRB and OTS.

5.4 Configuration for Clock Output

The 2 clock outputs are connected to the certain pins within alternative function. The clock signal which is expected to output, can be selected in clock selector register, then divided and output to the related pin.

Table 5-5 lists the configuration of clock selectors and dividers.

Table 5-6 shows the pin arrangement and the corresponding port alternative functions of clock output. The detailed information to configure the port alternative function is provided in Table 5-7.

Table 5-5 Clock Setting of Clock Output

Clock Name	Register Name	Bit Name	Selection	Set Value
EXTCLK0O	CKSC_FOUT0C	FOUT0SCSID[2:0]	CLK_MOSC	000_B, 110_B, 111_B
			CLK_HSB	001_B
			CLK_LSIOSC	011_B
			CLK_HSIOSC/20	100_B
	CLKD_FOUT0C	FOUT0DIV[9:0]*1	1/1 to 1/1023	001_H, $3FF_H$
EXTCLK1O	CKSC_FOUT1C	FOUT1SCSID[2:0]	CLK_MOSC	000_B, 110_B, 111_B
			CLK_HSB	001_B
			CLK_LSIOSC	011_B
			CLK_HSIOSC/20	100_B
	CLKD_FOUR1C	FOUT1DIV[9:0] *1	1/1 to 1/1023	001_H, $3FF_H$

Notes: 1. This register must not be written with a new value while the CLKD_FOUT0S.FOUT0SYNC is 0.
2. To configure these registers, the key code protection register CLKKCPROT1 must be set to $A5A5A501_H$.

Table 5-6 Pin Arrangement for Clock Output

Clock Output	Pin Name	Alternative function	Pin Location					
			144-Pin	156-Pin	176-Pin	292-Pin	373-Pin	512-Pin
EXTCLK0O	P2_8	Output Mode 3	-	-	149	B14	C15	G19
	P2_15	Output Mode 2	-	-	-	A11	A13	F16
	P4_10	Output Mode 2	64	P11	80	W15	AD16	AD20
	P4_12	Output Mode 2	-	N11	84	W16	AC16	AD21
	P10_7	Output Mode 3	10	F2	10	F2	M1	L7
EXTCLK1O	P4_8	Output Mode 3	61	-	75	W14	AD15	AD19
	P6_9	Output Mode 2	80	L13	103	N20	U24	V25
	P6_14	Output Mode 2	89	J13	112	L19	R23	T24
	P10_9	Output Mode 2	13	-	14	G2	N1	M7
	P10_14	Output Mode 4	21	G3	22	K1	R2	R6

Table 5-7 Configuration of Port Alternative Functions

Alternative-Function	Register					
	PMC	PIPC	PM	PFCAE	PFCE	PFC
Output Mode 1	1	0	0	0	0	0
Input Mode 1			1			
Output Mode 2			0		0	1
Input Mode 2			1			
Output Mode 3			0		1	0
Input Mode 3			1			
Output Mode 4			0		1	1
Input Mode 4			1			

Output Mode 5	0	1	0	0
Input Mode 5	1			
Output Mode 6	0		0	1
Input Mode 6	1			
Output Mode 7	0		1	0
Input Mode 7	1			
Output Mode 8	0		1	1
Input Mode 8	1			

6. Clock Supply in Standby Mode

6.1 Chip Standby Mode

In chip standby mode (STOP mode, DeepSTOP mode, and Cyclic STOP mode), the LS IntOSC continues operation. The Main OSC, HS IntOSC and PLL can be set to stop or continue using the <name>STPM registers. For the detailed configuration of <name>STPM register please refer to Table 5-1.

CLK_CPU, CLK_SBUS and CLK_HBUS are stopped in chip standby mode (STOP mode, DeepSTOP mode, and Cyclic STOP mode).

The clock operation in different chip standby modes are described in table 6-1.

Table 6-1 Clock Supply in Chip Standby Mode

Clock	Power Domain	Chip Standby Modes			
		STOP	**DeepSTOP**	**CyclicRUN**	**CyclicSTOP**
CLK_LSIOSC	AWO	Operable	Operable	Operable	Operable
CLK_HSIOSC		Stopped / Operable*1	Stopped / Operable*1	Operable	Stopped / Operable*1
CLK_MOSC					
CLK_HVIOSC		Operable	Stopped *3	Operable	Operable
CLK_PLLO	ISO	Stopped / Operable*2	Power off	Stopped	Stopped
CLK_CPU		Stopped		Operable	Stopped
CLK_SBUS					
CLK_HBUS					
CLK_UHSB		Operable			Operable
CLK_HSB					
CLK_LSB					

Notes: 1. The default value of <name>STPM.STPMSK bit is 0, the stop request of CLK_HSIOSC or CLK_MOSC is not masked in this case, the clocks stop operation in this chip standby mode.
If <name>STPM.STPMSK bit is set to 1, the stop request is masked, the clocks continue operation in this chip standby mode.
2. By default, CLK_PLLO stops in STOP or Cyclic STOP modes. PLL continues operation if PLLSTPM.STPMSK bit is set to 1.
3. The operation of CLK_HVIOSC in DeepSTOP mode depends on VMON DeepSTOP control register VMONDSCR.

For peripherals, the clock stop mask bits MSR_ <name>.STPMSK_<name> are used to determine the operation status of the clock in chip standby mode:

- If the stop mask bit is set to 0, the stop request is not masked, the related peripheral clock stops during chip standby mode.
  If the clock is in operation before entering standby mode, the clock restarts automatically after wake up of chip standby mode.
- If the stop mask bit is set to 1, the stop request is masked, the corresponding peripheral clock continues operate during chip standby mode.
  The clock supply of ISO area is stopped in DeepSTOP mode.

6.2 Module Standby Mode

Module standby mode stops the clocks for peripheral macros to reduce the power consumption in accordance with register settings.

The module which is in the module standby mode is not reset by releasing chip standby mode and the register access is prohibited.

The bit MSR_<name>.MS_<name>_n is used to stop or start all target clock domains:

- The default value of this bit is 1, in this case, all clocks connected to the corresponding peripheral are stopped, any configuration to the peripheral registers is invalid.
- If this bit is set to 0, the corresponding peripheral operates, the peripheral registers can be configured.
- This bit returns to the default value by module reset, for detailed information please refer to HW User's Manual *R01UH0864EJxxxx Section 9 'Reset Controller'*.

6.3 Module Standby Mode in Chip Standby Mode

According to *Section 6.1* and *6.2*, depending on the state of module standby register MSR_<name>, the clock supply state in each operation mode and chip standby mode is shown in Table 6-2.

Table 6-2 Module Standby Settings and Clock Supply of Peripherals in Chip Standby Mode

Register MSR_<name>		Operation Mode		Chip Standby Mode		
Bit MS_XXX	**Bit STPMSK_XXX**	**RUN**	**CyclicRUN**	**STOP**	**DeepSTOP**	**CyclicSTOP**
0	0	Operable	Operable	Stop	Stop	Stop
	1	Operable	Operable	Operable	Operable	Operable
1	0	Stop	Stop	Stop	Stop	Stop
	1	Stop	Stop	Stop	Stop	Stop

Note: To configure the MSR_<name> registers, the key code protection register MSRKCPROT must be set to $A5A5A501_H$.

For the operation propriety of each module clock, please refer to HW User's Manual *R01UH0864EJxxxx Section 15.1.2.3 Table 15.10.*

7. Sample Software

A sample SW is provided to show the basic clock configuration, clock output function and module standby settings.

The sample SW is based on RH850/U2A-EVA device R7F702Z19AEDBG, with PiggyBack board V1 RH850-U2A-516PIN-T1-V1.

The development tool of the SW package is GHS MULTI V800 version v7.1/2018.1.5 or later. For detailed information, please refer to Getting Started SW Package.

7.1 Clock Related Functions

The clock related functions in sample software are listed in Table 7.1.

Table 7-1 Clock-Related Functions in Sample SW

Function Name	Location in SW Package	Description
CLKINIT	U2A_GHS_CLK_TIMER\device\device.h	Clock initialization. This function provides an example of basic clock settings of U2A-EVA device.
initTAUJ	U2A_GHS_CLK_TIMER\src_mca\TIMER.c	TAUJ configuration. This function includes the module clock setting with MS bit.
initTAUD	U2A_GHS_CLK_TIMER\src_mca\TIMER.c	TAUD configuration. This function includes the module clock setting with MS bit.
initFOUT	U2A_GHS_CLK_TIMER\src_mca\TIMER.c	Configuration of clock output.

Please notice that part of the clock settings should be configured using option bytes, this part is not included in the sample SW. For Details please refer to HW User's Manual *R01UH0864EJxxxx Section 51.12.16 'OPBT10 — Option Byte 10'* and *Section 51.12.17 'OPBT11 — Option Byte 11'*.

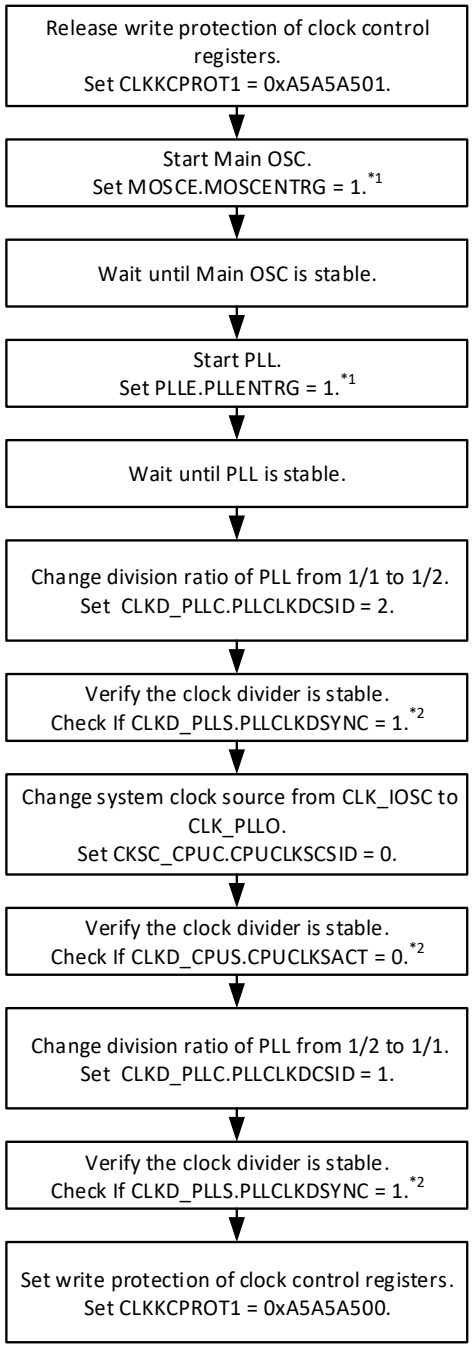
For further information to program the option byte, please refer to Getting Started SW Package.

7.2 Setting Procedure of Clocks in Sample SW

This section provides the diagram of the clock setting procedures.

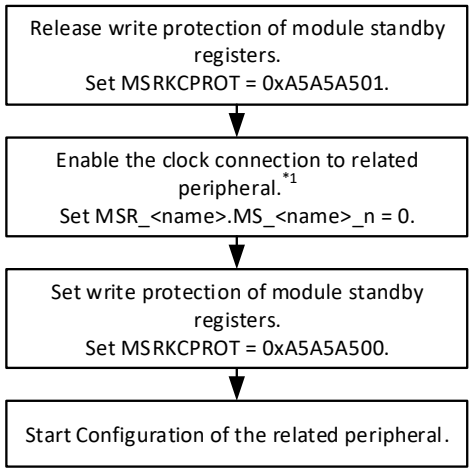
Figure 7-1 shows the system clock setting in sample software.

Figure 7-2 shows the general configuration of peripheral clock connection.



Notes: 1. These steps depend on the OPBT setting:
If OPBT11.STARTUPPLL = 1, the Main OSC and PLL should be manually enabled, these steps are necessary.
If OPBT11.STARTUPPLL = 0, the Main OSC and PLL start automatically after release of reset state.
2. Wait 100 µs after verifying.

Figure 7-1 Setting Procedure of System Clock in Sample SW



Note: 1. The clock connection must be enabled before configuration of the corresponding peripherals. Otherwise the peripheral registers cannot be accessed.

Figure 7-2 Setting Procedure of Peripherals in Sample SW

8. Summary

According to the sections described above, this document provides an overview and detailed information of configuration to the clock supplies of RH850/U2A devices.

Certain clock supplies are stopped in chip standby mode, peripheral clocks can be defined inoperable in module standby mode to conserve power.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
0.10	Jul 23, 2018		Internal release
1.00	Dec 15, 2018		release
1.10	Jan 25, 2019	23 to 25	Add sample SW to the document package and related descriptions (*Section 7 Sample SW*)
1.20	Nov 01, 2019	8	Update the Table 3-1, add table note
1.21	Dec 09,2019	1	Add the product information of RH850/U2A-EVA series
		1, 23	Update the device number regarding to HW UM
1.30	Nov 06, 2020	8	Update the description of general features regarding to HW UM.
		16	Replace all the information of MOSC_FREQ[1:0] to MOSC_FREQ[2:0]
		18	Add notes for Table 5-4
		20	Add notes for Table 5-5
1.40	Jun 13, 2022	1	Update the product line
		7	Update the reference document
		18	Add note 4 for Table 5-4
		20	Update the Table 5-6 Pin Arrangement for Clock Output
		24	Update the Table 7-1 Clock-Related Functions in Sample

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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