RH850/U2A

Clock Monitor

Introduction

This document describes the clock monitor on the RH850/U2A-EVA microcontrollers.

It should be used in conjunction with the corresponding RH850/U2A-EVA series user's manual.

Target Device

This application note is intended to describe the clock supply on the RH850/U2A-EVA series.

In this document the RH850/U2A16 device R7F702300BFABA-C is employed to implement this example application. Still, the concept described in this document applies also to other members of the RH850/U2A-EVA series.

The RH85/U2A-EVA series has the following variants:

RH850/U2A-EVA	FBGA-516	R7F702Z19AEDBG
		R7F702Z19BFDBG
RH850/U2A16	FBGA-516	R7F702300EBBG-C
		R7F702300AEBBC-C
		R7F702300BEBBC-C
	FBGA-373	R7F702300EBBB-C
		R7F702300AEBBB-C
		R7F702300BEBBB-C
	FBGA-292	R7F702300EABA-C
		R7F702300AFABA-C
		R7F702300BFABA-C
RH850/U2A8	FBGA-373	R7F702301EBBA-C
		R7F702301AEBBA-C
		R7F702301BEBBA-C
	FBGA-292	R7F702301EABG-C
		R7F702301AFABG-C
		R7F702301BFABG-C
RH850/U2A6	FBGA-292	R7F702302FABB-C
	HLQFP-176	R7F702302FAFK-C
	FBGA-156	R7F702302FABD-C
	HLQFP-144	R7F702302FAFM-C

Disclaimer

Table of Contents

1. Background

The RH850/U2A-EVA devices provide the clock monitor feature, which monitors the frequency of certain clocks. It takes the sampling clock as reference and detects when the monitored clock is out of the expected frequency range.

The information in this document applies to all clock monitors for the RH850/U2A-EVA devices, while the software sample focuses on CLMA0.

2. Reference Documents

This chapter contains information about the device reference documentation.

2.1 Hardware User's Manual

The Hardware User's Manual provides information on the functional and electrical behavior of the device.

At the release time of this document the following manual version is available:

- RH850/U2A-EVA Group User's Manual: Hardware (R01UH0864EJ0140, Rev.1.40)

It's recommended to use the corresponding document or other later versions.

2.2 User's Manual for RH850/U2A16 Starter Kit

The Starter Kit User's Manual provides information about the RH850/U2A16 Starter Kit and peripheral circuits.

At the release time of this document the following manual version is available.

- RH850/U2A16 Starter Kit User's Manual: Hardware (R20UT4861ED0300, Rev.3.00)

It's recommended to use the corresponding document or other later versions.

3. Software and Hardware Tools

This section contains information about the tools used to implement the clock monitoring application.

3.1 Development Tools

The compiler used for the sampling software is Green Hills Multi (GHS).

The required version of the GHS compiler for U2A-EVA devices is V7.1.6/2019 or later.

The EXEC, 850eserv2 and device files are also required before compiling the application code. For further information, please refer to the Getting started software package *RH850U2A_GettingStarted_Vx.00.*

3.2 Emulator E2

The Renesas E2 emulator is required for debugging.

3.3 RH850/U2A-EVA Evaluation boards

The following evaluation boards are used in this document to implement the clock monitoring application.

3.3.1 Starter Kit Board

The Starter Kit Board Version 3, Y-ASK-RH850U2A16 carries the target device. The SW in this document is performed on the RH850/U2A16 device R7F702300EABA-C within these Starter Kit boards. The software uses the User LEDs on the Starter Kit. A removable crystal oscillator was used to test the functionality of clock monitoring.

4. General Features

The Clock monitor (CLMA) can detect frequency abnormalities in the monitored clock. The monitored and sampling clocks are compared to check if the monitored clock is within a specified range. When the clock monitor detects an Error, it sends the error notification to the Error Control Module.

4.1 List of clock sources

The clocks generated from clock oscillators and output to CPU, Bus and peripherals are clock sources. Table 4-1 shows the list of clock sources and the typical working frequencies of them.

Table 4-1 List of Clock Sources[*1]

Clock Name	Symbol	Clock frequency (MHz)	Clock Source
High voltage internal oscillator	CLK_HVIOSC	16	
Low speed internal oscillator	CLK_LSIOSC	0.24	
High speed internal oscillator	CLK_HSIOSC	200	
Main oscillator	CLK_MOSC	16, 20, 24, 40	
Internal OSC clock	CLK_IOSC	0.24	CLK_LSIOSC
		200	CLK_HSIOSC
PLL	CLK_PLL	800, 640, 480	CLK_MOSC
	CLK_PLLO	800, 640, 480 or 400, 320, 240[*2]	CLK_PLL
System clock	CLK_SYS	0.24, 200	CLK_IOSC
		800, 640, 480 or 400, 320, 240	CLK_PLLO

Notes: 1. For detailed information please refer to Application Note “Clock Supply” R01AN4593EDxxxx_RH850_U2A.

2. The output frequency of the PLL depends on the selection of clock divider. Please notice that within this output frequency, the maximal applicable CPU / system clock is 400, 320 or 240 MHz.

4.2 List of clock monitors

Each Clock monitor monitors one Clock and takes a Sampling Clock as reference.

Table 4-2 List of Clock Monitors

Clock Monitor	Monitored Clock	Monitored Clock Accuracy	Sampling Clock	Sampling Clock Accuracy
CLMA0	CLK_MOSC	±0.1%*1	CLK_HSIOSC/400	±5%
CLMA1	CLK_WDT (HS IntOSC 1/20, 1/640)	±5%	CLK_LSIOSC/2	±10%
CLMA2	CLK_LSIOSC	±10%	CLK_HSIOSC/1600	±5%
CLMA3*3	CLK_LSB	±0.1%*1	CLK_MOSC/8	±0%
CLMA4*4	CLK_LSB	±0.1%*1*2	CLK_HSIOSC/20	±0%
CLMA5	CLK_UHSB/2 (Target: GTM Main Clock)	±0.1%*1	CLK_LSB/4	±0%
CLMA6	CLK_CPU/4 (Target: PE0 checker Clock)	±0.1%*1	CLK_LSB/4	±0%
CLMA7	CLK_CPU/4 (Target: PE1 checker Clock)	±0.1%*1	CLK_LSB/4	±0%
CLMA8	CLK_CPU/4 (Target: PE2 checker Clock)	±0.1%*1	CLK_LSB/4	±0%
CLMA9	CLK_CPU/4 (Target: PE3 checker Clock)	±0.1%*1	CLK_LSB/4	±0%

Notes: 1. Depends on the accuracy of the external parts.
2. This is the value of “CLK_LSB = CLK_IOSC”
3. CLMA3 is only available, if PLL clock is source of CLK_SYS.
4. CLMA4 is only available, if CLK_IOSC is source of CLK_SYS

5. Detailed Description

The following Section describes the Architecture of the Clock Monitor and how to calculate the Limits.

5.1 Operating Principle

The Monitored Clock is connected to a 12-bit counter. On each rising edge of the Monitored Clock, the bit counter increases. Before starting the Clock monitor, the Lower and Higher Limits get set. They represent the minimum and maximum number of cycles of the Monitored Clock. After 16 cycles of the Sampling Clock, the counter is compared to the lower and higher limit. If the value does not fall in the specified range, an error is forwarded to ECM.

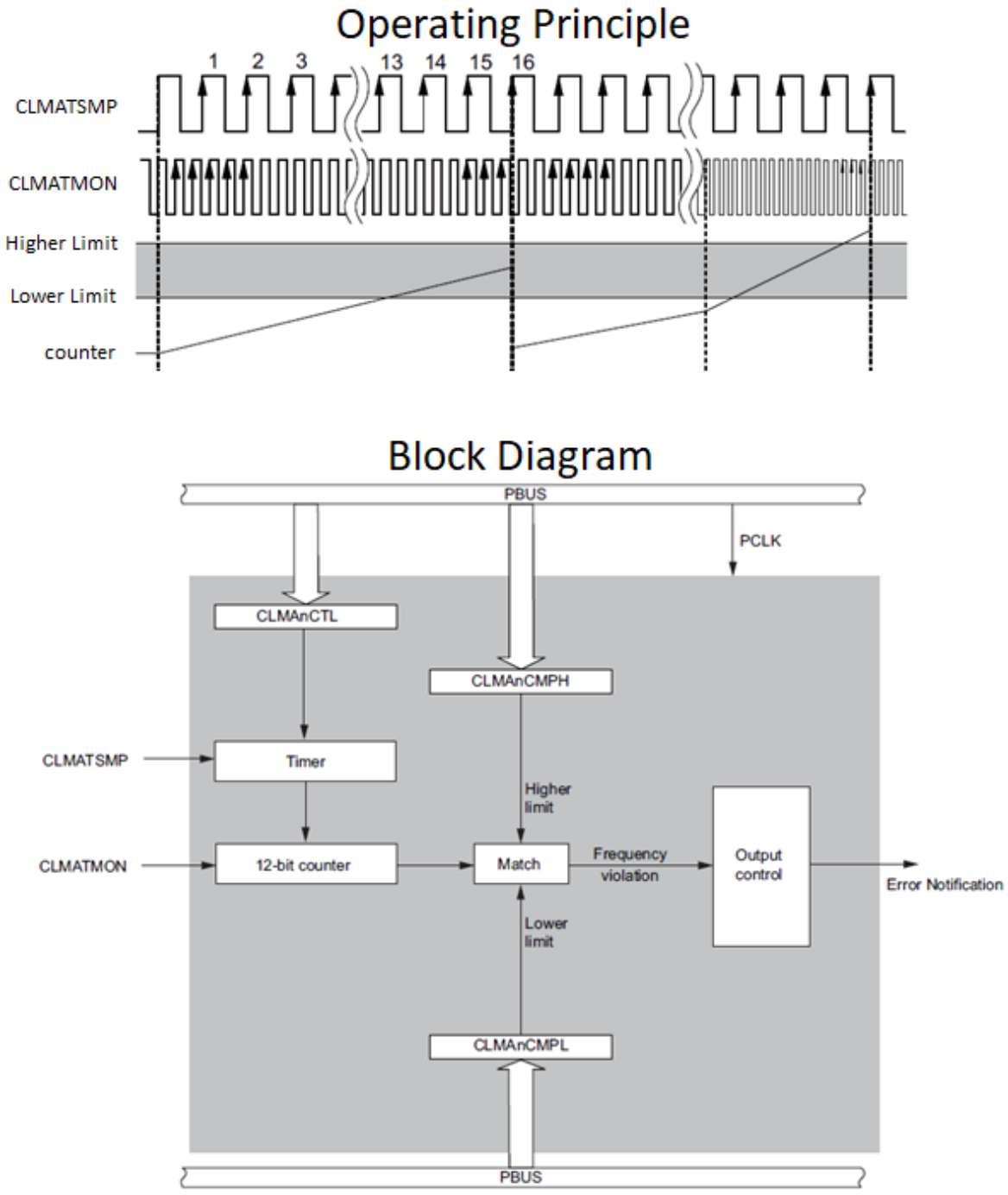

Figure 5-1 Operating Principle and Block Diagram of Clock Monitor

5.2 Calculation of Limits

For setting the comparison Registers, the higher and lower limits can be calculated using the following formulas:

Lower Limit $= \frac{f_{CLMATMON(\min)}}{f_{CLMATSMP(\max)}} \times 16 - 1$

Higher Limit $= \frac{f_{CLMATMON(\max)}}{f_{CLMATSMP(\min)}} \times 16 + 1$

The minimal and maximal frequencies for the monitored and sampling clock can be calculated with the formulas below. Please notice that the Frequencies of both clocks often need to be divided by a constant. For more information and details about accuracy, please refer to table 4-2. The accuracy may depend on external Parts.

Minimal accepted monitored frequency:

$$f_{CLMATMON(\min)} = f_{CLMATMON} - accuracy \times f_{CLMATMON}$$

Maximal accepted monitored frequency:

$$f_{CLMATMON(\max)} = f_{CLMATMON} + accuracy \times f_{CLMATMON}$$

Minimal sampling frequency:

$$f_{CLMATSMP(\min)} = f_{CLMATSMP} - accuracy \times f_{CLMATSMP}$$

Maximal sampling frequency:

$$f_{CLMATSMP(\max)} = f_{CLMATSMP} + accuracy \times f_{CLMATSMP}$$

5.3 Configuration of CLMA

This chapter describes the Configuration of CLMA, including a brief overview of the used Registers for Configuration and self-test.

5.3.1 Registers

The registers listed in Table 5-1 are used for Configuration and self-test of CLMA.

Table 5-1 List of CLMA registers

Register	Function
CLMAPRKCPROT	Sets and unsets writing protection Write A5A5A501$_H$ to disable writing protection Write A5A5A501$_H$ to enable writing protection
CLMAnCMPL	Sets the lower limit of CLMA
CLMAnCMPH	Sets the higher limit of CLMA
CLMAnCTL	Enables or disables CLMA Write 01$_H$ to enable CLMA Write 0 to disable CLMA
CLMACCLMATEST	Sets Test modes for CLMAs (*see Chapter 8: Self-Test of clock monitor for reference*)
CLMACCLMATESTS	Only used during self-test. Monitors the error flags which are otherwise forwarded to ECM

Note: Replace “n” with the desired clock monitor number.

5.3.2 Workflow of setting CLMA

Note: In the following the CLMA number is referred to as “n”. Please make sure to change the register names according to the desired CLMA.

The setup process of Initializing the CLMA can be described as follows:

To avoid CLMA error notifications during initialization, the CLMA should only be initialized if both the sampling clock and the monitored clock are oscillating stable. Only if both clocks are stable, the initialization may begin.

To enable writing to certain CLMA registers, the CLMA writing protection needs to be disabled. This is done by writing A5A5A501$_H$ to CLMAPRKCPROT.

After disabling the write protection, the lower and higher limit (referring to chapter 5.2 “Calculation of Limits”) can be written to CLMAnCMPL (lower limit) and CLMAnMPH (higher limit).

The Clock Monitor can now be enabled by writing 01$_H$ to CLMAnCTL.

After configuring the CLMA, the writing protection should be enabled by writing A5A5A500$_H$ to CLMAPRKCPROT.

6. Error Control Module

The Error Control Module (ECM) monitors various failure detection states of the device and defines the operation to be carried out upon failure detection.

For this application the ECM is used to check and describe the response to the errors forwarded on CLMA errors. In the following, the process of checking the ECM for CLMA Errors and configuration of the ECM is described.

6.1 Checking for CLMA Errors

The errors collected in the ECM can be read by ECMMESST0 – ECMMESST10. Only ECMMESSTR0, ECMMESSTR1, ECMMESSTR7, ECMMESSTR8, ECMMESSTR9 and ECMMESSTR10 are relevant for clock monitor applications.

Table 6-1 List of Error sources

Error source	Register	Bit (beginning from LSB = 0)
CLMA0	ECMMESSTR1	16
CLMA1	ECMMESSTR1	17
CLMA2	ECMMESSTR1	18
CLMA3	ECMMESSTR1	19
CLMA4	ECMMESSTR1	20
CLMA5	ECMMESSTR1	21
CLMA6	ECMMESSTR7	5
CLMA7	ECMMESSTR8	5
CLMA8	ECMMESSTR9	5
CLMA9	ECMMESSTR10	5
ECM Status*1	ECMMESSTR0	0

Notes: 1. ECM Status shows the inverted state of all bits connected by or.
ECM Status is 1, if no error has occurred.
ECM Status is 0, if an error has occurred.

6.2 Configuration of ECM

Before the ECM is configured, the ECM should be initialized.

In the software example the error thrown by CLMA0 is configured as Software-Reset.
The Configuration is executed in 2 Steps:

1. Each ECM-Reset is configured as application-reset by setting SYSCTRLRESC0 to 1.
2. The Error from CLMA0 is configured as reset by setting the according bit of ECMIRCFGn.
   The Register number and bit are the same as ECMMESSTRn.
   (For CLMA0 the 16th bit of ECMIRCFG1 needs to be set)

Note: Both registers are protected.
SYSCTRLRESC0 is protected by SYSCTRLRESKCPROT0.
ECMIRCFGn is protected by ECMCPROT.
To enable write Protection, write A5A5A500$_H$ to the protection Register.
To disable write Protection, write A5A5A501$_H$ to the protection Register.

7. Self-Test of clock monitor

To ensure the proper function, each CLMA can be self-tested. The CLMA is set into Self-Test mode with CLMATEST. During the self-test, the limits are purposefully set to generate an error. When in self-test-mode, errors get forwarded to CLMATESTS instead of ECM. After waiting for the clock detection Time, CLMATESTS can be checked.
If CLMATESTS shows an error, the Self-Test was successful and the CLMA can be Configured.
If CLMATESTS does not show an error, the Self-Test failed.

The following Registers are relevant to the self-test:

- **CLMATEST**

  The Clock Monitor Test register is used to enable the test mode for each CLMA, define its error settings during self-test and reset CLMA.

- **CLMATESTS**

  The Clock Monitor Test Status Register monitors the error detection flags which are otherwise forwarded to the ECM during self-test. The bit number corresponds to the CLMA number (CLMAn). If the ERRS bit for the corresponding CLMA is set, the CLMA did throw an error.

7.1 Procedure for self-test

The procedure for the self-test is described below. “n” corresponds to the Clock Monitor Number (0-9).

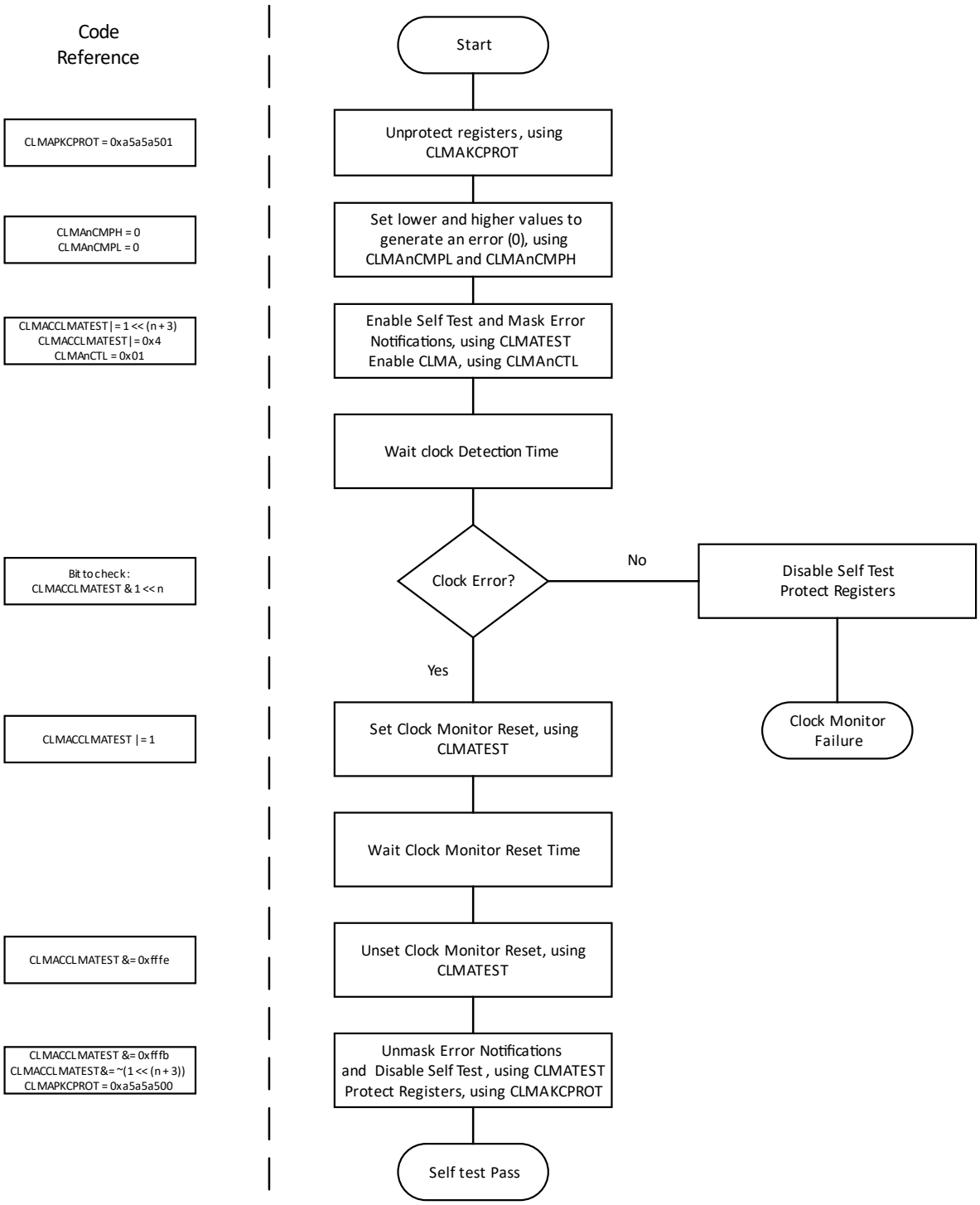

Figure 7-2 Self-Test procedure in sample SW

8. Description of Attachments

8.1 Sample Software

The corresponding sample software of this document can be found in the attachment file: *r20an0713ed0100_rh850_u2a_sw.7z*.
It is based on the software tools and hardware setups described in Section 3. The target device of the software is the RH850/U2A16 device R7F702300BFABA-C, the device files in the package DF-RH850U2A-EE_V130.zip is used for the sample SW. Please notice that the latest device files are always recommended for the SW development.
The sample software is executed from core 0, it contains the configuration of CLMA functions, ports configuration, clock configuration and the main function.
The software includes optional UART outputs, identically to messages on debug Terminal.

In the following each file with its functions are listed:

Table 8-1 CLMA-Related Functions in sample SW

Function Name	Location in SW Package	Description
main	U2A16_GHS_CLMA\src_mca\main_pe0.c	configures ECM, self-tests and initializes CLMA, Initializes LEDs, Initializes main Oscillator output
init_ecm_low	U2A16_GHS_CLMA\src_mca\r_ecm.c	Initializes ECM and clears all ECM error sources and error flags
set_ecm	U2A16_GHS_CLMA\src_mca\r_ecm.c	Configures the CLMA0 error-bit as software reset
check_for_reset	U2A16_GHS_CLMA\src_mca\r_ecm.c	Checks the ECM-Flag of RESF and clears it afterwards to determine, if a CLMA-Reset occurred.
selfTest	U2A16_GHS_CLMA\src_mca\r_clma.c	Tests, if CLMA0 is working correctly. Returns 1, if self-test passed Returns 0, if self-test failed
enableCLMA	U2A16_GHS_CLMA\src_mca\r_clma.c	Waits for stable monitored and sampling clock and enables CLMA
	U2A16_GHS_CLMA\src_mca\r_rlin.c	Rlin initialization and string transmission used for UART
	U2A16_GHS_CLMA\src_mca\r_uart.c	Functions for UART initialization and string transmission

8.2 Excel Tool

The Excel tool is provided to simplify the calculation of limits which is described in Chapter 5.2. It can be found in the attachment file: *r20an0713ed0100_rh850_u2a_CLMA_calculation.xlsx*.

After entering the configuration details, the values for CLMAnCMPL and CLMAnCMPH are automatically calculated.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 02. 2024		First release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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TOYOSU FORESIA, 3-2-24 Toyosu,
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