Determining the Open-Loop Output Impedance of Rad Hard Op-Amps

Introduction

The open-loop output impedance, Z_O, of an operational amplifier (op-amp) is the inherent impedance of its output stage without external feedback applied. Z_O is design dependent. It interacts with capacitive loads, which can destabilize an amplifier circuit (Figure 1).

As the design equations for capacitive load compensation techniques require the knowledge of Z_O, it is necessary to understand how to derive its value.

Note: Z_O must not be confused with the closed-loop output impedance of an amplifier circuit, Z_{OUT}, which is a function of Z_O, and much lower in value due to applied feedback (Figure 1).

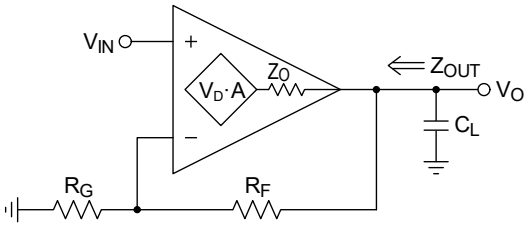

Figure 1. Figure 1. Open-Loop Output Impedance, Z_O

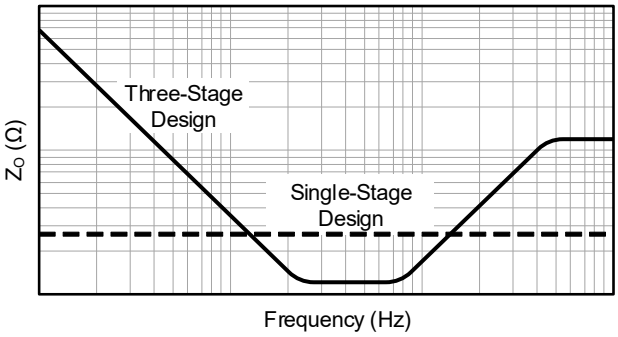

Figure 2. Figure 2. Design Dependent Z_O Characteristics

Legacy op-amps with a single-stage BJT output feature a flat resistive Z_O characteristic over frequency. The precision op-amps discussed in this application note feature a three-stage design, which is reflected in their three-stage Z_O characteristic over frequency. (Figure 2).

This application note explains the method of determining the Z_O characteristics for Renesas ISL70244, ISL70227, ISL70218, and ISL70219A families of radiation-hardened dual op-amps. These characteristics also apply to the quadruple op-amp versions of these devices.

Contents

© 2026 Renesas Electronics

1. Open-Loop versus Closed-Loop Output Impedance

The closed-loop output impedance can be determined by driving a current of constant amplitude into the output of an amplifier circuit while measuring the output voltage (Figure 3). Therefore, the closed-loop output impedance is the ratio of output voltage to input current:

(EQ. 1) $$Z_{OUT} = \frac{V_O}{I_{IN}}$$

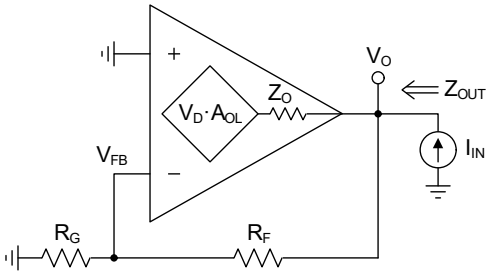

Figure 3. Z_O versus Z_{OUT}

Making the value of the feedback resistor significantly larger than the maximum anticipated value of Z_O ($R_F >> Z_O$) ensures that I_{IN} solely flows into the op-amp output and through Z_O. This creates a voltage across Z_O of $I_{IN} \times Z_O = V_O - V_D \times A$. As the non-inverting input is grounded (0V), the differential input voltage is $V_D = -V_O \times \beta$, with β as the feedback factor $R_G/(R_F + R_G)$. This makes the voltage across Z_O:
$I_{IN} \times Z_O = V_O + V_O \times A_{OL} \times \beta = V_O(1 + A_{OL} \times \beta)$ and solving for I_{IN} gives:

(EQ. 2) $$I_{IN} = \frac{V_O(1 + A_{OL} \times \beta)}{Z_O}$$

Then, substituting I_{IN} in Equation 1 with Equation 2 yields:

(EQ. 3) $$Z_{OUT} = \frac{Z_O}{1 + A_{OL} \times \beta}$$

Equation 3 shows that the closed-loop output impedance is the open-loop output impedance reduced by the loop-gain, $A_{OL} \times \beta$. Then, solving Equation 3 for Z_O gives:

(EQ. 4) $$Z_O = Z_{OUT}(1 + A_{OL} \times \beta)$$

Equation 4 shows that finding the open-loop output impedance requires the measurements of open-loop gain and closed-loop output impedance.

2. Measuring the Open-Loop Gain (A_{OL})

Measuring A_{OL} uses the inverting amplifier configuration to avoid input common-mode error. Choosing a high circuit gain of $R_F/R_G \geq 100$ eliminates the effect of the parasitic input capacitance, C_P. Installing the input capacitance, C_G, sets the DC gain of 1, therefore, preventing any input offset from being amplified. Using a network analyzer to measure the ratio of output-to-feedback voltage yields the open-loop gain: $A_{OL} = -V_O/V_{FB}$.

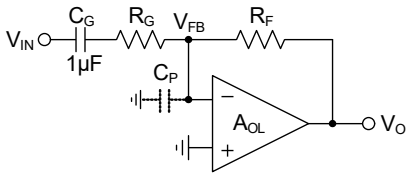

Figure 4. A_{OL} Measurement Circuit

Figure 5 to Figure 8 show the open-loop gain and phase responses for the respective op-amps.

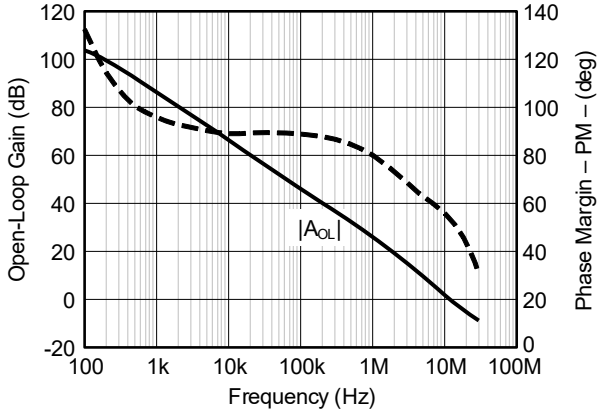

Figure 5. ISL70244: Open-Loop Gain & Phase

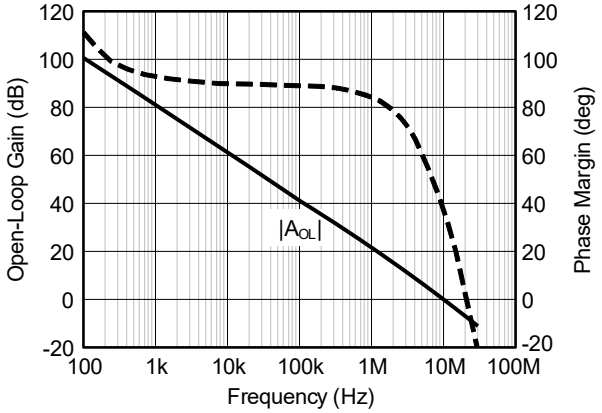

Figure 6. ISL70227: Open-Loop Gain & Phase

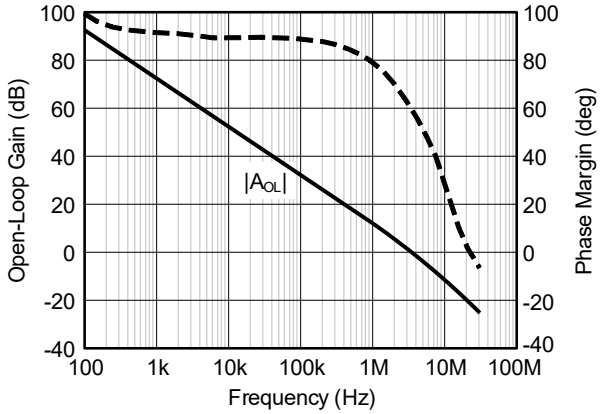

Figure 7. ISL70218: Open-Loop Gain & Phase

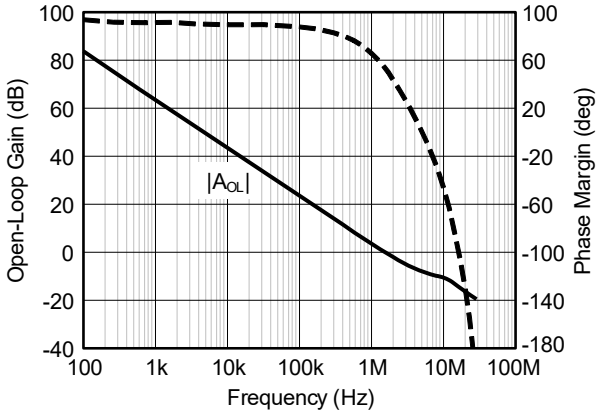

Figure 8. ISL70219A: Open-Loop Gain & Phase

3. Deriving Closed-Loop (Z_{OUT}) and Open-Loop (Z_O) Output Impedance

According to Equation 1, $Z_{OUT} = V_O / I_{IN}$. As high-frequency current sources with constant amplitude do not extend into the MHz range, a high-frequency voltage source, V_{IN}, and a series resistor, R_S, are used to generate I_{IN}.

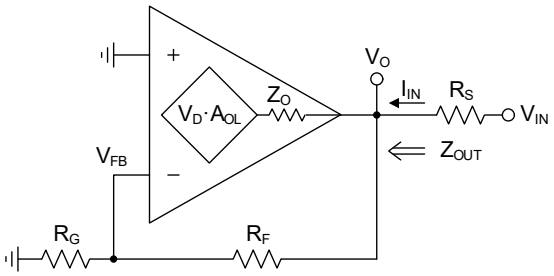

Figure 9. Measurement Circuit to Establish Z_{OUT}

Therefore, the input current is defined by:

(EQ. 5) $$I_{IN} = \frac{(V_{IN} - V_O)}{R_S}$$

Substituting I_{IN} in Equation 1 with Equation 5 gives:

(EQ. 6) $$Z_{OUT} = \frac{R_S}{V_{IN}/V_O - 1}$$

As the circuit in Figure 9 measures the reciprocal voltage ratio, V_O/V_{IN}, Equation 6 is rewritten as:

(EQ. 7) $$Z_{OUT} = \frac{R_S}{1/(V_O/V_{IN}) - 1}$$

After calculating Z_{OUT}, use the A_{OL} values found in Measuring the Open-Loop Gain (A_{OL}) to calculate Z_O with Equation 4: $Z_O = Z_{OUT} \times (1 + A_{OL}\beta)$.

All equations use complex values, consisting of magnitude and phase. As only the magnitude of Z_O is of interest, the magnitude of Equation 4 is:

(EQ. 8) $$|Z_O| = |Z_{OUT}| \times |1 + A_{OL}\beta|$$

Deriving the magnitude function of Equation 7 gives:

$$|Z_{OUT}| = \frac{R_S}{\sqrt{\left[\cos\left(-\phi_{V_O/V_{IN}}\right)/|V_O/V_{IN}| - 1\right]^2 + \left[\sin\left(-\phi_{V_O/V_{IN}}\right)/|V_O/V_{IN}|\right]^2}}$$

Also, the magnitude of the 1+Aβ term is:

$$|1 + A_{OL}\beta| = \sqrt{[1 + |A_{OL} \times \beta| \times \cos(\phi_{Aol})]^2 + [|A_{OL} \times \beta| \times \sin(\phi_{Aol})]^2}$$

Inserting both into Equation 8 gives the magnitude function of Z_O:

(EQ. 9)
$$|Z_O| = R_S \times \sqrt{\frac{[1+|A_{OL}\times\beta|\times\cos(\phi_{Aol})]^2+[|A_{OL}\times\beta|\times\sin(\phi_{Aol})]^2}{\left[\cos\left(-\phi_{V_O/V_{IN}}\right)/|V_O/V_{IN}|-1\right]^2+\left[\sin\left(-\phi_{V_O/V_{IN}}\right)/|V_O/V_{IN}|\right]^2}}$$

Figure 10 to Figure 13 show the Z_{OUT} and Z_O characteristics for each op-amp family.

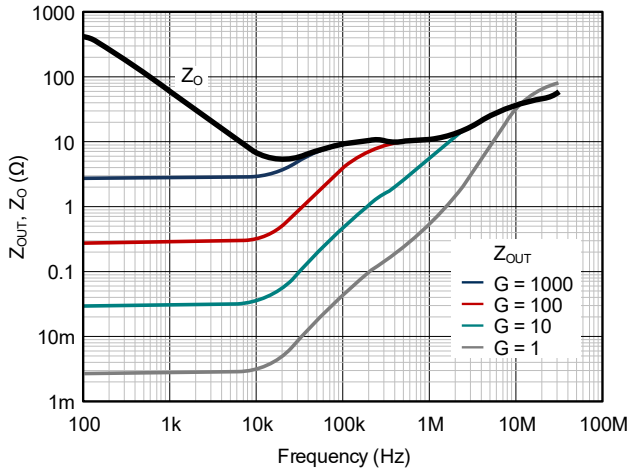

Figure 10. ISL70244 (19MHz): Z_O and Z_{OUT}

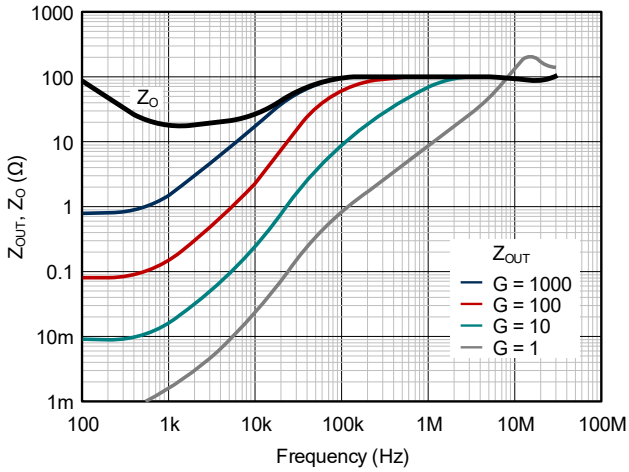

Figure 11. ISL70227 (10MHz): Z_O and Z_{OUT}

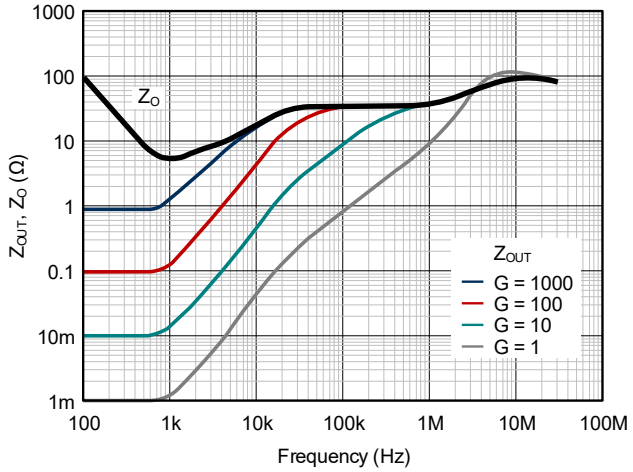

Figure 12. ISL70218 (4MHz): Z_O and Z_{OUT}

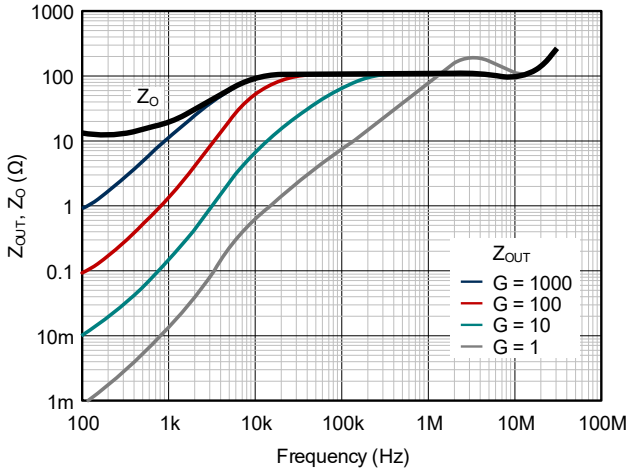

Figure 13. ISL70219A: (1.5MHz): Z_O and Z_{OUT}

4. Conclusion

Figure 14 depicts the open-loop output impedances of all four op-amps. The dotted lines represent the sections for loop-gains smaller one ($A_{OL}\beta < 1$), in other words, outside an op-amp's gain-bandwidth.

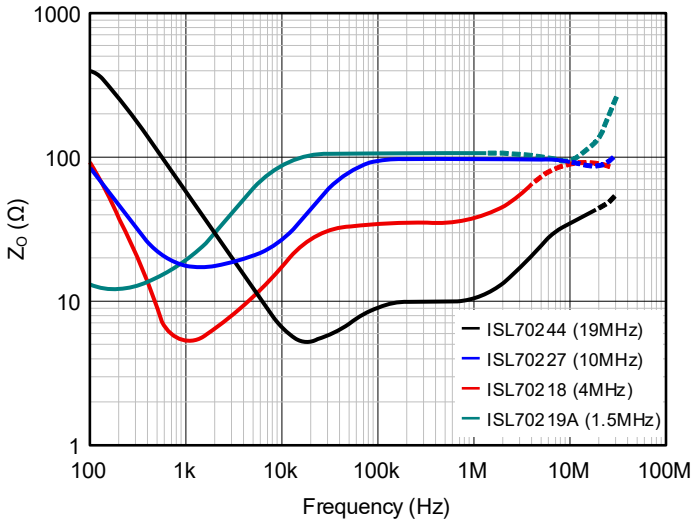

Figure 14. Z_O Characteristics of all Op-Amps

While these curves have been established for a small number of samples at room temperature, the changes in output impedance due to process and temperature variations can be as high as 40%.

Phase compensation techniques that stabilize capacitively loaded amplifier circuits, such as voltage reference buffers, should always use the highest possible Z_O value in their stability calculations. Therefore, Table 1 lists the recommended Z_O values for each op-amp that include a +50% shift from the Z_O value at $A_{OL}\beta = 1$.

Table 1. Recommended Z_O values for Phase Compensation Calculations

Op-amp Family	Gain-Bandwidth (MHz)	Z_O Value (Ω) at $A_{OL}\beta = 1$	
		Measured	Recommended
ISL70244	19	50	100
ISL70227	10	100	200
ISL70218	4	65	130
ISL70219A	1.5	100	200

5. Revision History

Revision	Date	Description
1.00	Feb 3, 2026	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2026 Renesas Electronics Corporation. All rights reserved.