

RAA214023 SPICE Model

This document discusses the SPICE model for the RAA214023 LDO including the features supported and not supported by the model. To download the model, see the [RAA214023](#) product page.

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1. Model Features

This Pspice Macromodel is intended to give typical DC and AC performance characteristics under a wide range of external circuit configurations using compatible simulation platforms - such as iSim PE.

1.1 Device Performance Features Supported

The following are the device performance features that are supported by this model:

- Device parameters are set to typical room temperature values
- Output voltage programmed using internal and external resistors
- Gain and phase
- Input noise terms including $1/f$ effects
- PSRR
- Transient V_{IN} , V_{OUT} , and Load. Reference the Excel spreadsheet that is included with the SPICE software ([Figure 1](#)) for test results (RAA214023 SPICE model Validation.xlsx).
- Output current limit
- Enable and Disable function using the Enable pin
- Power-good using the PG pin.
- UVLO <1V and 300 Ω output impedance.
- 300 Ω output pull-down when part is disabled and $V_{IN} > 1V$.
- 300 Ω output pull-down when part is enabled and $1V < V_{IN} < 2.5V$.

1.2 Device Performance Features NOT Supported

The following are the device performance features that are NOT supported by this model:

- Harmonic distortion effects
- Thermal effects and/or over-temperature
- Parameter variation
- Part-to-part performance variation because of normal process parameter spread
- Any performance difference arising from different packaging

2. Downloading and Running the Software

The RAA214023 SPICE model software can be down loaded from the [RAA214023](#) product page.

Save the file to a common directory for your SPICE simulations. This application note assumes you have a basic knowledge of running SPICE simulations. To open the software, click on the file titled **RAA214023FDSPICEMODELrev01.opj** (highlighted in [Figure 1](#)). An Excel spreadsheet is also provided documenting the validation of the model.

Name	Date modified	Type	Size
RAA214023FDSPICEMODELrev01-PSpiceF...	6/2/2021 8:25 AM	File folder	
RAA214023FDSPICEMODELREV01_0.DBK	5/26/2021 3:03 PM	DBK File	537 KB
RAA214023FDSPICEMODELrev01.dsn	6/1/2021 10:44 AM	DSN File	537 KB
RAA214023 SPICE model Verification.xlsx	5/26/2021 5:01 PM	Microsoft Excel W...	619 KB
RAA214023SUBCKTREV01_0.OBK	5/3/2021 12:04 PM	OBK File	41 KB
22uF output Cap.olb	8/28/2020 4:45 PM	OLB File	5 KB
22uFLabOutputCap.olb	8/31/2020 8:15 AM	OLB File	7 KB
22uFoutputCap.olb	8/28/2020 4:46 PM	OLB File	5 KB
LabCap_C1210C226K8R2C.olb	6/2/2021 8:54 AM	OLB File	7 KB
RAA214023FDSUBCKT.olb	5/13/2021 3:51 PM	OLB File	40 KB
RAA214023SUBCKTREV00.olb	5/13/2021 8:44 AM	OLB File	10 KB
RAA214023SubCKTrev01.olb	5/3/2021 12:06 PM	OLB File	41 KB
RAA214023SubCKTrev02.olb	5/13/2021 3:24 PM	OLB File	43 KB
RAA2214020SubCKTFDrev02.olb	1/14/2021 8:45 AM	OLB File	39 KB
special.olb	8/18/2009 9:23 PM	OLB File	51 KB
RAA214023FDSPICEMODELrev01.opj	6/2/2021 8:52 AM	OPJ File	12 KB
22uF output Cap.lib	8/28/2020 4:45 PM	PSpice Model Libr...	1 KB
22uFLabOutputCap.lib	8/31/2020 8:24 AM	PSpice Model Libr...	1 KB
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diodenoise.lib	8/31/2020 3:33 PM	PSpice Model Libr...	1 KB
LabCap_C1210C226K8R2C.lib	6/2/2021 8:54 AM	PSpice Model Libr...	1 KB
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pmsbottomcascode.lib	8/20/2020 11:44 AM	PSpice Model Libr...	1 KB
pmscascodeepm16.lib	8/20/2020 3:43 PM	PSpice Model Libr...	1 KB
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raa214023subcktrev00.lib	5/11/2021 2:44 PM	PSpice Model Libr...	14 KB
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schmitttriggerlh.lib	5/12/2021 3:30 PM	PSpice Model Libr...	1 KB
schmitttriggerll.lib	8/14/2020 2:11 PM	PSpice Model Libr...	1 KB

Figure 1. RAA214023 SPICE Model Software

The screen shown in [Figure 2](#) appears. The test circuits for PSRR, Gain Phase, Noise, Schematic, SCHNetlist, TransLoad, TransLoad, TransVIN, TransVout, and TransVOUExternalR are all setup. To run the different tests, click the down arrow and select the test you want to run (red arrow). You might need to right click on the specific test and **Make Root** to get it to run. To see the test schematic, double click on **PAGE 1** and the schematic with the RAA214023SUBCKTREV01 appears.

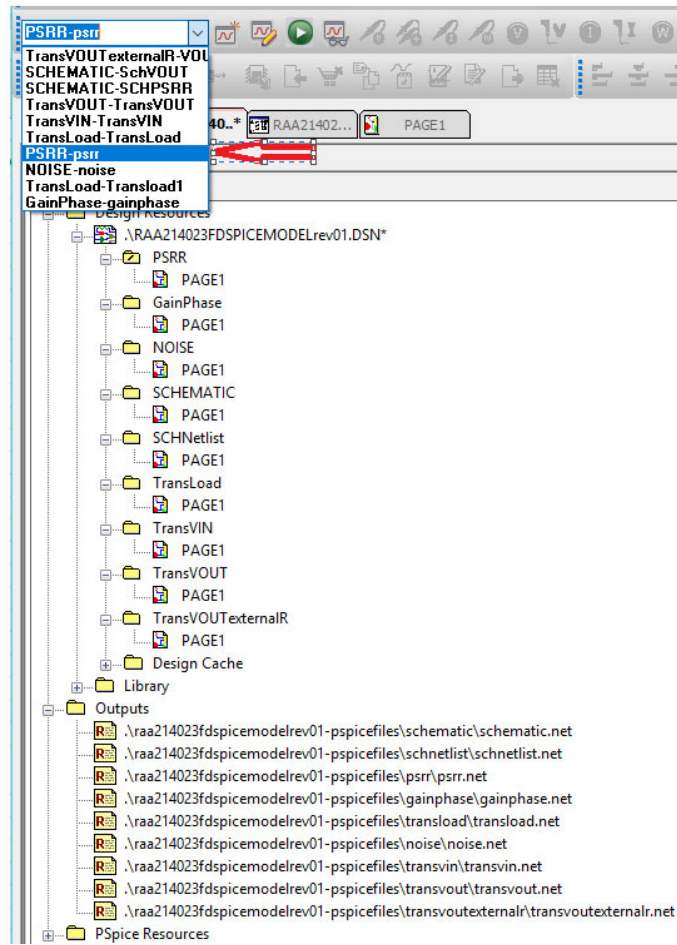


Figure 2. SPICE Software Test Selection Window

Note: All pins need to be connected on the SubCKT to avoid errors during net listing. Figure 3 shows the correct and incorrect connection of the RAA214023 output voltage programmed to 3.3V with the internal resistors. Pin 3, Pin 5, Pin 7, and Pin 9 are floating to achieve this. You must connect a wire to the floating pins.

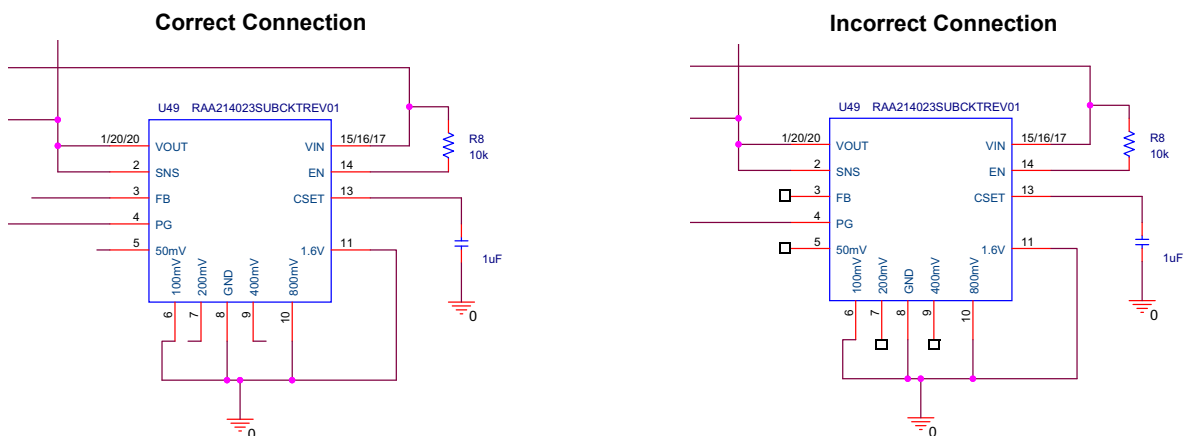


Figure 3. Floating Pins Need to be Connected

Figure 4 shows the PSRR test circuit.

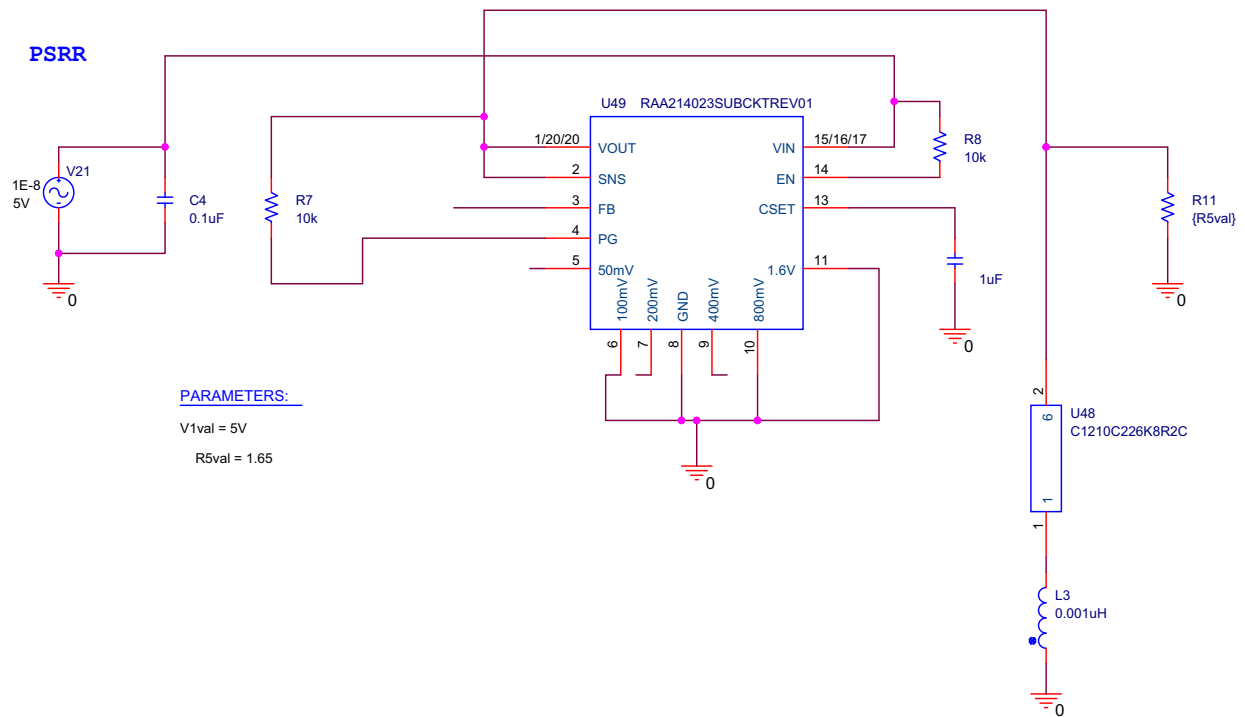


Figure 4. RAA214023SUBCKTREV01 PSRR Test Circuit

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4. Revision History

Revision	Date	Description
1.0	Jun 16, 2021	Initial release

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