RA4W1 Group

Guidelines for 2.4 GHz Wireless Board Design

Introduction

This document describes RF board design guidelines for RF transceiver.

Target Device

RA4W1 Group

Note: The contents of this document are provided as a reference and do not guarantee the signal quality in the system. When designing the actual system, thoroughly evaluate the product in the overall system and apply these contents on your own responsibility.

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1. Overview

This document shows board design guidelines for the RF transceiver part.

1.1 Related documents

The following documents are related to this application note. Also refer to these documents when using this application note.

- [1] Tuning procedure of Bluetooth dedicated clock frequency (R01AN4887).
- [2] RA4W1 User's Manual: Hardware (R01UH0883).

Note: The latest version of each document (R01*) can be downloaded from the Renesas Electronics website.

2. Board design guidelines

2.1 Pin list of the RF transceiver unit

Table 2-1 shows the RF transceiver unit pins.

Table 2-1 Description of the RF transceiver unit pins

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin Connect it to the system power supply.
	VSS	Input	Ground pin Connect it to the system power supply (0V).
Clock	CLKOUT_RF	Output	The Wireless-dedicated (Bluetooth-dedicated) clock output pin for output of a 1-, 2-, or 4-MHz signal. The default output setting is off. Connecting the clock output pin to the external clock input pin of MCU, the RF clock can be used as the MCU system clock.
	XTAL1_RF	Input	Pins for connecting a 32 MHz crystal resonator of the Wireless-dedicated (Bluetooth-dedicated) clock oscillator.
	XTAL2_RF	Output	
RF	VCC_RF	Input	The RF transceiver power-supply pin
	AVCC_RF	Input	The RF transceiver power-supply pin
	VSS_RF	Input	The RF transceiver ground pin Note: Separate this “pin” from the ground area of the “Exposed Die Pad”, same name as the “VSS_RF” as shown in Figure 2-11.
	ANT	I/O	RF single I/O pin for the RF transceiver Adjust characteristic impedance of a signal line between an antenna and this pin to 50 ohm.
	DCLOUT	Output	The RF transceiver power-supply output pins for the DC-DC converter mode or the linear regulator mode.
	DCLIN_A	Input	The RF transceiver power-supply input pins These pins should be connected to the “DCLOUT” pin via a filter with an external inductor and capacitor when the DC-DC converter mode is selected. When the linear regulator mode is selected, these pins should be connected to the “DCLOUT” with an external decoupling capacitor.
	DCLIN_D	Input	

2.2 Oscillator circuit for the Wireless-dedicated (Bluetooth-dedicated) clock

Note the followings when designing the Wireless-dedicated (Bluetooth-dedicated) clock oscillator circuit.

Figure 2-1 shows an example of the crystal resonator connection. Figure 2-2 shows an example of the pattern around the crystal resonator.

- Place the crystal resonator close to the “XTAL1_RF” and “XTAL2_RF” pins. In case of the Figure 2-2, the distance between these two pins and the crystal resonator is approximately 6 mm.
- Shield lines from the “XTAL1_RF” and “XTAL2_RF” pins to the crystal resonator with the ground pattern. Do not place the pattern for these signals in parallel with or across other patterns where a large current flows or a signal level changes frequently.
- Do not place any signal, power or ground lines other than those for the oscillator circuit on and below the oscillator circuit lines and area. As shown in Figure 2-2, the ground pattern is placed in the layers under the oscillator circuit.
- Separate the oscillator circuit and a signal line from an antenna to the “ANT” pin by placing slit patterns on all layers.
- As shown in Figure 2-2, ensure the return path in layer2, and the layer3 if possible, from ground of the crystal resonator to "Exposed Die Pad (VSS_RF)”.
- Any external load capacitor of the crystal resonator for a frequency tuning of the oscillator is not required, because capacitors to tune the frequency of the oscillator are built in the chip. With respect to the tuning procedure of the Wireless-dedicated (Bluetooth-dedicated) clock frequency, refer to descriptions of the application note [1].
- As shown in Figure 2-1, insert a damping resistor (Rd) as required. Determine the resistance to the value recommended by an oscillator manufacturer as the value depends on the oscillator and its driving capability. A feedback resistor (Rf) between the “XTAL1_RF” pin and the “XTAL2_RF” pin is not required on the board. The feedback component is built in the RF transceiver instead of the Rf.
- The resistance of the Rd and Rf should be determined by oscillation characteristics evaluation with a crystal resonator to be mounted. Theses resistors are not always required, depending on the oscillation characteristics.
- When the Wireless-dedicated (Bluetooth-dedicated) clock from the “CLKOUT_RF” pin is used, the wiring length from the “CLKOUT_RF” pin should be as short as possible. The wire must not branch. The maximum number of Vias of the wiring from the “CLKOUT_RF” pin to the external clock input pin of MCU is tow.
- Shield the transmission line of the “CLKOUT_RF” with the "VSS" pattern to avoid noise coupling to “VSS_RF”.

Note: Carefully consider and determine your crystal resonator in consultation with a crystal resonator manufacturer because the oscillation characteristics depend on a board design. For example, in the case of the Bluetooth 5.0 standard, the transceiver clock frequency tolerance which includes an initial error, a temperature drift, and an ageing effect should be less than or equal to +/– 50 ppm. Especially, the initial error should be minimized as possible by [1].

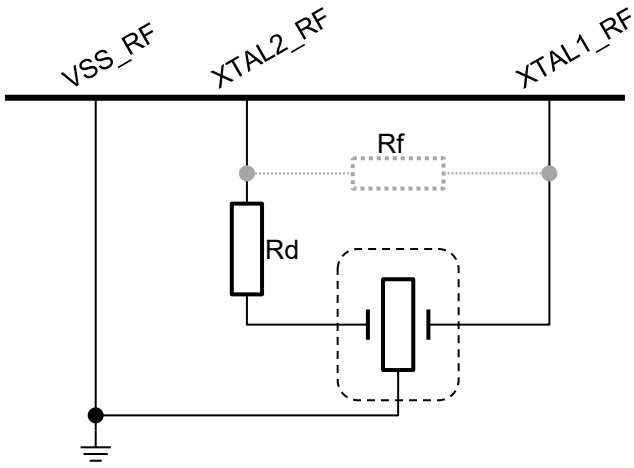


Figure 2-1. Example of the crystal resonator connection

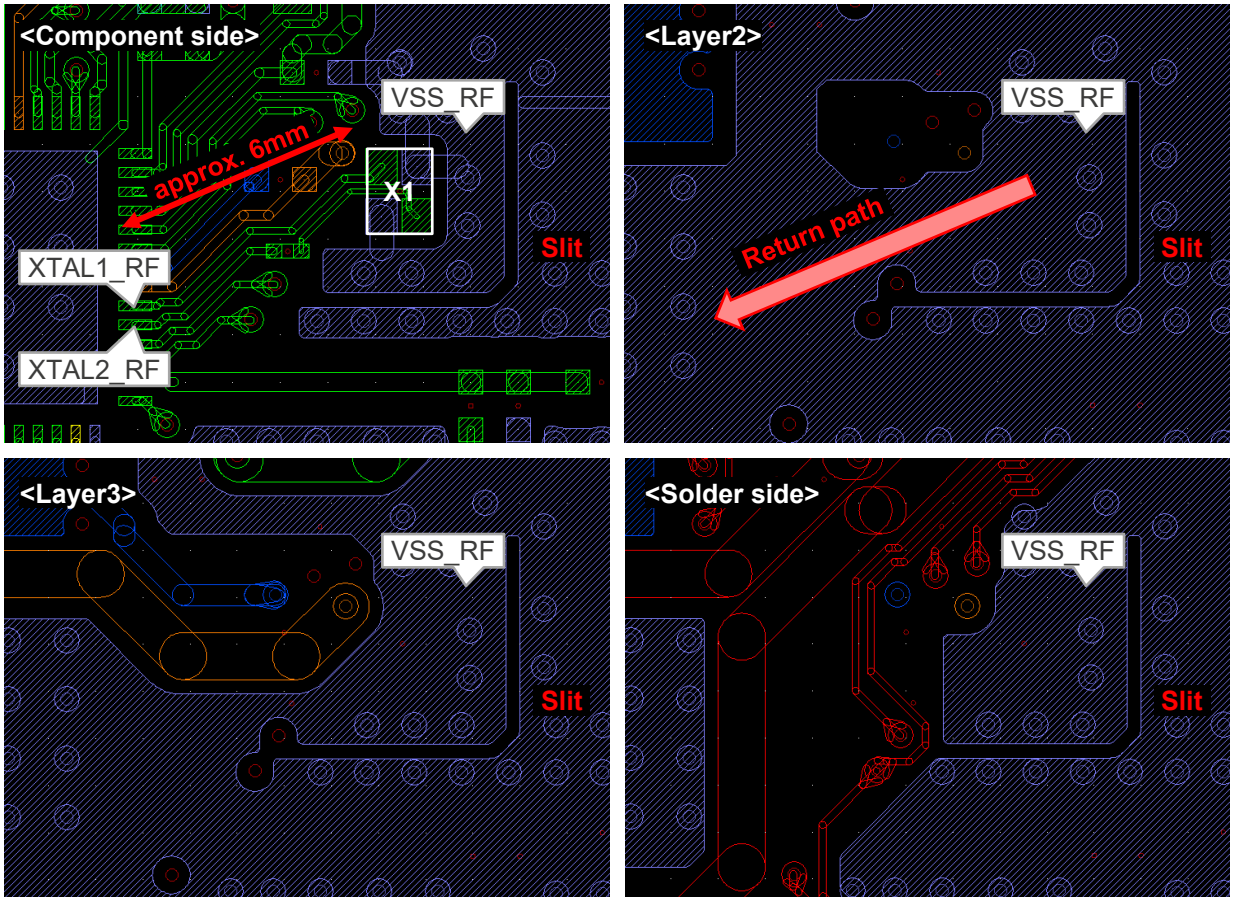


Figure 2-2. Example of the pattern around the crystal resonator

2.3 Antenna Connection pin

Note the followings for the antenna connection line design.

2.3.1 Impedance of the signal line form an antenna to the “ANT” pin

- Adjust the characteristic impedance of 50 ohm for the signal line from an antenna to the “ANT” pin. Design the width of signal line and the gap between signal line and ground pattern, considering the printed circuits board (PCB) permittivity and layer thickness. In the case of Figure 2-3, the signal line is a coplanar waveguide. Depending on the antenna used, additional parts such as inductors or capacitors may be required.
- When mounting a connector, keep the characteristic impedance of 50 ohm including the connector.
- The metal layer at least one level below the coplanar waveguide should be solid ground, having no crossing with any signal, power, and other ground lines.
- Place Vias as many as possible between the coplanar waveguide ground pattern and the solid ground. In the case of Figure 2-3, the Via pitch is approximately 1.0 mm.

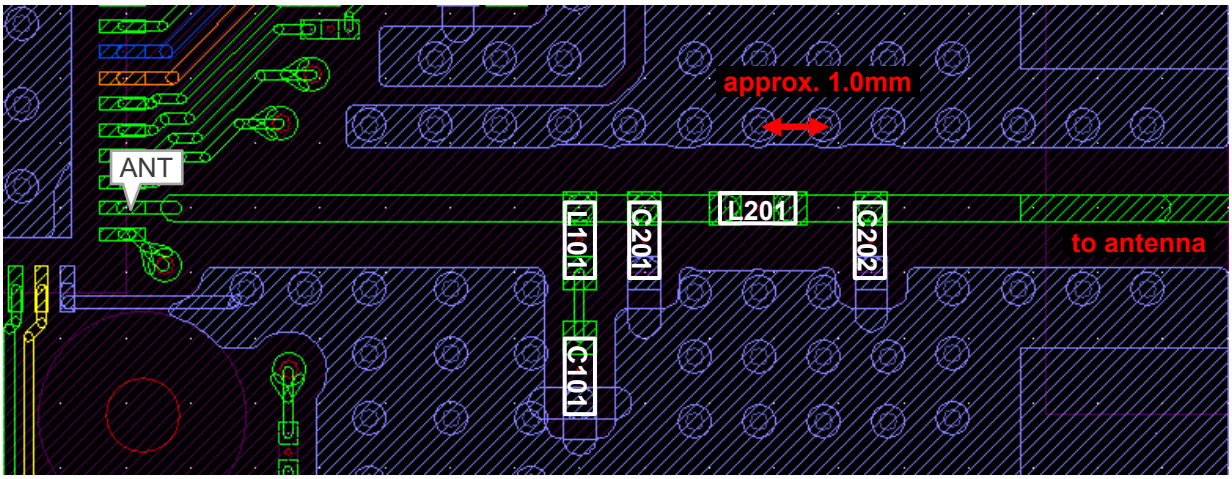
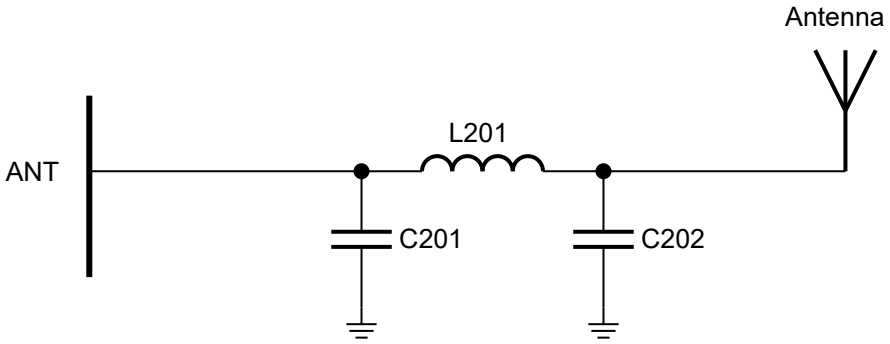


Figure 2-3. Example of the pattern around the “ANT” pin

2.3.2 RF Filter for spurious emissions reduction

- When certifying of Federal Communications Commission (FCC) regulatory, the emission of harmonics in transmission mode should be suppressed with RF filter. Figure 2-4 shows the Pi filter configuration which is suitable for harmonics spurious emission filter. The measurement results of harmonics levels are in Table 2-2. The measured devise under test is RA4W1. Measurements are performed at 2440 MHz, conducted, 4dBm-mode, the DC-DC converter mode, Continuous Wave signal, 3.3 V power supply, and room temperature, using a calibrated spectrum analyzer (Keysight E4440A) and calibrated for cable losses. The output power levels are measured at the SMA output of the device under test.
- It is recommended that the filter SMDs (L201 and C202) should have good high frequency characteristics in order to effectively suppress HD5 or higher.
- All suppression levels of harmonics in transmission mode depend on board pattern and antenna frequency characteristics.



Note: L201: 1.1 nH (MLG1005S1N1ST000)
C201: 0.8 pF (GJM1554C1HR80BB01)
C202: 0.3 pF (GJM1554C1HR30BB01)

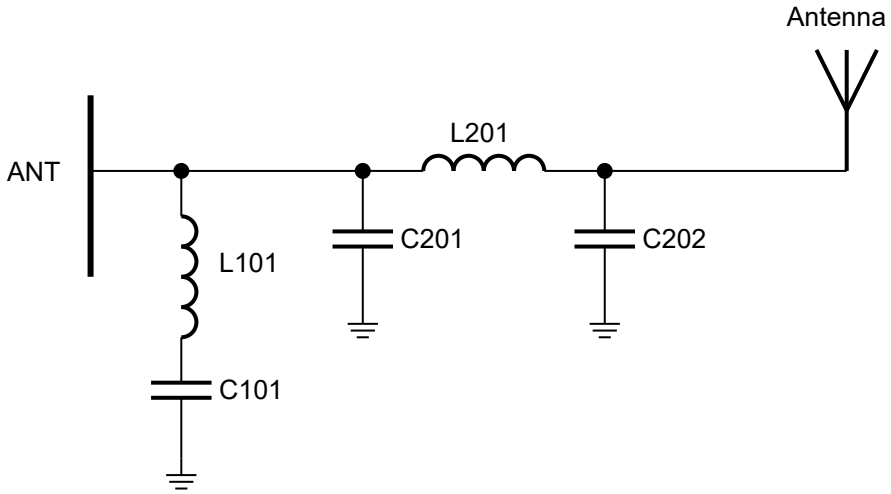
Figure 2-4. Example of the Pi filter configuration

Table 2-2. Measurement results of the spurious emission with the Pi filter

Filter	Fund.	HD2	HD3	HD4	HD5	HD6	HD7	HD8	HD9	HD10
Without	3.0	–53.2	–50.3	–35.5	–47.0	–36.8	–49.7	–49.7	–64.3	–62.2
With	2.4	–52.8	–68.7	–57.7	–62.3	–59.4	–58.8	–55.7	–61.5	–65.2

Notes: 1. All values in dBm.
2. Fund.: Output power of fundamental tone.
3. HD”x”: “x” order Harmonic Distortion.

- When certifying of Korea Communications Commission (KCC) regulatory, an emission in 1.9 GHz frequency band due to LO leakage in reception mode should be suppressed with an RF filter. An LC Notch Filter is suitable for reduction of 1.9 GHz frequency band emission. Figure 2-5 shows the Pi and LC Notch filter configuration. The measurement results of harmonics levels and 1.9 GHz frequency band emission are in Table 2-3. The measured devise under test is RA4W1. Measurements are performed at 2440 MHz, conducted, 4dBm-mode, the DC-DC converter mode, Continuous Wave signal, 3.3 V power supply, and room temperature, using a calibrated spectrum analyzer (Keysight E4440A) and calibrated for cable losses. The output power levels are measured at the SMA output of the device under test. Note that the measured frequency of LO leakage is 1952 MHz (2440 MHz × 4/5).
- It is recommended that the filter SMDs (L201 and C202) should have good high frequency characteristics in order to effectively suppress HD5 or higher.
- All suppression levels of LO Leakage in reception mode and harmonics in transmission mode depend on board pattern and antenna frequency characteristics.



Note: L101: 7.5 nH (LQG15HS7N5J02)
C101: 0.5 pF (GRM1554C1HR50BA01)
L201: 1.1 nH (MLG1005S1N1ST000)
C201: 0.8 pF (GJM1554C1HR80BB01)
C202: 0.3 pF (GJM1554C1HR30BB01)

Figure 2-5. Example of the Pi and LC Notch filter configuration

Table 2-3. Measurement results of the spurious emission with the Pi and LC Notch filter

Filter	Fund.	HD2	HD3	HD4	HD5	HD6	HD7	HD8	HD9	HD10	1.9 GHz Band
Without	3.0	–53.2	–50.3	–35.5	–47.0	–36.8	–49.7	–49.7	–64.3	–62.2	–55.2
With	2.5	–56.5	–69.1	–56.0	–70.0	–59.4	–57.7	–52.7	–61.3	–66.3	–68.4

Notes: 1. All values in dBm.
2. Fund.: Output power of fundamental tone.
3. HD”x”: “x” order Harmonic Distortion.

2.4 Power supply mode for the RF transceiver

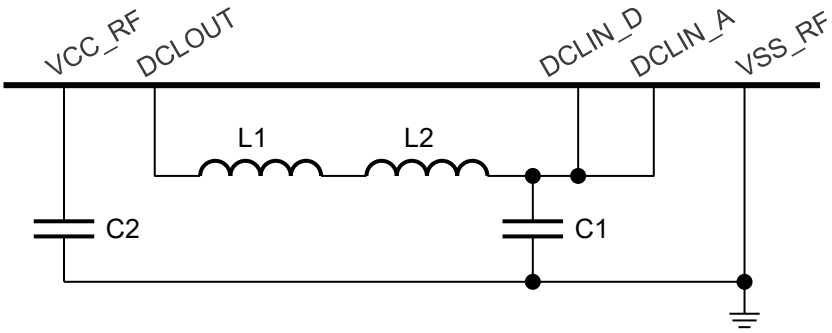
Note the followings for an external circuit design in two power supply modes which are the DC-DC converter mode and the linear regulator mode in the RF transceiver. Users should select the power mode after understanding a trade-off between an operating current and Bill Of Materials (BOM) cost of the RF transceiver. For the lower operating current, User should select the DC-DC converter mode. On the other hand, Users should select the linear regulator mode to reduce inductors, which saves the BOM cost and board area.

2.4.1 DC-DC converter mode

Note the followings for an external circuit design of the DC-DC converter mode.

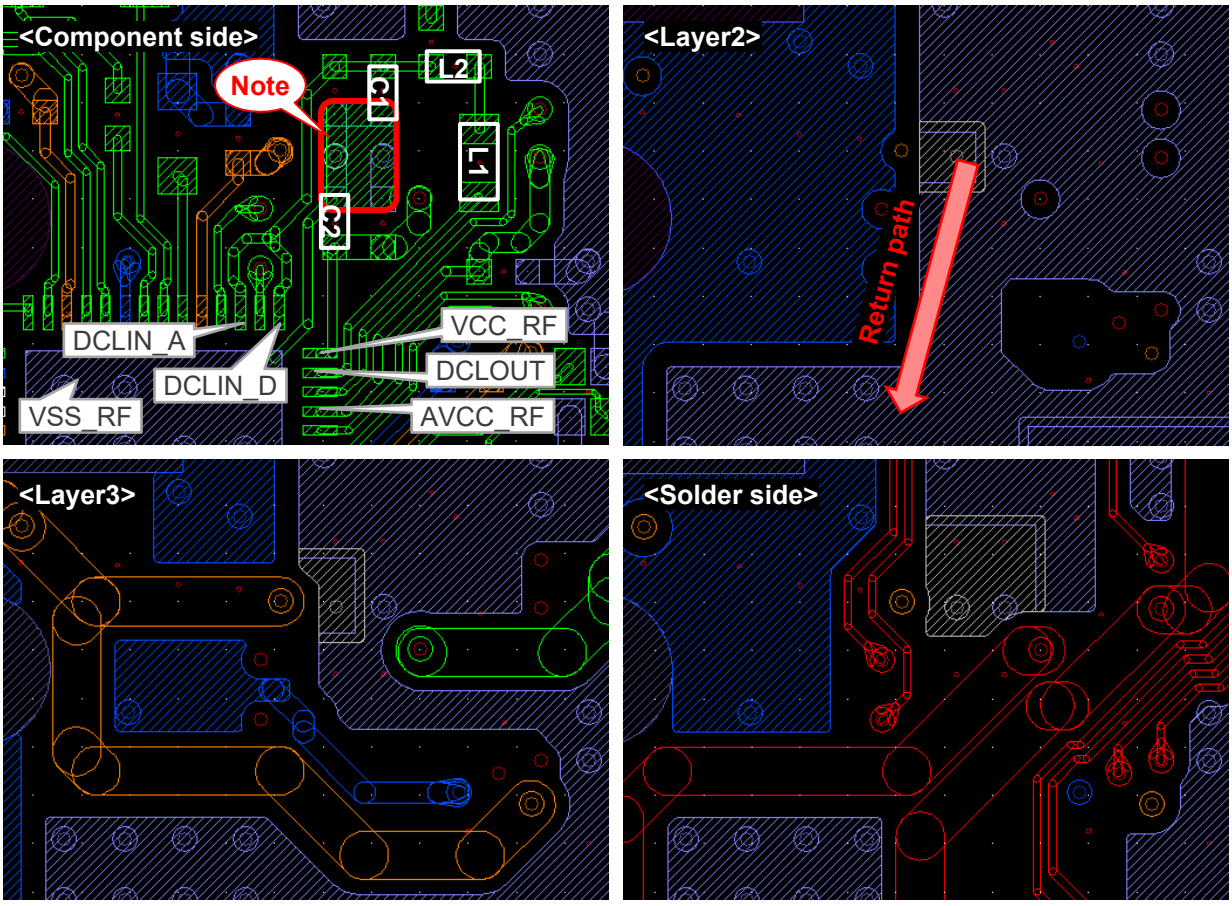
Figure 2-6 shows an example of the external circuits for the DC-DC converter mode, Figure 2-7 shows an example of the pattern around power supply line for the DC-DC converter mode.

- Make the signal pattern from the “DCLOUT” pin to the “VSS_RF” through the inductor “L1” and the capacitor “C1” shorter and wider to reduce impedance as possible. Place ground pattern in the area which is enclosed with the line connecting the “DCLOUT” and the “DCLIN_A”, as shown in Figure 2-7. In addition, connect the capacitor “C1” and the “VSS_RF” to this ground pattern.
- Connect the line connecting the “DCLOUT” pin and the “DCLIN_A” pin on the component side of the board without any Via.
- Reduce loop area which is enclosed with the line connecting the “DCLOUT” pin and the “DCLIN_A” pin as possible.
- Placing the inductor “L1”, “L2” and the capacitor “C1” as close as possible to the “DCLOUT” pin is recommended.
- Do not place any SMD component except the external circuits for the DC-DC converter mode, on the loop which is enclosed with line connecting the “DCLOUT” pin and the “DCLIN_A” pin.
- Ensure the return path in layer-2, and layer-3 if possible, from the ground in the loop to the "Exposed Die Pad (VSS_RF)”, as shown in Figure 2-7.
- Recommended electrical characteristics of the “L1” are the followings:
  - Inductance = 10 µH +/– 20%
  - Rated current ≥ 90 mA
  - DC resistance ≤ 1.0 ohm
  - Self-resonate frequency ≥ 30 MHz
  - Good DC superimposing characteristic
- The capacitance “C1” should be less than or equal to 2.2 µF +/– 20 %
- Do not place other analog signal, power, and ground lines than the external circuit for the DC-DC converter mode, on and below the circuit area.
- With mounting the inductor “L2”, noise caused by the DC-DC converter can be reduced. Therefore, it is recommended to prepare a mount space of the “L2” on a board pattern.



Note: L1: 10 µH, MLZ1608M100WT000
L2: SHORT (reserved inductor)
C1: 2.2 µF, GRM155R61A225KE95
C2: 2.2 µF, GRM155R61A225KE95

Figure 2-6. Example of the external circuit for the DC-DC converter mode



Note: Ground pattern in the loop which is enclosed with line connecting “DCLOUT” and “DCLIN_A”.

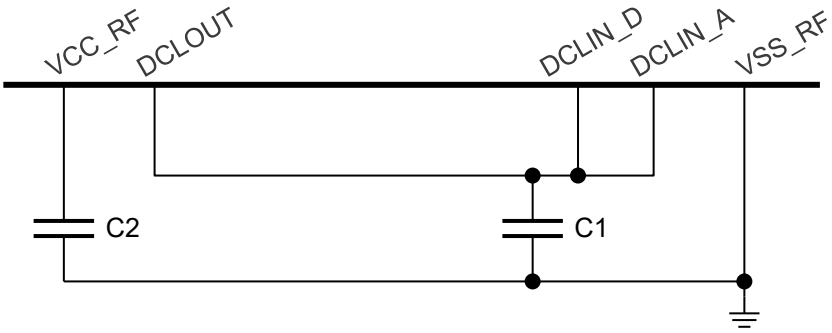
Figure 2-7. Example of the pattern for the DC-DC converter mode

2.4.2 Linear regulator mode

Note the followings for an external circuit design of the linear regulator mode.

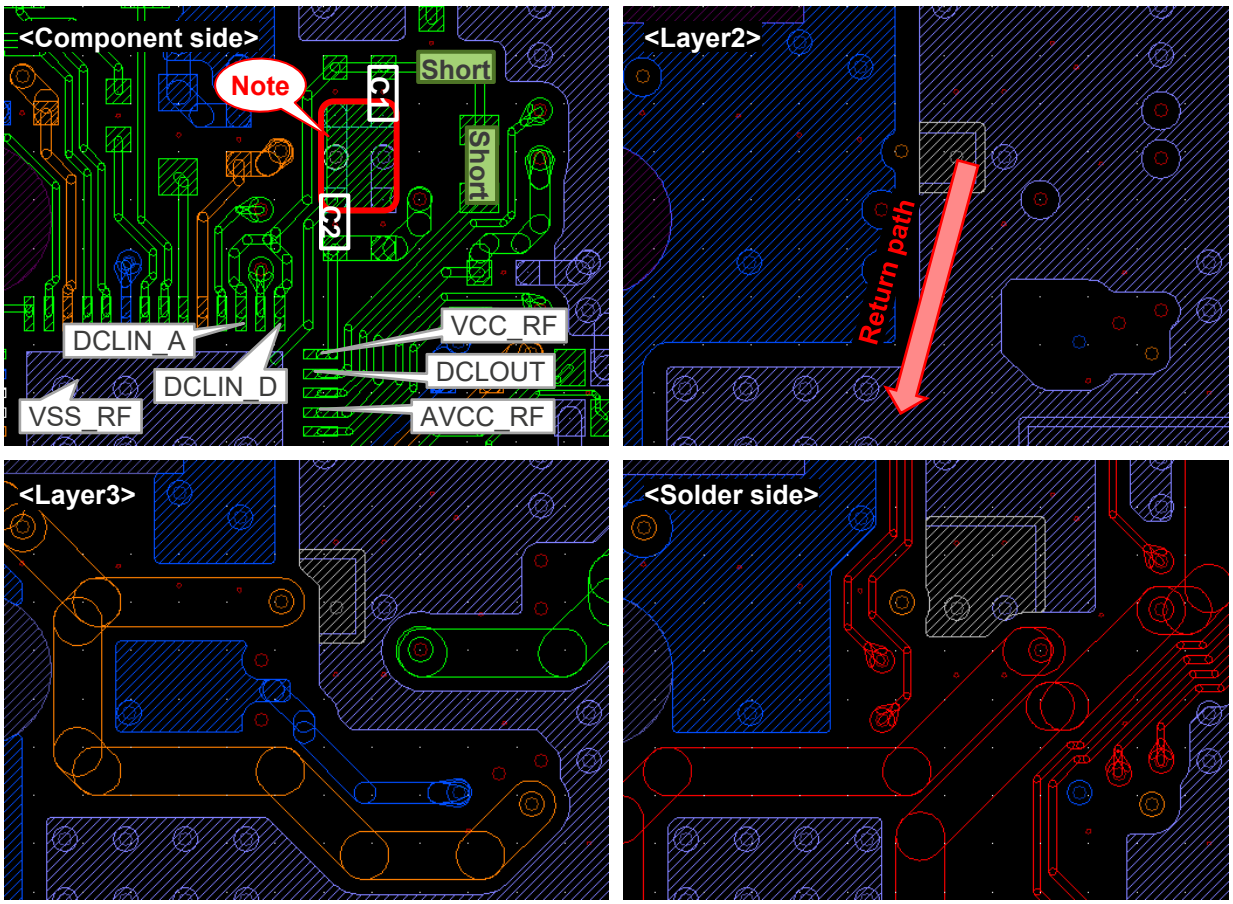
Figure 2-8 shows an example of the external circuits for the linear regulator mode, Figure 2-9 shows an example of the pattern around power supply line for the linear regulator mode.

- Make the signal pattern from the “DCLOUT” pin to the “VSS_RF” through the capacitance “C1” shorter and wider to reduce impedance as possible. Place ground pattern in the area which is enclosed with line connecting the “DCLOUT” pin and the “DCLIN_A” pin, as shown in Figure 2-9. In addition, connect the capacitor “C1” and the “VSS_RF” to this ground pattern.
- Connect the line connecting the “DCLOUT” pin and the “DCLIN_A” pin on the component side of the board through without any Via.
- Reduce loop area which is enclosed with line connecting the “DCLOUT” pin and the “DCLIN_A” pin as possible.
- Do not place any SMD component except the external circuit for the linear regulator mode, on the loop which is enclosed with line connecting the “DCLOUT” pin and the “DCLIN_A” pin.
- Ensure the return path in layer-2, and the layer-3 if possible, from ground in the loop to "Exposed Die Pad (VSS_RF)”, as shown in Figure 2-9.
- Do not place other analog signal, power, and ground lines than the external circuit for the linear regulator, on and below the circuit area.
- The capacitance “C1” should be less than or equal to 0.47 µF +/– 20 %.



Note: C1: 0.47 µF, GRM155B30J474KE18
C2: 2.2 µF, GRM155R61A225KE95

Figure 2-8. Example of the external circuit for the linear regulator mode



Note: Ground pattern in the loop which is enclosed with line connecting “DCLOUT” and “DCLIN_A”.

Figure 2-9. Example of the pattern for the linear regulator mode

2.5 Power supply and ground patterns

Note the followings for power supply patterns and ground patterns design.

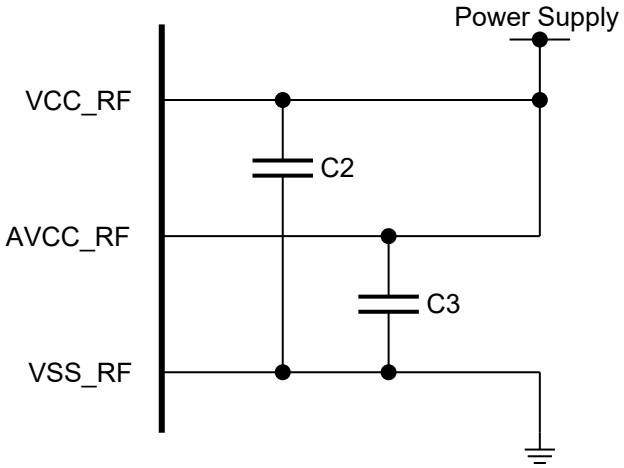
Figure **2-10** shows an example of how to place the bypass capacitors. Figure 2-11 shows an example of the ground pattern.

2.5.1 Power supply

- The power supply lines of the “AVCC_RF” pin and the “VDD_RF” pin should have low impedance and be located as far as possible from other power supply or signal lines to avoid noise couplings.
- The power supply lines of the “AVCC_RF” pin, the “VDD_RF” pin and other power lines (e.g. “VCC”) should be connected with lower common impedance as possible. For example, the “AVCC_RF” line, the “VDD_RF” line and other power line are connected at a certain point and are supplied from the same power source. After the connection point, each power line is isolated and connected to each pin of the RF transceiver.
- Each power line bypass capacitor should be located closed to the RF transceiver power supply pins. In addition, do not place any Via in the line between the bypass capacitor and the RF transceiver power supply pins.

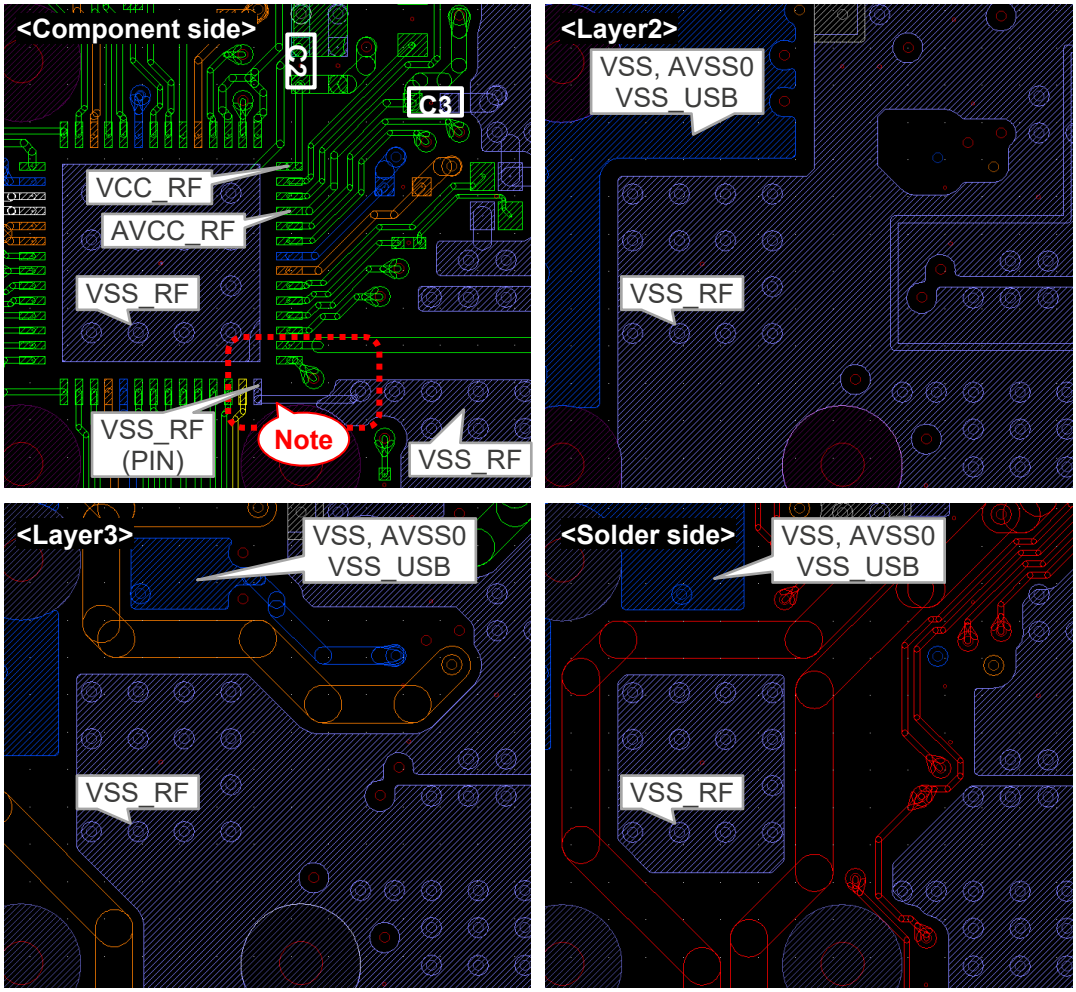
2.5.2 Ground

- The ground pattern should be placed on as much area of the board as possible.
- The ground pattern of the “VSS_RF” should have low impedance and be located as far as possible from other noisy ground patterns (e.g. USB ground) or noisy signal lines to avoid noise couplings.
- When using the ground pattern as a shield line, keep the shield pattern as far away from the oscillation and digital circuit grounds as possible to avoid noise couplings into the shielded signal from shield itself.
- The “Exposed Die Pad” is the reference ground for the RF transceiver. The reference ground should not be split and should not be with other signals, power lines or ground patterns.
- The below layer of the chip should be solid ground. The ground pattern of the “VSS_RF” should have low impedance, and it is recommended to place Vias as shown in Figure 2-11.
- When the ground pattern is connected to the upper and/or lower layers of the same potential, as many Vias as possible should be placed to reduce the impedance between each layer.
- The reference ground the “VSS_RF” and other grounds (e.g. “VSS”) are connected at a certain single point.
- Separate the “VSS_RF(PIN)” and the "Exposed Die Pad (VSS_RF)” on the component side of the board.



Note: C2: 2.2 µF, GRM155R61A225KE95
C3: 0.1 µF, GRM155R61E104KA87D

Figure 2-10. **Example of the bypass capacitors connection**



Note: Separate the ground area for "VSS_RF (Exposed Die Pad)" and "VSS_RF (PIN)" on the component side of the board.

Figure 2-11. Example of the ground pattern

2.6 Circuit diagram for reference

Figure 2-12 shows a reference circuit diagram in which the 2.4 GHz transceiver related part is only described.

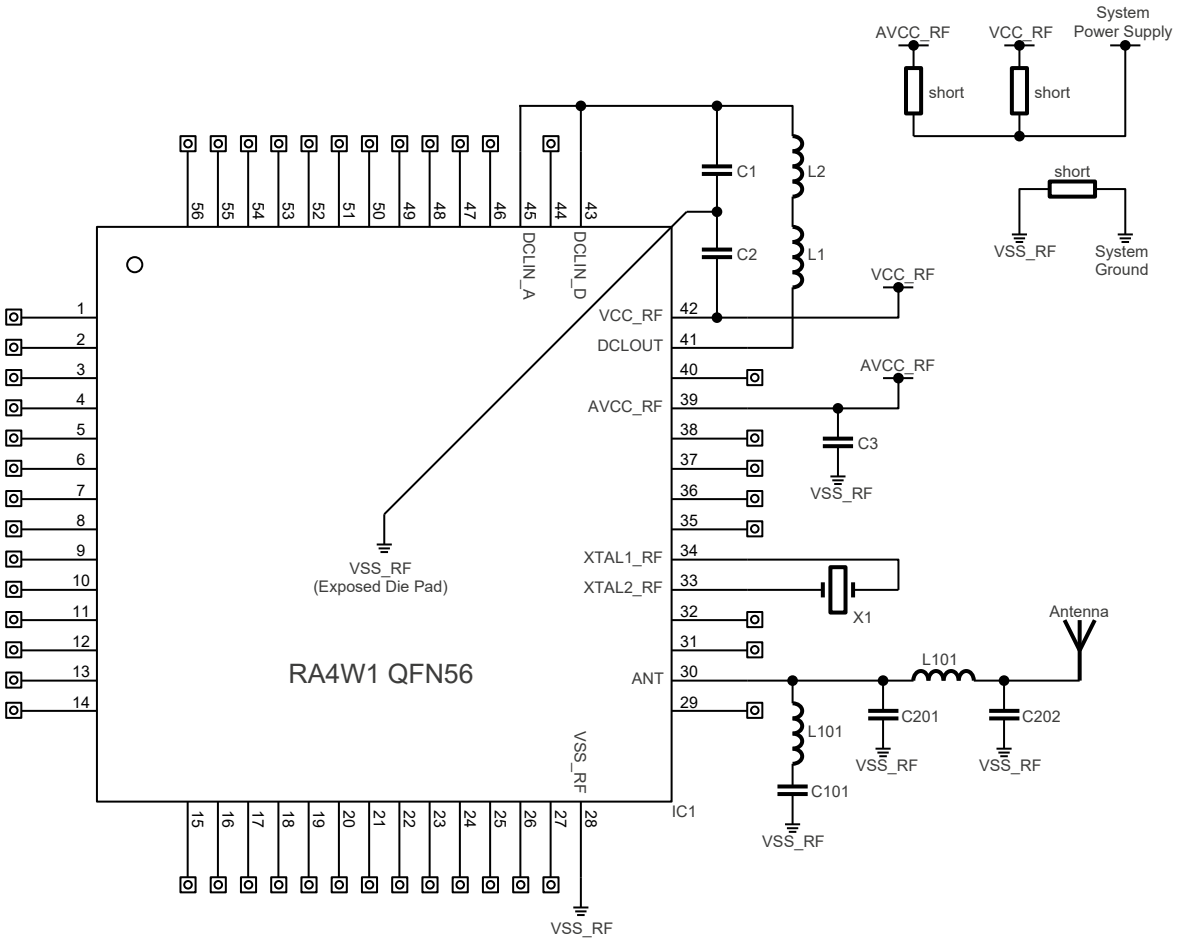


Figure 2-12. Circuit diagram (for reference)

2.7 Parts list for reference

Table 2-4 lists the parts.

Table 2-4. Parts list (for reference)

No.	Parts Reference	Pars number	Size code In mm	Value	Note
1	IC1	RA4W1 QFN chip	-	-	-
2	X1	NX1612SA-32.000MHZ-CHP-CIS-3	1612	32.00 MHz	-
3	L1	MLZ1608M100WT000	1608	10 µH	1
		(Short pattern)	-	―	2
4	L2	LQG15HS4N7S02	1005	4.7 nH	1
		(Short pattern)	-	―	2
5	C1	GRM155R61A225KE95 (*1)	1005	2.2 µF	1
		GRM155B30J474KE18(*2)	1005	0.47 µF	2
6	C2	GRM155R61A225KE95	1005	2.2 µF	-
7	C3	GRM155R61E104KA87D	1005	0.1 µF	-
8	L101	LQG15HS7N5J02	1005	7.5 nH	3
		(Open pattern)	-	-	4
9	C101	GRM1554C1HR50BA01	1005	0.5 pF	3
		(Open pattern)	-	-	4
10	L201	MLG1005S1N1ST000	1005	1.1 nH	
11	C201	GJM1554C1HR80BB01	1005	0.8 pF	
12	C202	GJM1554C1HR30BB01	1005	0.3 pF	

Notes: 1. DC-DC converter mode.
2. Liner regulator mode
3. Pi and LC Notch filter configuration
4. Pi filter configuration

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May.07.20	-	First edition issued
-	-	-	-

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

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