R-Car V4H Series SoC

Using the RAA271005, RAA271010, RAA271011, RAA271040, and RAA271041 Power-Supply ICs

Introduction

This document includes examples of circuits and layouts and provides guidelines for designing the power-supply circuits for the R-Car V4H Series System-on-Chip (SoC) products by using the RAA271005, RAA271010, RAA271011, RAA271040, and RAA271041 power-supply ICs to implement standard control operations such as power sequencing, CPU boot-up, and system shutdown.

The Renesas R-Car SoCs adapt to different application scenarios with varying feature sets. The R-Car V4H Series SoC is designed for applications requiring higher performance such as in-vehicle infotainment systems, digital cockpit solutions, and advanced driver-assistance systems (ADAS).

Contact Renesas Electronics regarding the specifications of the RAA271005, RAA271010, RAA271011, and RAA271041. Also, Renesas recommends referring to the SoC-related documents and the design guidelines for other devices in use and referring to the manual, *R-Car V4H Series User's Manual: Hardware*.

Target SoCs

- R-Car V4H Series

Note: The R-Car series products in this document are referred to as SoCs.

Target Power-Supply ICs

- RAA271040 – Primary Regulator, Dual Buck Regulator output
- RAA271041 – Primary Regulator, Pre-Boost + Buck Regulator output
- RAA271005 – PMIC for 4th Generation R-Car SoCs
- RAA271010 – Multi-phase Synchronous Buck Controller for RAA271011
- RAA271011 – Smart Power Stage works with RAA271010, (15A continuous)

Currents at T_J = 125°C, TYP DC Operating Voltage, 100% Utilization			**System PMIC RAA271005 OTP Number**	**VDD Rail RAA271010 OTP Number (based on VDD Rail Load Current Profile)**		**Primary Regulator OTP Number**	
SoC	VDD	VDD_OD	-	2-Phase	1-Phase	RAA271041	RAA271040
V4H-7	23.6A	4.3A	05.61	0D.00	5.06	7	3
V4H-5	22.1A	4.0A	05.61	0D.00	5.06	7	3
V4H-3	21.8A	3.4A	05.61	0D.00	5.06	7	3

References

- *V4H Whitehawk Hardware Manual*
- *RAA271005 Datasheet*
- *RAA271005 Safety Application Note*
- *RAA271005 Safety Requirement Specification*
- *RAA271010 Datasheet*
- *RAA271011 Datasheet*
- *RAA271040 Datasheet*
- *RAA271041 Datasheet*

Contents

1. V4H R-Car SoC

The V4H R-Car System-on-Chip (SoC) is an adaptable platform designed explicitly for automotive applications, tailored to the demands of modern vehicles. The V4H SoC has both CPU and GPU cores, providing the computational strength necessary for executing sophisticated automotive tasks such as powering infotainment systems, navigation functionalities, and driver assistance features. Integrated graphics processing units (GPUs) empower the V4H SoC to support high-resolution displays and intricate graphical interfaces, lending themselves seamlessly to in-car entertainment systems and digital instrument clusters.

The V4H SoC has dedicated multimedia processing units capable of managing audio and video playback, enabling support for diverse multimedia formats and ensures all the graphics and animations on your car's screen look sharp and clear.

Renesas recognizes the important role of connectivity in modern automotive ecosystems, the V4H SoC extends its skill by being compatible with a wide array of communication protocols, including CAN, Ethernet, and LIN, facilitating seamless integration and communication across various vehicle systems and external peripherals.

Renesas' commitment to safety and security, the V4H SoC integrates advanced features such as hardware-based encryption, secure boot processes, and trusted execution environments, strengthening its defenses against cyber threats and unauthorized access. V4H's scalability and flexibility empower automotive manufacturers to tailor and optimize the platform to meet specific requirements and use cases, ensuring compatibility across vehicle models and configurations.

The V4H SoC maintains a steadfast focus on energy efficiency, meticulously optimizing power consumption to augment battery life in electric and hybrid vehicles while concurrently curbing overall operating costs. In essence, the V4H R-Car SoC emerges as an encompassing solution for automotive computing, seamlessly amalgamating high performance, advanced graphics and multimedia functionalities, robust connectivity options, and stringent safety and security features to address the dynamic needs of contemporary vehicles.

2. Power-Supply Specifications

The V4H R-Car power supply system comprises a primary power supply block tasked with stepping down the voltage from the car battery to feed into the secondary power supply block, which generates secondary power-supply voltages typically from a 5V input. Additionally, it encompasses power supplies tailored for peripheral circuits, offering diverse options to accommodate the system configuration and requirements.

For this application, the primary power source can be sourced from the RAA271040, an IC that has a wide input voltage range from 4V to 42V to ensure stabilization of the output voltage in cold crank conditions.

2.1 RAA271005 Features

- Input Voltage Range 2.7V to 5.5V
- 5 High Efficiency Switching Regulators with adjustable output voltages
  - 12A (Buck 1); V_{OUT} from 0.3V to 3.3V
  - 2.5A (Buck 2); V_{OUT} from 0.3V to 3.3V
  - 2.5A (Buck 3-5); V_{OUT} from 0.5V to 3.3V
  - Merge-mode 2 x 2.5A regulators = 5A
  - Buck 5 can operate as asynchronous boost up to 5.0V V_{OUT}
- 6 Linear Drop Out (LDO) Regulators
  - 4 × 75mA; V_{OUT} = 1.8V or 3.3V
  - 2 × 500mA; V_{OUT} = Factory Programmable
- 12-bit Analog-to-Digital converter for monitoring with programmable OV/UV thresholds
- Programmable power sequence, fully 4th Generation R-Car SoC sequence requirements
- Low-I_Q Deep-stop / Always On (AWO) Mode
- Suspend-to-RAM / DDR-backup Mode
- Supports R-Car SoC Activation
- Q&A Watchdog Timer
- Configurable through I^2C or SPI interface

2.2 RAA271010 Features

- Programmable 4-, 3-, 2-, 1-Phase Buck controller
- Higher than 90% efficiency (with RAA271011 power stages)
- Fast ramping of current from microprocessor idle to full current
- Up to 100mV/µs dynamic voltage scaling
- 0.5% voltage regulation accuracy
- On-chip temperature monitoring system
- MPIO/GPIO digital interface
- Fast Dynamic Voltage Scaling through I^2C/SPI bus or physical pin control

2.3 RAA271011 Features

- Delivers up to 10A of continuous current and 15A of peak current
- High-power density and high efficiency
- High-switching frequency operation up to 4MHz
- V_{IN} operating range: 2.5V to 5.5V
- Three-state PWM logic
- Integrated bootstrap switch
- Optimized dead time control
- Comprehensive protection features, UVLO, OCP, and OT
- Built-in current sensing for current balance

2.4 RAA271040 Features

- ASIL-D
- V_{IN} operating range: 3.75V to 42V
- Low quiescent current: 6µA typical, one channel
- Switching frequency: 440kHz or 2.2MHz, selectable ±10% around these settings
- Dropout mode for high duty-cycle operation
- Minimized FET ON and OFF times (25ns and 50ns)
- External synchronization using the SYNC pin
- Optional pseudo-random spread spectrum clocking
- Dual over-temperature protection monitors
- Integrated MOSFET drivers for both channels
- Protection mechanisms for OV/UV/OC/OT

2.5 RAA271041 Features

- ASIL-D
- 40V boost and buck integrated controller + driver
- FET drivers support source current of 2A and sink current of 3A
- Low quiescent current: 6µA typical (Buck 1 only)
- Separate or combined wake (Enable) inputs for each channel
- Minimized FET ON and OFF times (25ns and 50ns)
- Optional pseudo-random spread spectrum clocking
- High-efficiency buck exceeding 80% at 10mA
- Buck frequency options 400kHz or 2.2MHz
- Boost frequency options 400kHz or 2.2MHz (2.2MHz requires buck frequency at 2.2MHz)
- VBATS sense for boost enable during cold crank
- Boost Bypass mode (for Buck in CCM)
- External synchronization using the SYNC pin
- Dual over-temperature protection monitors

3. V4H Power System Block Diagram

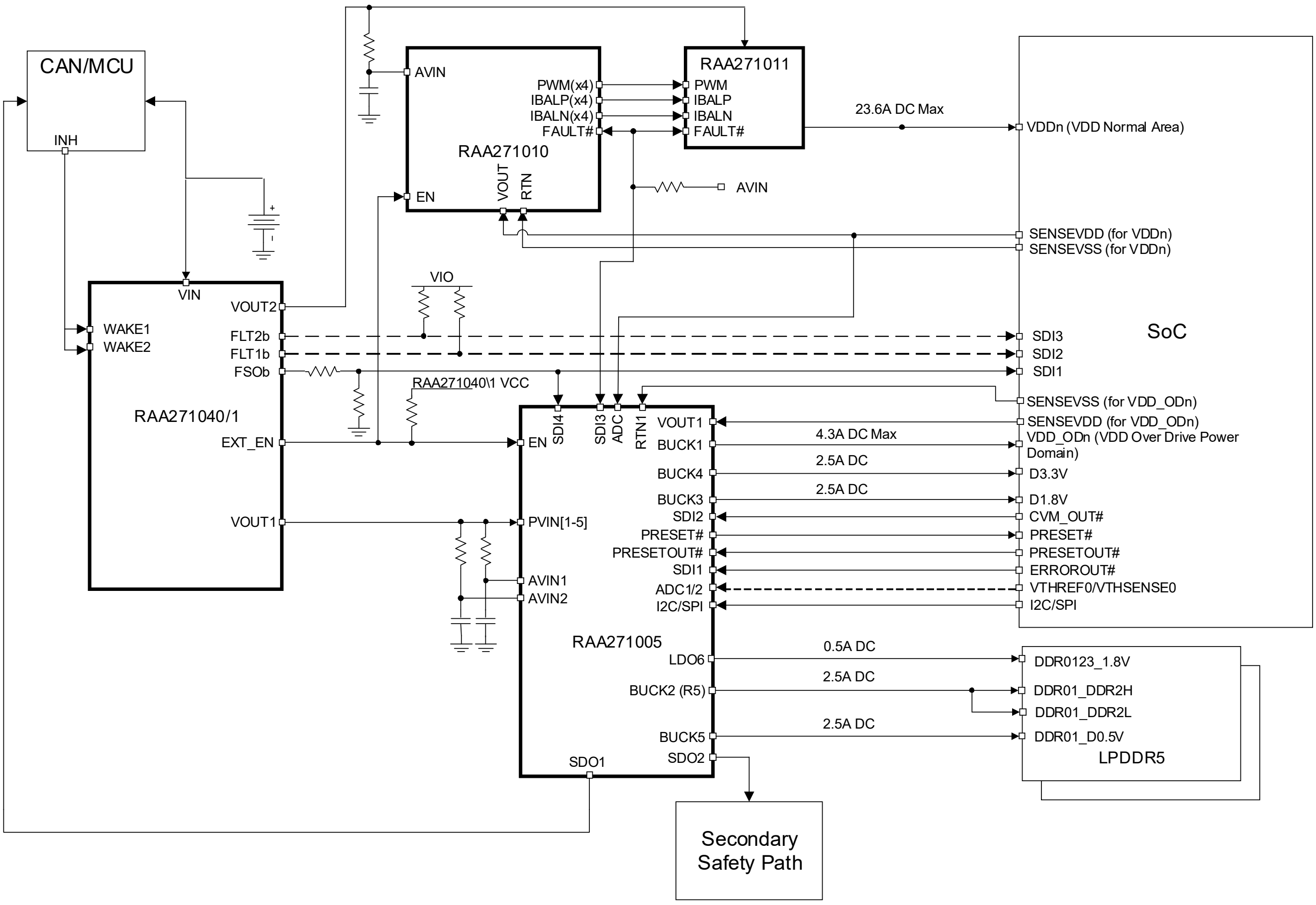


Figure 1. V4H System Block Diagram

3.1 Recommended System Use Case

For the RAA271005 assumed use case (see Figure 1), an ASIL D Pre-buck (RAA271040/1) provides safe power supply to the RAA271005 VINs (Regulation input (AVIN1), Protection input (AVIN2), and the Power Stage inputs (PVINs). RAA271005 collects fault information detected by internal SMs of the following components through an SDI pin:

- RAA271040/1 (FSOb)
- R-CAR SoC (ERROROUT* and VMONOUT*)

The RAA271005 offers versatile configuration options to enhance system control and safety. It can be tailored to respond to individual SDIs, transitioning the PMIC to either RESET or ERROR states, and it supports control of a secondary safety path signal on receiving an SDI. Additionally, the RAA271005 facilitates control of a CAN transceiver Inhibit pin to disable the pre-buck function. Its PWR_CTRL* pins enable efficient power domain management. Furthermore, the RAA271005 allocates two external ADC channels for testing the SoC CVM functionality.

3.2 RAA271005 Configuration

The RAA271005 contains five DC/DC switching regulators and six low-drop out linear regulators (LDO). The DCDC5 (Buck 5) switching regulator can be configured to work in buck mode or can be configured as a boost. The RAA271005 PMIC supports low power operation where three of the switching regulators (Buck 3-5) are optimized to consume low quiescent current.

RAA271005 supports up to ASIL D functional safety and includes an independent reference for monitoring of the output voltages, dual internal temperature monitors, challenge response watchdog timer, SoC and MCU error pin monitors, reset generator, a dedicated safety-control state machine, and a safety shutdown path. An integrated 12-bit ADC monitors all input rails, output rails, internal temperature, and includes additional inputs to monitor external analog sources.

For Buck 1 and Buck 2, the frequency of each buck can be set to hysteretic (varying frequency), fixed frequency, or fixed frequency + pseudo-random spread spectrum frequency. From these three options, hysteretic mode offers the best transient performance, and it is the default mode set in OTP.

Buck 3, Buck 4, and Buck 5 are peak current mode control regulators, which the peak of the inductor current is controlled cycle-by-cycle, allowing for current limiting against overcurrent conditions without an additional control loop. Buck 3-5 are the low I_Q bucks that offer the lowest quiescent current when operating in PFM mode at light load.

3.3 OTP Creator Guide

The RAA271005 OTP Creator allows the user to view and select OTP settings designed for their specific platform. This section reviews each group of selectable options with an explanation of the feature. The RAA271005 OTP creator is separated by four tabs (see Figure 2).

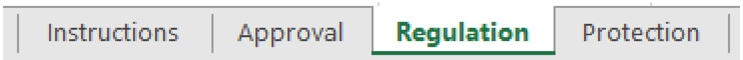


Figure 2. RAA271005 OTP Creator Tab

3.3.1 Instructions Tab

The Instruction tab provides guidelines for the OTP creator along with a timing diagram of the startup and shutdown delay. Review the Instructions tab before proceeding. This application note details the selectable options. The following are useful instructions:

- Only yellow cells are allowed to be modified.
- If the cell has a dropdown menu, only use the selectable options in the dropdown menu.
- Do not copy and paste cells because that could change the formula in the cell.
- Cells that are highlighted red can mean an issue with the selected setup. Review the highlighted red cells with a representative from Renesas.

3.3.2 Approval Tab

After each party has agreed on the OTP setting, the Approval tab is used to sign off and finalize the settings. An OTP version ID is provided by Renesas to be used for sample requests. If additional changes to the OTP setting are required, a new OTP version ID is assigned, and the approval process is repeated. Figure 3 charts the flow of the OTP creator, approval, and verification process.

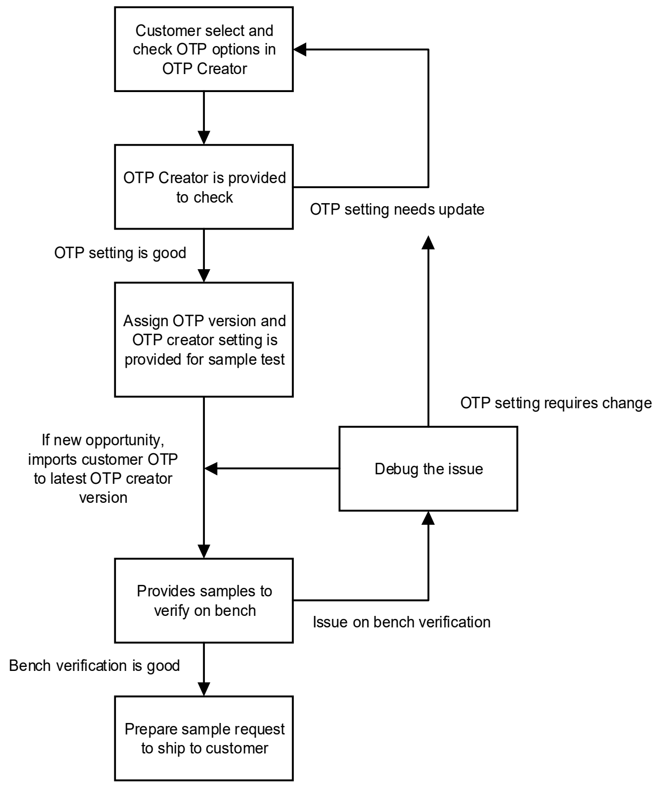


Figure 3. OTP Creator Flow Chart

3.3.3 Regulation Tab

In the Regulation tab, required settings can be selected such as output voltages, sequencing, fault reactions, IO pin settings, and pin mode.

3.3.3.1 Target Application (SoC)

Depending on the application, the OTP setting of each regulator can differ. Select the appropriate application on cell E3. The following the selectable options:

- S4 – When S4 is selected, Buck3 is configured in PFM.
- V4H – When VH4 is selected, all rails are in CCM and no power grouping should be required.
- V4M – When V4M is selected, all rails are in CCM and no power grouping should be required.
- Generic – When generic is selected, no additional setting is applied to the regulators.

3.3.3.2 Output Voltage Selection

A voltage range can be set for each regulator. If the regulator is not used, set the voltage value to 0, and set "Startup with EN?" to False in column O.

Table 1. Output Voltage Range

Regulator	Voltage Range	Additional Note
Buck1	0.3V to 3.3V	-
Buck2	0.3V to 3.3V	-
Buck3	0.5V to 3.3V	-
Buck4	0.5V to 3.3V	-
Buck5	0.5V to 3.3V	-
LDO1	1.8V to 3.3V	UV monitoring only available for 1.8V and 3.3V
LDO2	1.8V to 3.3V	UV monitoring only available for 1.8V and 3.3V
LDO3	1.8V to 3.3V	UV monitoring only available for 1.8V and 3.3V
LDO4	1.8V to 3.3V	UV monitoring only available for 1.8V and 3.3V
LDO5	0.6V to 3.3V	-
LDO6	0.6V to 3.3V	-

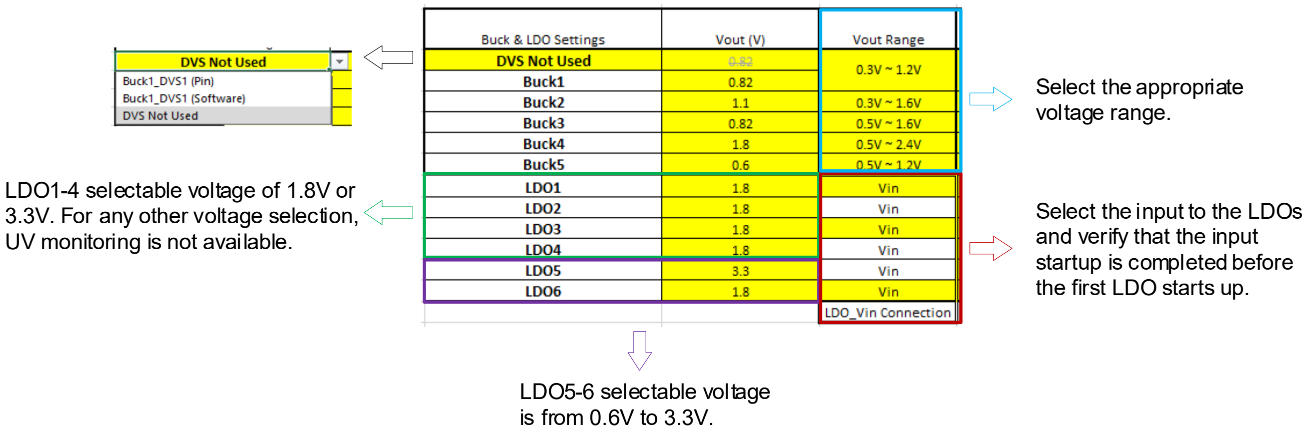


Figure 4. Output Voltage Selection

The VIO voltage must be selected based on the schematic. *Note*: If one of the PMIC regulators is used for the VIO voltage, the selected regulator must be in the Always ON power state. Figure 5 shows the VIO voltage selection.

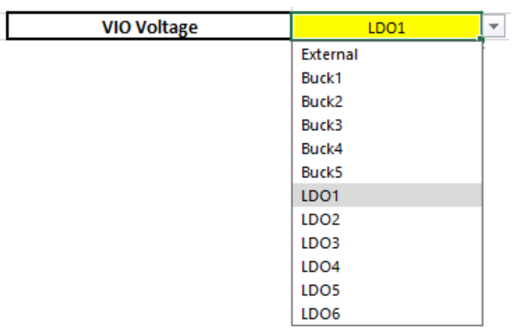


Figure 5. VIO Voltage

3.3.3.3 Timing Sequence and Power State

For each regulator output, the startup delay and shutdown delay are programmable. Each regulator can be set to a different power state (Always ON, PWRCTRL1, PWRCTRL2, and SW Shutdown Group. *Note*: The Always ON group does not have selection for Suspend to RAM because it is always enabled.

The Startup and Shutdown Delay can be set from 0 to 63.75ms in increments of 0.25ms.

Startup Delay (ms)	Shutdown Delay (ms)	Power State	Used with Suspend to RAM?
3	10	ALWAYS ON GROUP	~~FALSE~~
4	5	ALWAYS ON GROUP	~~FALSE~~
6	2	ALWAYS ON GROUP	~~FALSE~~
2	15	ALWAYS ON GROUP	~~FALSE~~
5	0	ALWAYS ON GROUP	~~FALSE~~
0	21	ALWAYS ON GROUP	~~FALSE~~
1	1	ALWAYS ON GROUP	~~FALSE~~
0	7	ALWAYS ON GROUP	~~FALSE~~
0	7	ALWAYS ON GROUP	~~FALSE~~
0	7	ALWAYS ON GROUP	~~FALSE~~
2	15	ALWAYS ON GROUP	~~FALSE~~
		SW_BKUP	FALSE

PWRCTRL1, PWRCTRL2, and SW SHDN group have the option for Suspend to RAM.

When SW_BKUP is set to True, a rail that remains on during SW_BKUP must have a power state set to PWRCTRL1 and Suspend to RAM set to True.

Figure 6. Sequence and Power State Selection

3.3.3.4 Fault Reactions

For fault reactions, the PMIC has the option to configure how it reacts to overvoltage, undervoltage, positive current limit, negative current limit, and regulation thermal shutdown. See Figure 7 for the dropdown menu options.

Dropdown: Shut down this regulator
- Do nothing
- Shut down this regulator
- Shut down groups
- Shut down all regulators

Fault Reactions					
Over Voltage	Under Voltage	High-Side Pos Current Limit	Low-Side Pos Current limit	Negative Current Limit	Regulation Thermal Shutdown Reaction
Shut down this regulator	Shut down this regulator	Shut down this regulator	Do nothing	Shut down this regulator	Shut down this regulator
Shut down this regulator	Shut down this regulator	Shut down this regulator	Do nothing	Shut down this regulator	Shut down this regulator
Shut down this regulator	Shut down this regulator	Shut down this regulator	Do nothing	Shut down this regulator	Shut down this regulator
Shut down this regulator	Shut down this regulator	Shut down this regulator	Do nothing	Shut down this regulator	Shut down this regulator
Shut down this regulator	Shut down this regulator	Shut down this regulator	Do nothing	Shut down this regulator	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator

The overall fault reaction might be different based on protection block interactions

Figure 7. Fault Reaction Selection

Note: The Low-Side Positive Current Limit for Buck1 is not available and is set to "Do Nothing".

3.3.3.5 Pin Mode and IO Settings

The RAA271005 have two pin mode option, Pinmode 0 and Pinmode 1:

- In Pinmode 0, the SPI communication is used forcing the set of IO3, IO4, and IO5 to SS_B, MOSI and MISO, respectively. These three IO pins cannot be used as a generic GPIO in this mode (see Figure 9).
- In Pinmode 1, I^2C communication is used allowing IO3, IO4, and IO5 to be used as a generic GPIO (see Figure 9).

IO Pin Settings

	IO3	IO4	IO5	IO6	IO13	IO14	IO19
Direction	~~Input~~	~~Input~~	~~Input~~	Output	Output	Output	Output
Invert?	~~FALSE~~	~~FALSE~~	~~FALSE~~	FALSE	FALSE	TRUE	FALSE
Output Open Drain?	~~FALSE~~	~~FALSE~~	~~FALSE~~	FALSE	FALSE	FALSE	FALSE
Function*	SS_B	MOSI	MISO	PGOOD_GLB	PGOOD_ALWON	Global Interrupt	BKUP signal
Assert Delay (ms)	~~N/A~~	~~0~~	~~0~~	1	0.25	N/A	N/A
De-assert Delay (ms)	~~N/A~~	~~0~~	~~0~~	0	0	N/A	N/A

Pinmode	0

Figure 8. IO Pin Setting for Pinmode 0

IO Pin Settings							
	IO3	IO4	IO5	IO6	IO13	IO14	IO19
Direction	Input	Input	Input	Output	Output	Output	Output
Invert?	FALSE	FALSE	FALSE	FALSE	FALSE	TRUE	FALSE
Output Open Drain?	FALSE	FALSE	FALSE	FALSE	FALSE	FALSE	FALSE
Function*	Generic GPIO	Generic GPIO	Generic GPIO	PGOOD_GLB	PGOOD_ALWON	Global Interrupt	BKUP signal
Assert Delay (ms)	N/A	0	0	1	0.25	N/A	N/A
De-assert Delay (ms)	N/A	0	0	0	0	N/A	N/A
Pinmode	1						

Figure 9. IO Pin Setting for Pinmode 1

3.3.3.6 Buck and LDO Ramp Rate

Each regulator has configurable ramp rate options depending on the output voltage range.

- Refer to Table 2 for the Buck 1-5 ramp rate options based on the selected V_{OUT} range.
- Refer to Table 3 for the LDO 1-4 ramp rate options based on output voltage. LDO 1-4 output voltage from 1.8V to 1.89V uses Ramp Rate 1 while 1.9V - 3.3V uses Ramp Rate 2.
- Refer to Table 4 for the LDO 5-6 ramp rate options.

Table 2. Buck Startup Ramp Rate Options

V_{OUT} Range Setting	Ramp Selection	Ramp Rate (mV/µS)
Buck 1-2 (0.3V to 1.2V) Buck 3-5 (0.5V to 1.2V)	0	1.2
	1	3
	2	7.1
	3	14.2
	4	6
	5	12
Buck 1-2 (0.3V to 1.6V) Buck 3-5 (0.5V to 1.6V)	0	1.6
	2	3.2
	4	6.3
	6	12.6
Buck 1-2 (0.3V to 2.4V) Buck 3-5 (0.5V to 2.4V)	0	1.2
	2	2.4
	4	6
	6	12
Buck 1-2 (0.3V to 3.3V) Buck 3-5 (0.5V to 3.3V)	0	1.5
	2	3
	4	7.4
	6	14.8

Table 3. LDO 1-4 Startup Ramp Rate Options

Options	Ramp Rate 1 (mV/µs)	Ramp Rate 2 (mV/µs)
0	8.56	15.68
1	4.28	7.84
2	2.14	3.92
3	1.07	1.96
4	0.53	0.98
5	0.27	0.49
6	0.13	0.25

Table 4. LDO 5-6 Startup Ramp Rate Options

Options	Ramp Rate (mV/µS)
0	15.4
1	7.7
2	3.9
3	2
4	1
5	0.5
6	0.2

3.3.3.7 Spread Spectrum

The spread spectrum setting is disabled by default. To enable spread spectrum, select a direction in cell T17. After a direction is selected, the Algorithm Type, Algorithm Length, and Amplitude option is available. *Note:* The regulator is required to be set to Fix Frequency to enable spread spectrum. Figure 10 shows the selection for the Direction option while Figure 11 shows the frequency setting.

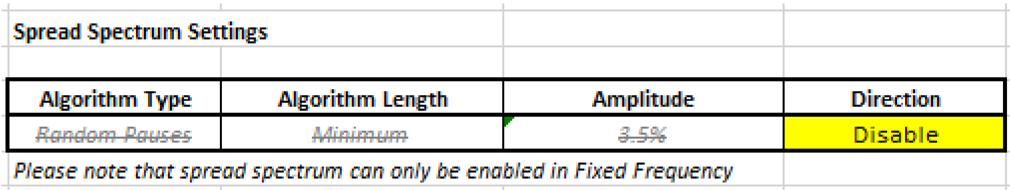


Figure 10. Spread Spectrum Selection

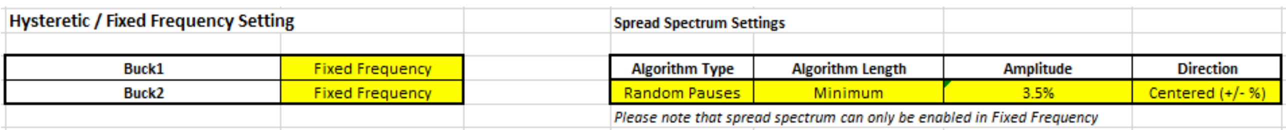


Figure 11. Frequency Setting After Spread Spectrum is Enabled

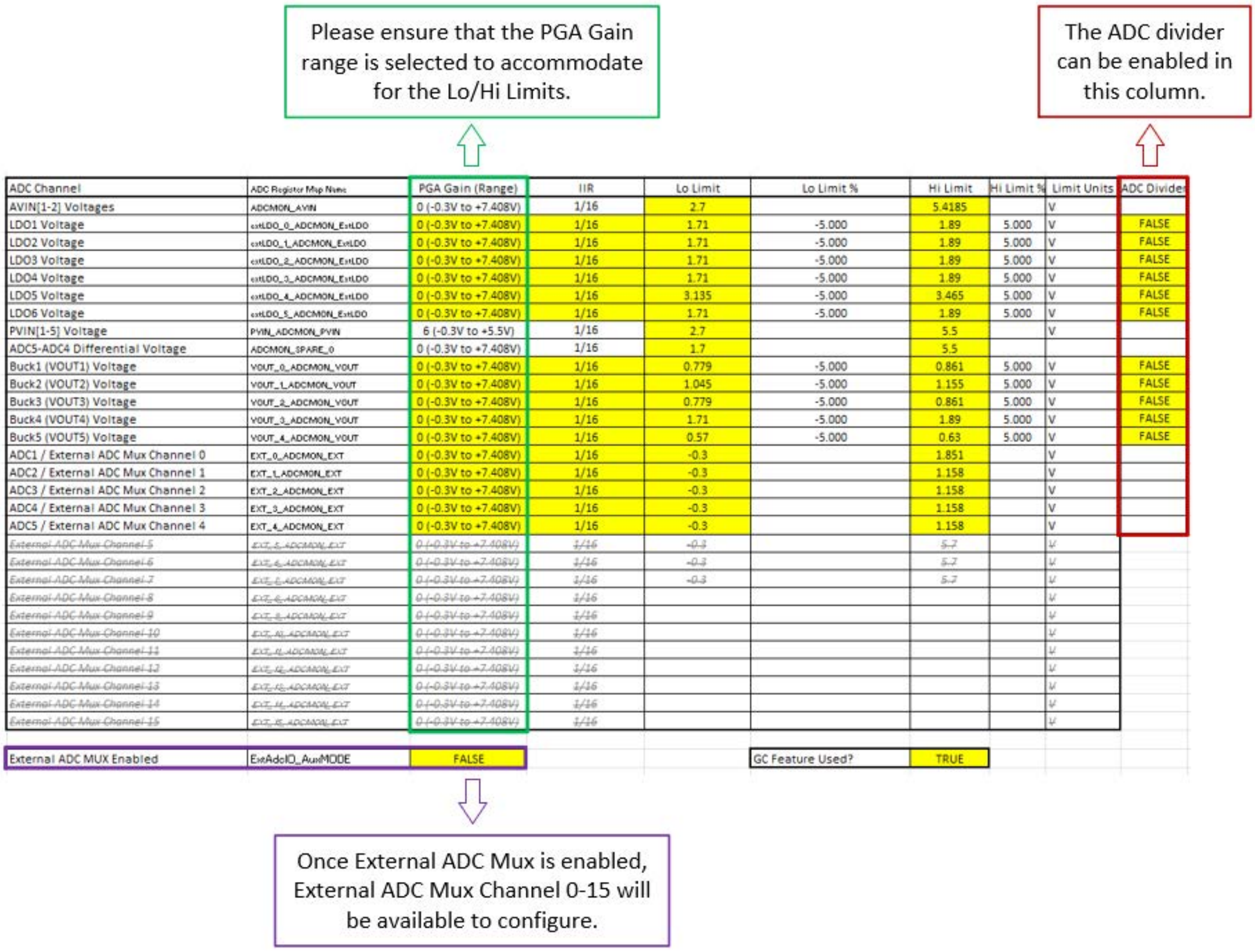
3.3.4 Protection Tab

3.3.4.1 ADC Channel Setting

In the ADC channel section, the LO and HI limits can be set for each regulator and ADC channel. There are eight PGA gain settings that set the voltage range of the input to the ADC. Table 5 shows the PGA gain options that can be independently set for each ADC channel.

Table 5. PGA Gain Options

Option Number	Input Voltage Range
0	-0.3V to +7.408V
1	-0.3V to +1.851V
2	-0.3V to +0.462V
3	-0.1V to +0.115V
4	-0.3V to +2.78V
5	-0.3V to +1.158V
6	-0.3V to +5.4V
7	-0.3V to +0.659V



ADC Channel	ADC Register Map Name	PGA Gain (Range)	IIR	Lo Limit	Lo Limit %	Hi Limit	Hi Limit %	Limit Units	ADC Divider
AVIN[1-2] Voltages	ADCMON_AVIN	0 (-0.3V to +7.408V)	1/16	2.7		5.4185		V	
LDO1 Voltage	extLDO_0_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
LDO2 Voltage	extLDO_1_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
LDO3 Voltage	extLDO_2_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
LDO4 Voltage	extLDO_3_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
LDO5 Voltage	extLDO_4_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	3.135	-5.000	3.465	5.000	V	FALSE
LDO6 Voltage	extLDO_5_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
PVIN[1-5] Voltage	PVIN_ADCMON_PVIN	6 (-0.3V to +5.5V)	1/16	2.7		5.5		V	
ADC5-ADC4 Differential Voltage	ADCMON_SPARE_0	0 (-0.3V to +7.408V)	1/16	1.7		5.5			
Buck1 (VOUT1) Voltage	VOUT_0_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	0.779	-5.000	0.861	5.000	V	FALSE
Buck2 (VOUT2) Voltage	VOUT_1_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	1.045	-5.000	1.155	5.000	V	FALSE
Buck3 (VOUT3) Voltage	VOUT_2_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	0.779	-5.000	0.861	5.000	V	FALSE
Buck4 (VOUT4) Voltage	VOUT_3_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
Buck5 (VOUT5) Voltage	VOUT_4_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	0.57	-5.000	0.63	5.000	V	FALSE
ADC1 / External ADC Mux Channel 0	EXT_0_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.851		V	
ADC2 / External ADC Mux Channel 1	EXT_1_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.158		V	
ADC3 / External ADC Mux Channel 2	EXT_2_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.158		V	
ADC4 / External ADC Mux Channel 3	EXT_3_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.158		V	
ADC5 / External ADC Mux Channel 4	EXT_4_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.158		V	
~~External ADC Mux Channel 5~~	~~EXT_5_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~	~~-0.3~~		~~5.7~~		~~V~~	
~~External ADC Mux Channel 6~~	~~EXT_6_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~	~~-0.3~~		~~5.7~~		~~V~~	
~~External ADC Mux Channel 7~~	~~EXT_7_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~	~~-0.3~~		~~5.7~~		~~V~~	
~~External ADC Mux Channel 8~~	~~EXT_8_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 9~~	~~EXT_9_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 10~~	~~EXT_10_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 11~~	~~EXT_11_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 12~~	~~EXT_12_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 13~~	~~EXT_13_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 14~~	~~EXT_14_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 15~~	~~EXT_15_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	

External ADC MUX Enabled	ExtAdcIO_AuxMODE	FALSE
GC Feature Used?	TRUE	

Figure 12. ADC Channel Setting

For applications where AVIN2 falls below a regulator programmed output voltage, the regulator ADC reading loses headroom because of the reduction in the ADC full scale range. To accurately monitor the regulator voltage, the ADC divider can be used to divide the ADC reading for that channel by half. For example, if LDO2 = 3.3V and AVIN2 drops to 3V, the ADC is not able to accurately display the 3V ADC reading of LDO2, but if the ADC divider setting is enabled, the ADC properly displays 1.5V.

3.3.4.2 Temperature Setting during Active and SOC Activation

The temperature sensor is monitored by the ADC and temperature thresholds can be set with a resolution of 0.25°C. Figure 13 shows the options for thermal warning and shutdown. *Note*: The following requirements:

- The Protection Thermal Warning (during Active) must be less than Protection Thermal Shutdown (during SoC activation).
- The Protection Thermal Shutdown (during Active) must be greater than Protection Thermal Shutdown (during SoC activation).

Temperature Setting During Active			
Protection Thermal Warning	ADCMON_WarnLimitLSB/MSB_Ter	90	°C
Protection Thermal Shutdown*	ADCMON_ShutDNLimitLSB/MSB_	150	°C
*Note: Both Temp sensor 2 & 4 are controlled by same cell			
Temperature Setting During SOC Activation			
Protection Thermal Shutdown	120	°C	

Figure 13. Protection Thermal Warning and Shutdown

3.3.4.3 IO Pin Safe State Setting

IO9 and IO10 pin can be configured to monitor the safe state the PMIC is in. Refer to the *Safety Application Note* for more information on each PMIC safe state.

	IO9/SDO1	IO12/SDO2	IO10/SSP
Start	Hi-Z	Hi-Z	Hi
Self Diagnostic	Hi-Z	Hi-Z	Hi-Z
SoC Activation	Hi-Z	Hi-Z	Hi
System Test (optional)	Hi	Hi	Hi
Active	Hi-Z	Hi-Z	Hi
Reset	Lo	Lo	Lo
Error	Lo	Lo	Lo
Lock	Lo	Lo	Lo
Debug Mode	**Hi**	**Hi**	**Hi**

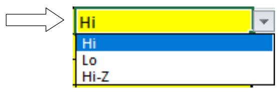


Figure 14. IO9 and IO10 Pin Safe State Setting

3.3.4.4 Watchdog

The Watchdog feature checks if the PMIC is alive and responds correctly during a predetermine pull in interval. This interval can be set using the dropdown menu in Figure 15.

Watchdog					
Watchdog Enable	WDT_WWDT_EN	TRUE			
Advance Mode Q&A Scheme	WDT_WWDT_ADV_16Q	16 QA	WDT Mode Selectior	WDT_VWDT_ADV_MC	Q&A
Watchdog Upper Limit (counts)	WDT_ULCNT	7			
Watchdog Lower Limit (counts)	WDT_LLCNT	4			
Watchdog Upper Limit (unit, s)	WDT_ULTICK	1m			
Watchdog Lower Limit (unit, s)	WDT_LLTICK	1m			
Watchdog Error Accumulator Limit	WDT_WWDT_ACC_TH	15			
Watchdog Question	WDT_DIS_LFSR	FALSE			

Figure 15. Watchdog Setting

Refer to the *Safety Application Note* for more details. The following are some recommendations on setting up the Watchdog feature:

- When the Watchdog feature is enabled, the PMIC can be set as either Q&A mode or Window mode.
- In Q&A mode, select either 16 QA or 4 QA.

- The Watchdog upper limit is required to be higher than the lower limit.

3.3.4.5 SoC Activation and Timeout Setting

Each SoC Activation sequence test can be independently enabled. Figure xx. shows the configurable options. Please refer to the SAN for more details.

The SoC activation timeout and error state timer can be configured to meet the desired timing requirements, shown in Figure 16. When PRESET# Check, Serial Interface Check, or System Test is enabled, please ensure the timeout setting is set appropriately. Each timeout setting is color coded to match the SoC Activation Test below.

	SoC Activation			
1	EXTPINCHK Enabled (PRESET - PRESETOUT)	PRESET_CHECK_DIS	FALSE	
2	Serial Interface Check Enabled	SINT_NOSTART_BYPASS	TRUE	
3	Sytem Test Enabled	STIL_MODE_EN	FALSE	
	EXTPINCHK2 Enabled	EXTPINCHK2_EN	FALSE	
			IO7	FALSE
			IO11 (PRESETb_LB)	FALSE
			IO12	FALSE
			IO15	FALSE
			IO16	FALSE
	Core Voltage Monitor Test Enabled		FALSE	

Figure 16. SoC Activation Test

	Timeout Settings		
	Parameter	Register Field Name	Time (s)
	Minimum Error State Timer	TIMEOUT_MIN_ERROR_ST	130m
1	Maximum time for PRESETOUT after PRESET# released	TIMEOUT_PRESETOUT	480u
	Time allowed for entire SoC Activation sequence	TIMEOUT_SOCACTIVA_ST	250m
3	Time allowed for System Test	TIMEOUT_STIL_MODE	5m
2	Serial Interface Check Timeout	SINT_TOUT	1056u
1	Time allowed for PRESET# -> PRESETOUT check	TIMEOUT_PRESET_CHK_TOUT	24m
3	Delay time before entering System Test state from SoC Activation	TIMEOUT_STIL_DLY_TIME	8m
	Timer from RESET to SOCACTIVATION when a reset condition occurs	TIMEOUT_PRESETOUT_DLY_TIME	56m

Figure 17. SoC Activation Timeout and Error State Timer

3.3.4.6 Fault Masking

All fault masking options are located at the end of the sheet. For initial sample testing, mask all faults except for OV/UV faults and PVIN fault. This allows for an easy verification of the regulators. After each regulator output voltage and sequence have been confirmed, additional fault reactions can be unmasked for testing.

3.3.4.7 Additional Customer Specific Settings

The Additional Customer Specific Settings section allows register settings that are not listed in the OTP creator to be configured. If required, contact a Renesas representative to help fill out this section.

3.4 V4H Power Supply Mapping

Table 6. V4H Power Supply Mapping

IC + Recommended Voltage Regulator	Output Voltage (V)	Maximum Current (A)	SoC Supply	Other connection
RAA271040	5V	-	VDD	RAA271005 RAA271010\RAA271011 VIN
RAA271010\RAA271011	0.75	23.6A	VDD0.75V	VDD VDD_PCIEn (n=0,1), VDD_CSIn (n=0,1), VDD_DSIn (n=0,1), VDD_DSIPLLn (n=0,1), VDD_DDRPLLn (n=01,23)
RAA271005_VOUT1	0.815V	4.3A	VDD_OD	-
RAA271005_VOUT2	1.05V	-	VDDQX_DDRn (n=0,1,2,3)	LPDDR5
	1.1V	-	VDDQX_DDRn (n=0,1,2,3)	LPDDR4x
RAA271005_VOUT3	1.8V	-	D1.8V	-
RAA271005_VOUT4	3.3V	2	D3.3V	-
RAA271005_VOUT5	0.5V	2.2	DDR0123_D0.5V	LPDDR5
	0.6V	2.2	DDR0123_D0.5V	LPDDR4x
RAA271005_LDO1	3.3V	0.035 + 0.025 + 0.003 + 0.001 = 0.064	SDHI_D1.8V/3.3V_LDO	VDDQ33, VDDQ18_33_SDHI, VDDQ18_33_I2C, VDDQ18_33_SPI
RAA271005_LDO2	3.3V	-	PMIC_VIO_LDO	-
RAA271005_LDO3	-	-	-	-
RAA271005_LDO4	-	-	-	-
RAA271005_LDO5	1.8V	0.4	DDR0123_D1.8V	-
RAA271005_LDO6	2.5V	0.3	VDDQ18_25_AVB <for TSN/AVB pins>)	-

3.5 V4H Power Supply Sequence

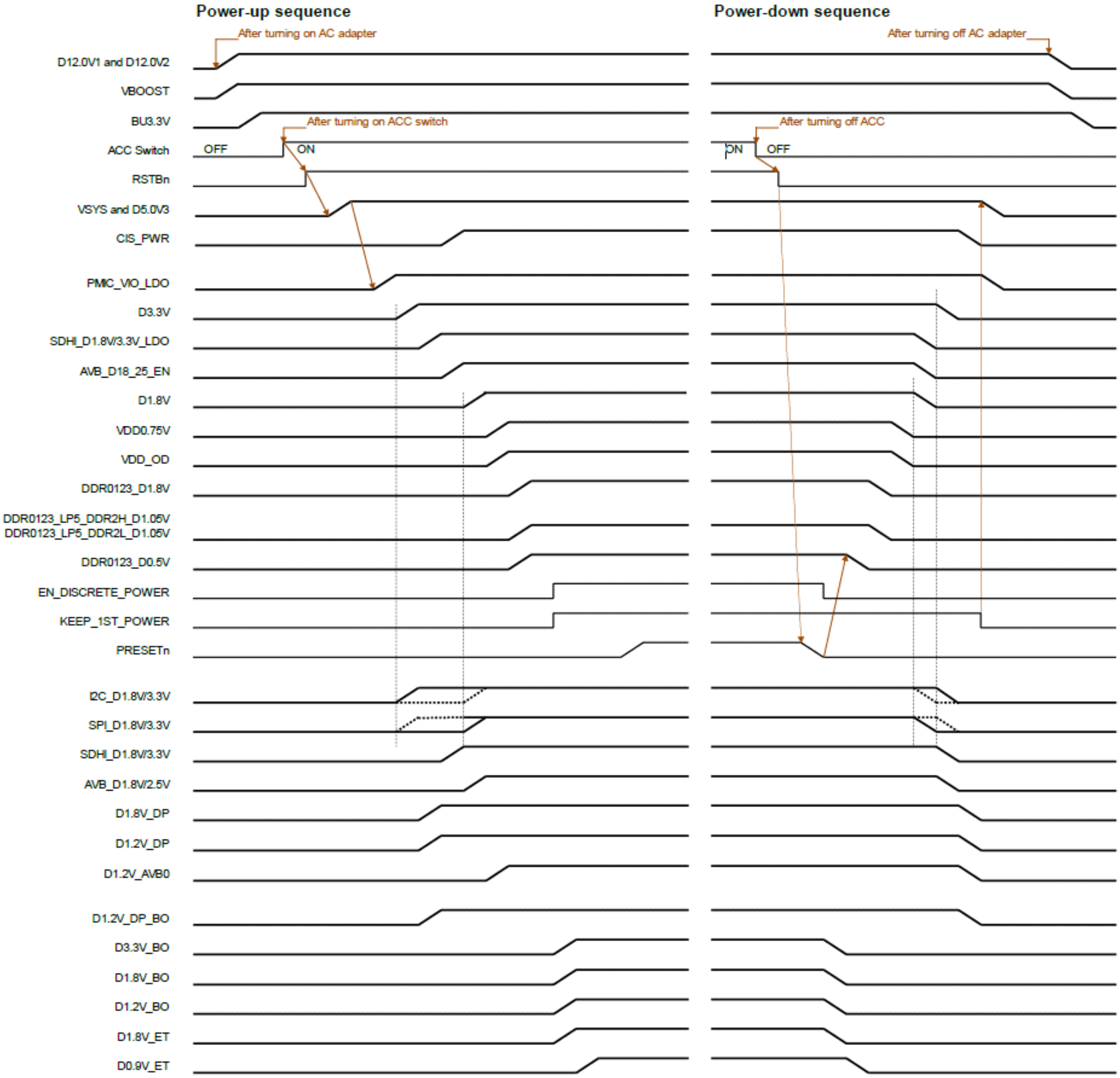


Figure 18. V4H Power-Up and Power-Down Sequence

3.5.1 RAA271005 Buck1 Dynamic Voltage Scaling

RAA271005 Buck1 has several options to achieve DVS. There are two independently programmable voltage settings for the Buck 1 controller, which can set the output voltage. These settings are DVS0 and DVS1. By changing the DVS number selected, the corresponding output voltage is selected. There are two methods to select the DVS output voltage.

- Method 1 – Using the IO6 pin to achieve DVS: This is the configuration used by the Whitehawk system reference board
- Method 2 – Use internal registers to select DVS by writing to the BUCK1_DVSSELECT bit in the BUCK1_DVSSEL register using SPI or I^2C. To use this method, the BUCK1_DVSCTRL bit must be set to 0b0 for the corresponding buck. The BUCK1DVSSELECT bit allows you to switch between the two different DVS settings with each corresponding to a set of DVS registers holding the DVS information.

3.6 RAA271010 Configuration

Paired with the Renesas Smart Power Stage RAA271011,the RAA271010 provides a complete solution for microprocessor core power supply. It can be configured as 4-, 3-, 2- or 1-phase, providing maximum flexibility for different power level of applications. The controller uses I2C or SPI bus to communicate with the system and achieves lower cost and smaller board area. Based on Renesas' R5 technology™, the PWM modulator compared to traditional modulators, has faster transient load response with minimum external components count. The RAA271010 has several other key features, including internal control loop compensation, remote differential voltage sense, programmable output, various fault monitor, etc.

3.7 RAA271011 Configuration

The RAA271011 is an integrated smart power stage optimized for synchronous buck applications to offer high current, high efficiency, and high power density. It enables voltage regulator designs to deliver up to 10A of continuous current and 15A peak current. Paired with Renesas multi-phase Buck controller RAA271010, it provides a complete solution for microprocessor core power supplies. The internal power MOSFETs use the Renesas state-of-the-art technology that delivers industry benchmark performance to significantly reduce switching and conduction losses. The RAA271011 incorporates an advanced MOSFET gate driver that features high-current driving capability, optimized dead time control, and an integrated bootstrap switch. The driver is also compatible with a wide range of PWM controllers, supports tri-state PWM, and 5V PWM logic.

3.8 RAA271040 Configuration

The RAA271040 is a dual buck controller that can operate across a wide VIN range of 3.75V to 42V. It supports wide duty-cycle operation for switching frequencies of 440kHz and 2.2MHz. To mitigate EMI, it supports synchronization to an external clock or programmable spread spectrum clocking. Its current-mode modulator is ideally suited to tolerate severe line transients. Also, the RAA271040 supports dropout operation and low 20ns on-time to operate through automotive cranking and load dump pulses.

The RAA271040 integrates robust MOSFET drivers and readily supports step-down applications requiring high output currents in normal operation. For applications that must also sustain extremely low power, always-on operation, the energy conservation mode can reduce operating current to 6µA. Integrated feedback for VOUT1 is provided for 3.3V or 5V applications to eliminate the current otherwise flowing in external feedback resistors. An automatic switchover to an external supply is also supported to maximize efficiency. A blocking diode is activated after startup to prevent the external supply from back-biasing a low input voltage at VIN.

3.9 RAA271041 Configuration

The RAA271041 is a controller for a dual regulator system supporting ASIL-D automotive systems that must continue to operate during battery dropout conditions. The Channel 2 boost regulator maintains the voltage rail that supplies the Channel 1 buck regulator, allowing the buck output to maintain regulation during a battery dropout event such as cold cranking.

The Channel 2 Boost in Cold Crank Boost mode has an adjustable output and is active when 2.2V < VBAT < 8V during the cold crank period. The output voltage from Channel 2 supplies the Channel 1 buck, which can either be configured as 3.3V or 5V fixed with a direct connection from FB1 to VOUT1 or be adjustable from 0.8V to 5V by using a resistor divider from VOUT1 to FB1 to ground.

The RAA271041 requires a minimum input voltage of 6V for start-up. The Channel 2 Boost has an input range from 2.2V to 42V while the Channel 1 Buck has an input range from 3.5V to 42V. The RAA271041 buck operates in Energy Conservation Mode (ECM) to provide a low IQ mode by reducing quiescent current draw to 6µA typical when no external load is applied. The buck switching frequency is factory programmed to 400kHz or 2.2MHz. The boost switching frequency is also factory programmed to 400kHz, or can optionally be 2.2MHz if the buck frequency is also 2.2MHz. Optional spread spectrum operation allows for a reduction of the EMI and noise levels.

4. Layout Guidelines

4.1 RAA271005 Layout Guidelines

- Place the input capacitors as close as possible to the Buck's PVIN and PGND pins with the least impedance routing
- Connect all PGND pins together through GND copper plane and use multiple vias connecting the inner and other GND layers.
- Connect the Buck-1 PH1 pins together through a PH1 copper plane on the PMIC component layer.
- Place inductors as close as possible to the PMIC.
- Place the output bulk capacitor COUT1 close to the inductor L1 output terminal.
  - Minimize the GND distance of the input capacitor CIN1 and the output capacitor COUT1. If CIN1 GND plane and CIN2 GND plane cannot be connected directly with copper, use enough vias connecting them to the inner or other GND plane respectively such as the two GND planes can be connected through the other GND layers with minimized resistance.
  - Solid ground plane is helpful for a good EMI performance, current conduction, and thermal dissipation.
- If possible, use two or multiple layer or wide enough PCB copper trace for the output voltage VOUT1 to minimize the conduction loss, since Buck-1 output carries high current.

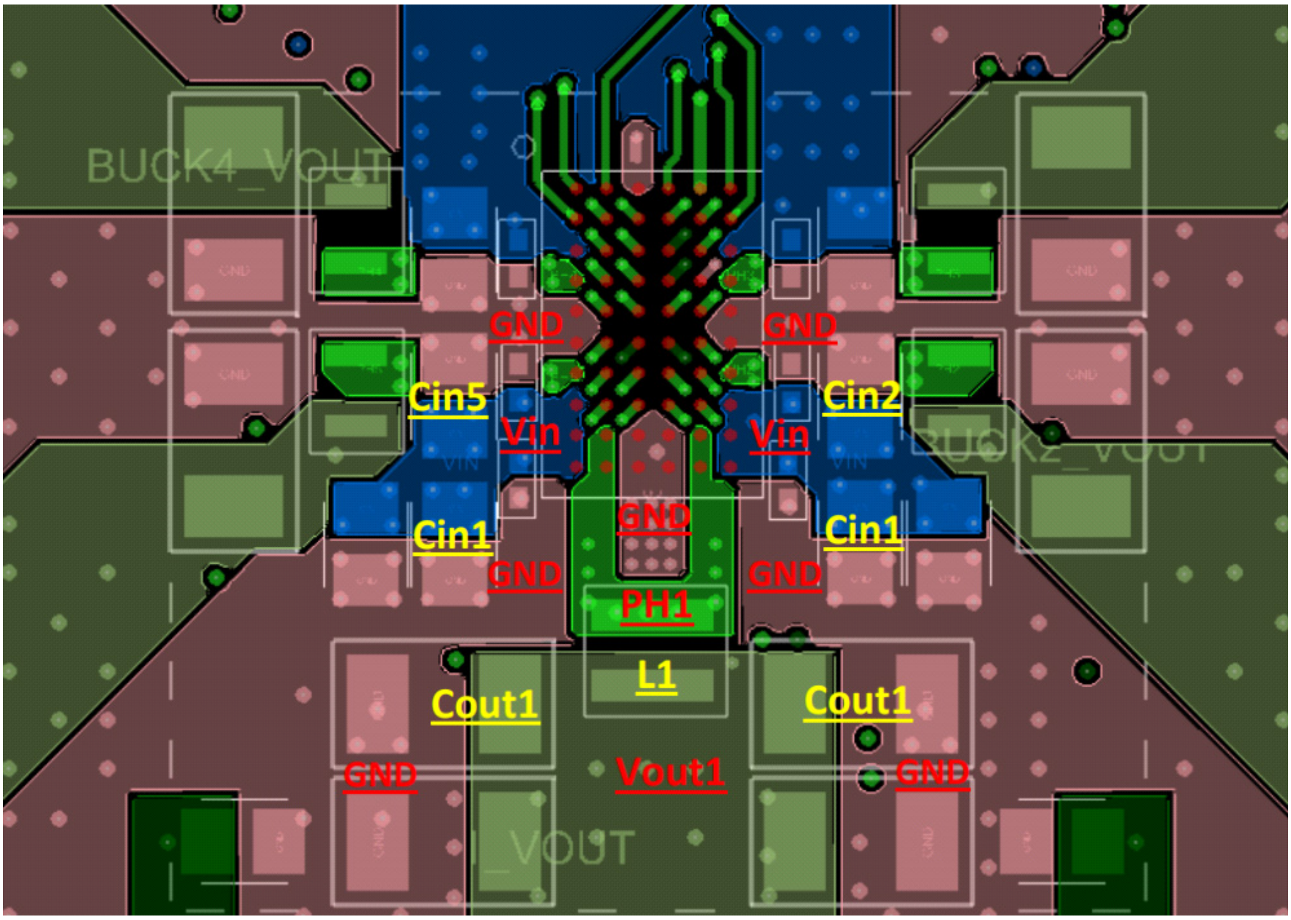


Figure 19. RAA271005 Component Placement Layout Recommendation

4.2 RAA271010 Layout Guidelines

Proper PCB layout is a very important design practice to ensure a satisfactory electrical and thermal performance.On the layout illustration figures, the signal/copper net name is labeled in RED text; the component is labeled inYELLOW text. RAA271010 and RAA271011 are placed on the PCB top component layer.

- Place the AVIN pin and VIO pin decoupling caps as close as possible to the pin.
- Use multiple vias connecting RAA271010 bottom pad to the internal or other GND layers.
- Run the VOUT and RTN output voltage feedback differential trace in parallel
  - Connect the VOUT and RTN differential sensing point to the output high frequency ceramic cap bank to minimize the feedback ripple and noise.
  - Shield the VOUT and RTN differential parallel traces with GND copper.
  - Stay away from the RAA271011 PHASE and BOOT the noisy signal via/trace/copper.
  - Stay away from the PWM1/2/3/4 the noisy signal via/trace/copper.
  - Stay away from the IBALP1/2/3/4 the noisy signal via/trace/copper.
  - Stay away from any high-speed digital signals.
- Run the IBALPx/IBALNx traces in parallel to RAA271011, shield with GND copper, keep any sensitive signal away since IBALPx signal which is noisy.
- Keep any sensitive signal away from PWM1/2/3/4 via/trace/copper.
- Keep GPIO0/1 and MPIO0/1/2/3 traces away from PWM1/2/3/4 and IBALP1/2/3/4 the noisy signal via/trace/copper.

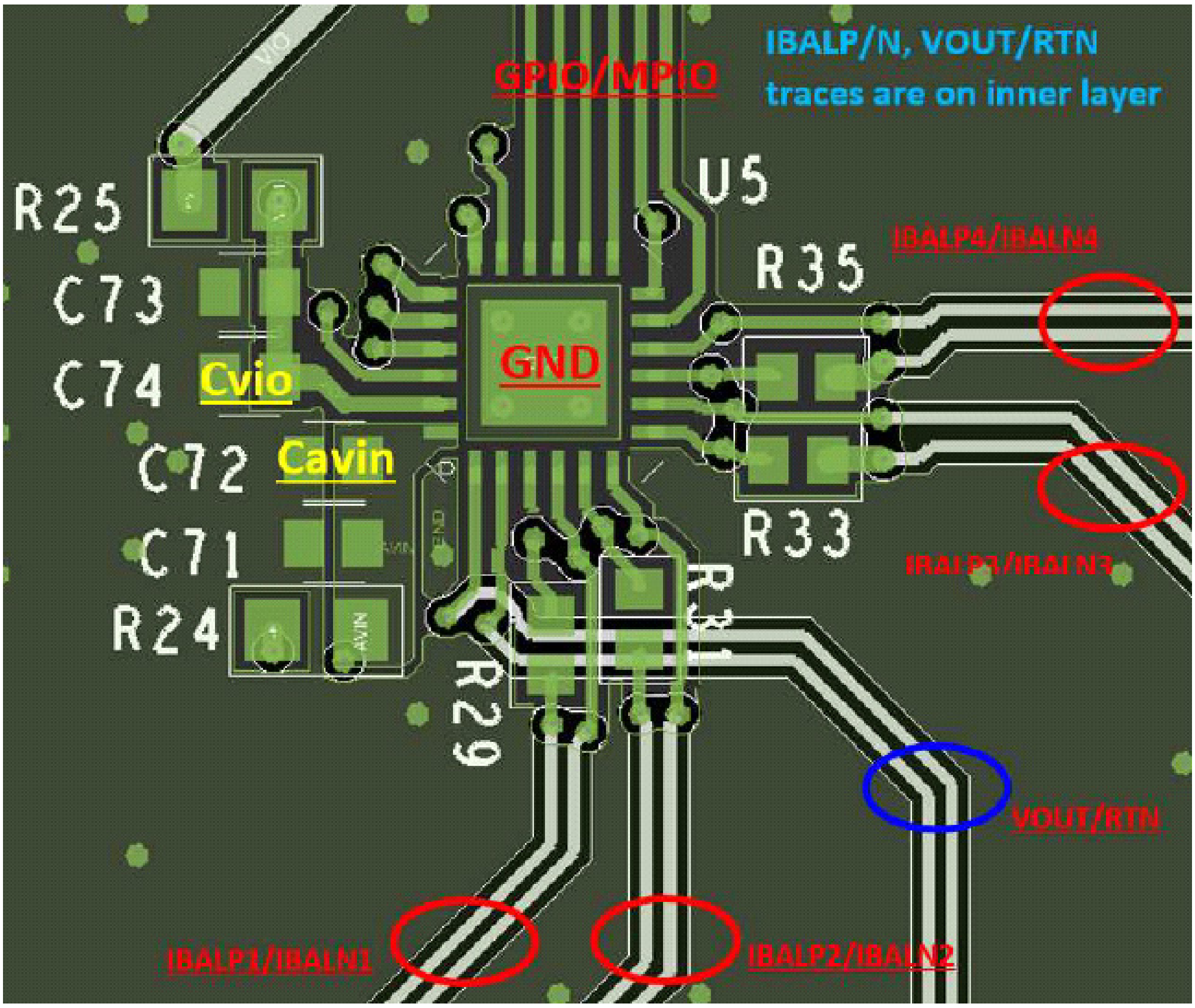


Figure 20. RAA271010 Component Placement Layout Recommendation

4.3 RAA271011 Layout Guidelines

- On the layout illustration figure, the signal/copper net name is labeled in red text; the component is labeled in yellow text. RAA271011 are placed on the PCB top component layer. Take one phase of RAA271011 as an example for multi-phase application.
- Place the input decoupling caps CIN as close as possible to PVIN and PGND pins, on both sides of RAA271011 PVIN pins (Pin 6 and Pin 15, respectively).
- Connect all the GND copper planes together with multiple vias connecting to the inner and other GND layers.
- Connect all the PHASE pins together through a PHASE copper plane on the RAA271011 component layer.
- Place the inductor L1 as close as possible to the RAA271011.
- Place the output bulk capacitor COUT close to the inductor L1 output terminal.
- Minimize the GND distance of the input capacitor CIN and the output capacitor COUT.
- If CIN GND plane and COUT GND plane cannot be connected directly with copper, use enough vias connecting them to the inner or other GND planes respectively, such as the two GND planes can be connected through the other GND layers with minimized resistance.
- Solid ground plane is helpful for a good EMI performance, current conduction and thermal dissipation.
- If possible, use two or multiple layers or wide enough PCB copper trace for the output voltage VOUT to minimize the conduction loss, because the buck output carries high current.
- Run the IBALP/IBALN traces in parallel, shield with GND copper, keep any sensitive signals away because theIBALP signal is noisy.
- Keep sensitive signals away from the PWM via/trace/copper.

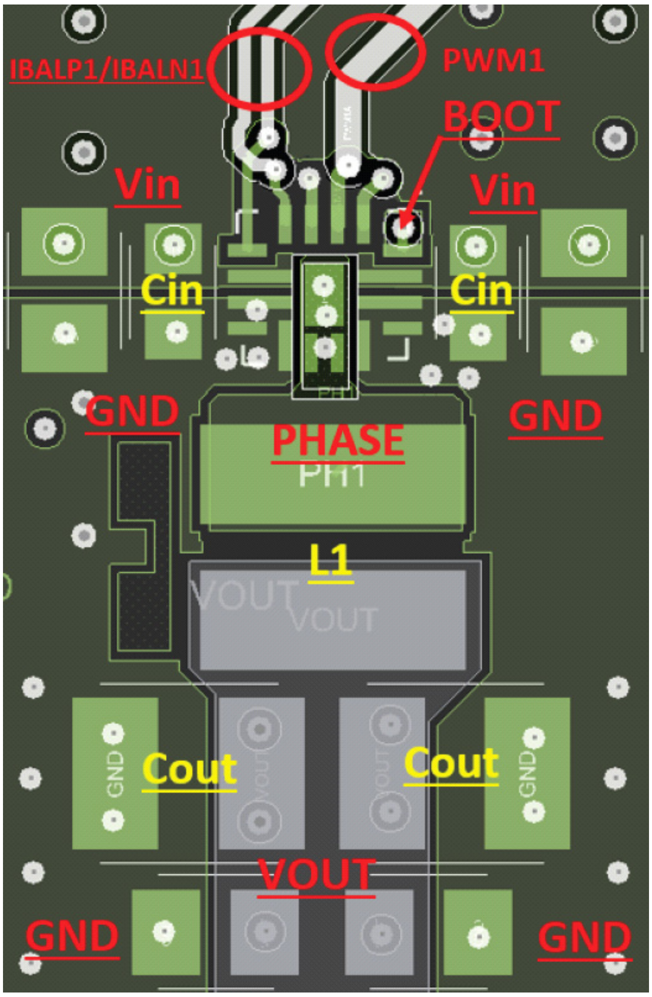


Figure 21. RAA271011 Component Placement Layout Recommendation

4.4 RAA271041 Layout Guidelines

Correct PCB layout is critical for proper operation of the RAA271041. Each channel of the switching buck converters requires specific attention to minimize the power loop area for highly efficient, stable operation. It is also important to consider routing the shared common areas between the two converters. Route the primary paths in a single layer copper if possible to reduce parasitic inductance in the power current paths.

The following are layout instructions

- In Figure 22, connect the common connection between input capacitors, output capacitors, and the low-side FET for each buck converter through the central ground (gray) area.
- When the high-side MOSFET is switched ON and OFF, the power current alternates flowing through the input capacitor and high-side MOSFET, or the low-side MOSFET. Minimize the loop area between CIN, the high-side MOSFET, and low-side MOSFET to reduce interference from the high di/dt intervals as the current alternates between the MOSFETs.
- The first inner layer below the top copper layer with power components should be a ground layer that is complete as possible, as indicated in Figure 22 using the light green fill. This provides a tightly coupled ground return path for the power circuitry. This layer is also used in conjunction with many vias to create a low-impedance connection from the common power GND region to the ISL78264 controller, and the thermal pad is connected to this plane using multiple vias.
- Connect the signal ground (Pin 11) to the thermal pad ground directly under the IC. For best noise immunity, signal pins such as COMP, RT, and configuration resistors can be connected in a small SGND pour that connects to Pin 11, which connects to PGND in a single point connection under the IC.
- Each converter has ISNS connections that should be routed as shown in Figure 22. The ISNS traces are routed on the second inner layer, which is shielded from power switching currents by the ground area on the inner layer 1. Begin the ISNS traces as a kelvin connection through a via in the center of the sense resistor in each converter.
- Minimize the trace lengths on the feedback loop and route around switching power circuits to minimize noise pick-up.
- Place the capacitors on VIN (Pin 26) and VCC (Pin 19) close to respective pins and ground connection.

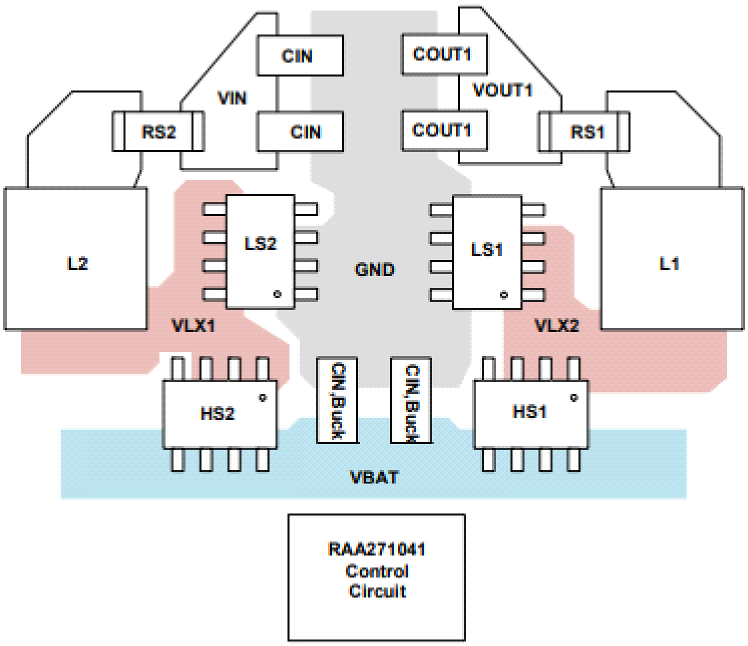


Figure 22. RAA271041 Component Placement Layout Recommendation

5. Revision History

Revision	Date	Description
1.01	Dec 15, 2025	Updated Page 1, Target Power-Supply ICs Updated Figure 1. Updated Figure 3. Updated Table 6.
1.00	Nov 18, 2025	Initial release.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Disclaimer Rev.5.0-1)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/