Application Note

DA914x PCB Layout Recommendations

AN-PM-145

Abstract

This application note provides recommendations on how to place and route DA914x devices. It also gives guidance on the passive components needed for proper functioning of the system. This document is a guideline only; target applications may have different requirements.

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1 Terms and Definitions

EVB	Customer evaluation board
FET	Field effect transistor
GND	Ground
GPIO	General purpose input or output
IC	Integrated circuit
PCB	Printed circuit board
FC-BGA	Flip chip, ball grid array

2 References

[1] DA9141-A, DA9142-A Datasheets (for automotive applications), Renesas
[2] DA9141, DA9142 Datasheet (for standard applications), Renesas
[3] DA9140 Customer Evaluation Board Schematic, DA9140-30-A_sch.pdf, Renesas
[4] AN-PM-010, PCB Layout Guidelines for Dialog PMICs, Application Note, Renesas
[5] UM-PM-061, DA9140 Quick Guide EVB, Renesas
[6] UM-PM-062, DA9140 User Guide EVB, Renesas

Note 1 References are for the latest published version, unless otherwise indicated.

3 Introduction

Renesas' DA9141 and DA9142 devices are power management ICs with integrated power FETs, see datasheets [1] and [2]. DA9141 is a single channel, quad-phase buck converter capable of driving up to 40 A loads, while the DA9142 is a dual-phase buck converter capable of driving up to 20 A loads.

The recommended components and connections for DA9141 are shown in Figure 1 and Table 1. Note that AEC-Q200 compliant components are required for Automotive applications.

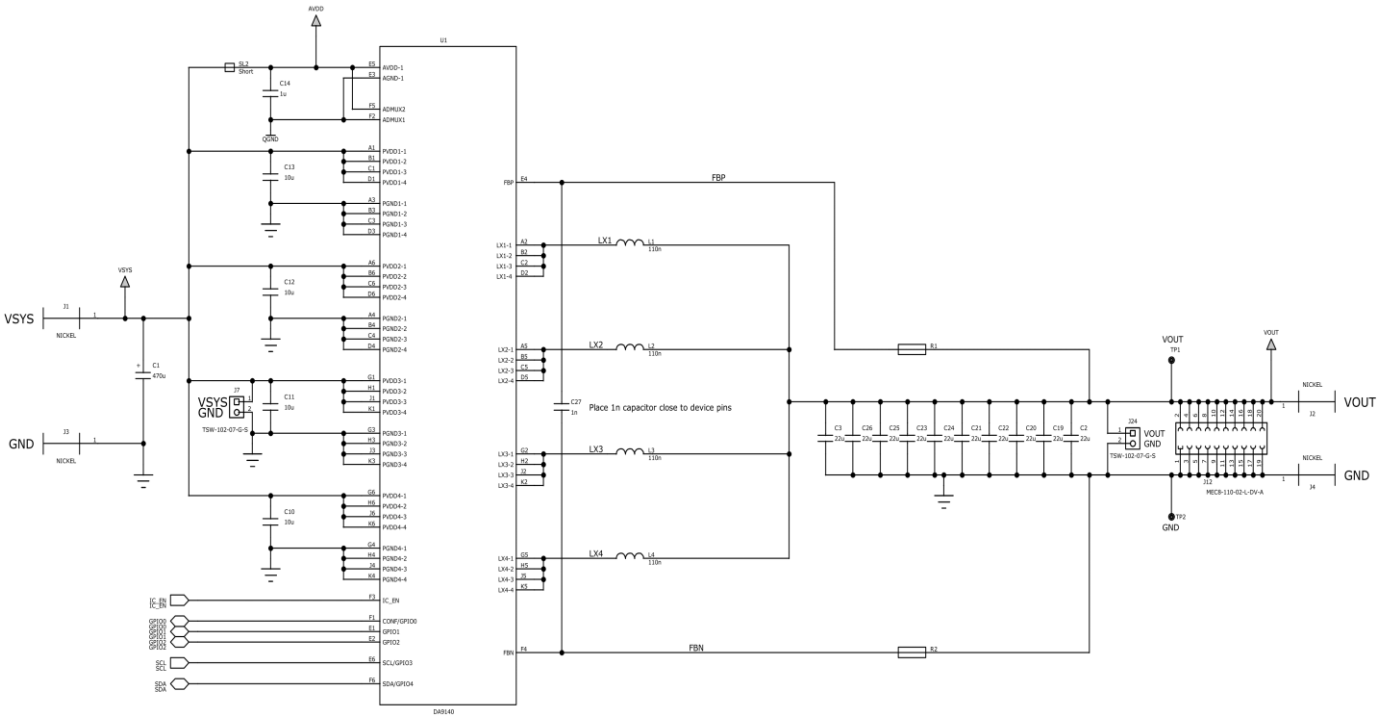


Figure 1: DA9141 Recommended Components and Connections

The details of the design reference can be obtained from the Customer Evaluation Board (EVB) schematics [3]. The EVB is described in the User Guides [5] and [6].

Details on recommended components are listed in Table 1.

Table 1: DA9141 Recommended Components

Application	Part Reference	Value	Part number
AVDD Bypass Capacitor	C14	1 µF	GCM188R71E105MA64
PVDD Bypass Capacitor	C10, C11, C12, C13	10 µF	GCM188D70J106ME36D
VOUT Bypass Capacitor	C2, C3, C19, C20, C21, C22, C23, C24, C25, C26	22 µF	GCM188E70E226M
FB Bypass Capacitor	C27	1 nF	GCD188R71H102KA01D
Output Inductor	L1, L2, L3, L4	112 nH	CLT3225AR11MI3

4 Layout Recommendations

DA914x is packaged in a 60-pin FC-BGA package with a 0.65 mm pitch.

At least a four-layer PCB stack-up should be used for best PCB layout design. However, the number of routing layers and other PCB parameters are also determined by the other devices in the system.

These recommendations are with reference to the DA9140 EVB, a six-layer PCB. General PMIC layout guidelines are provided in AN-PM-010 [4].

4.1 DA914x Package Information

4.1.1 Ball Map

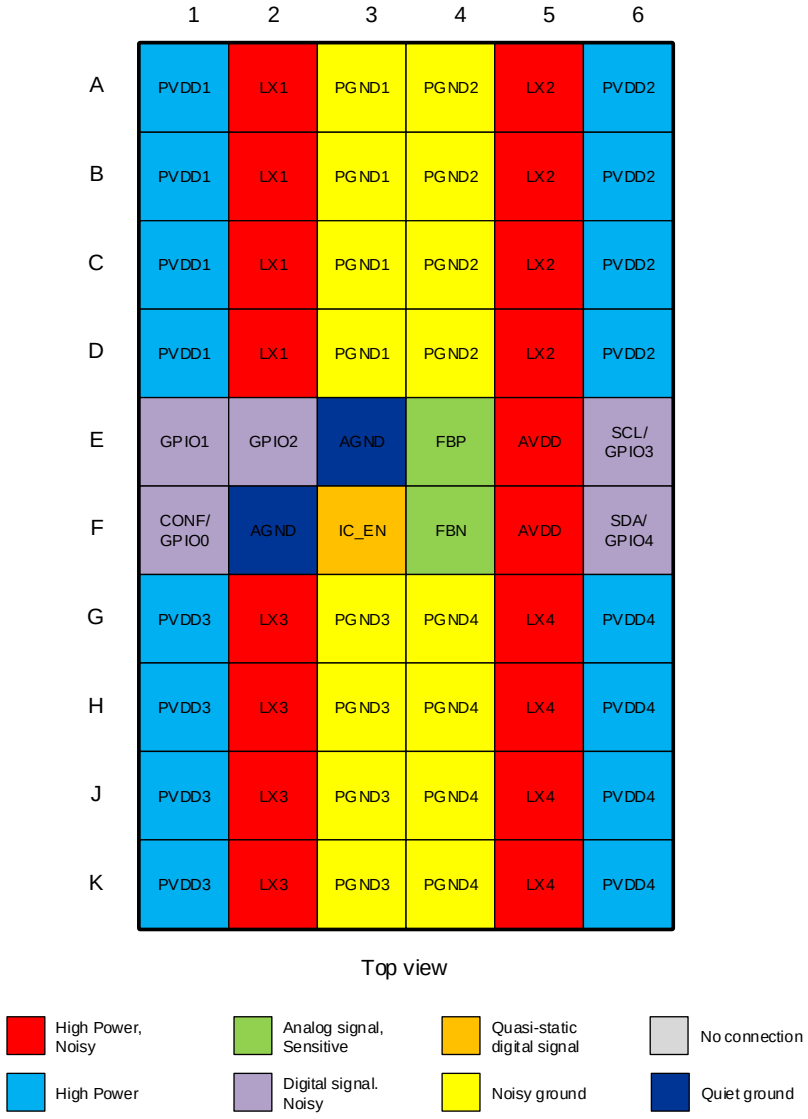
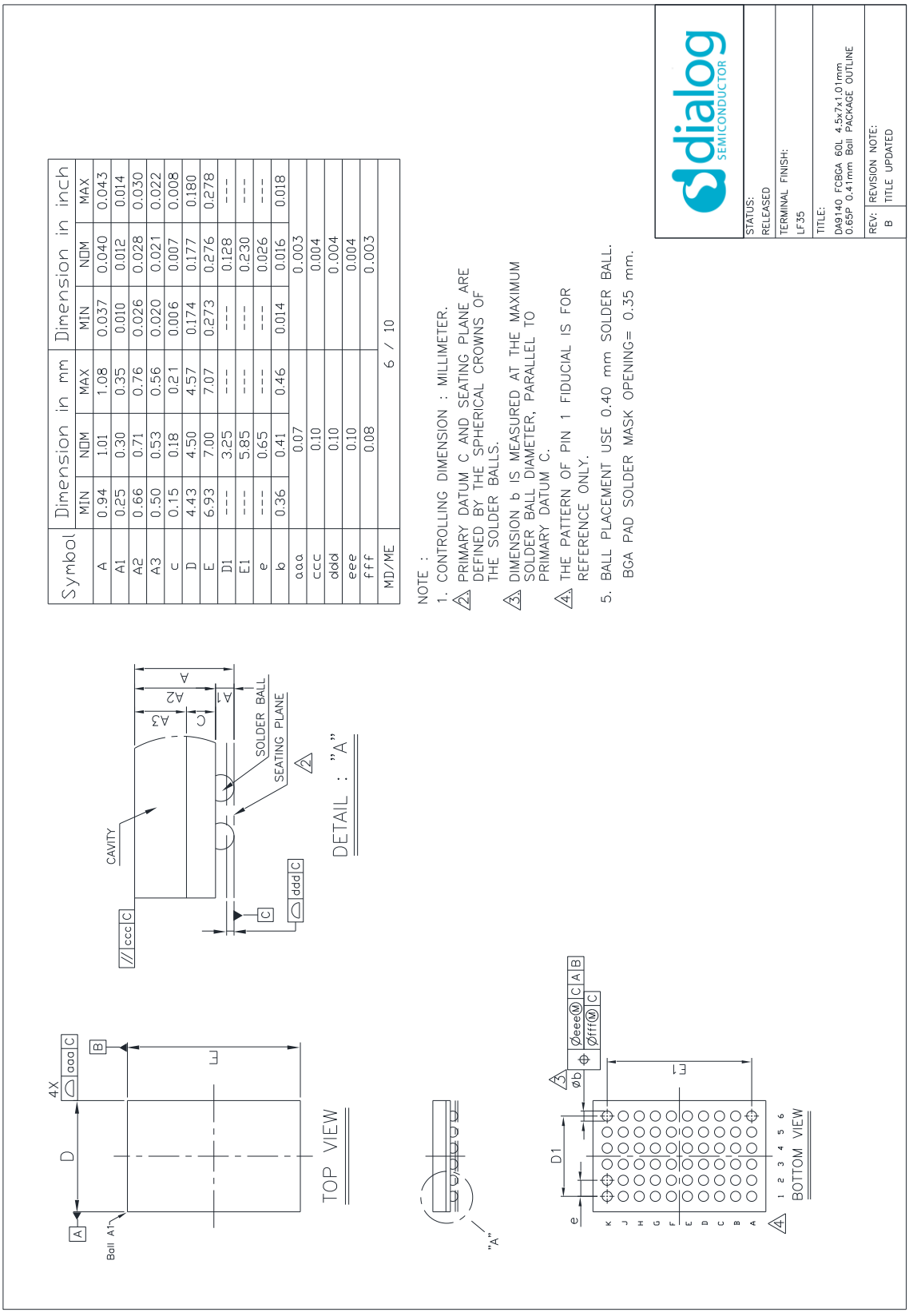


Figure 2: Ball Map

4.1.2 Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.94	1.01	1.08	0.037	0.040	0.043
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.66	0.71	0.76	0.026	0.028	0.030
A3	0.50	0.53	0.56	0.020	0.021	0.022
c	0.15	0.18	0.21	0.006	0.007	0.008
D	4.43	4.50	4.57	0.174	0.177	0.180
E	6.93	7.00	7.07	0.273	0.276	0.278
D1	---	3.25	---	---	0.128	---
E1	---	5.85	---	---	0.230	---
e	---	0.65	---	---	0.026	---
b	0.36	0.41	0.46	0.014	0.016	0.018
aaa		0.07			0.003	
ccc		0.10			0.004	
ddd		0.10			0.004	
eee		0.10			0.004	
fff		0.08			0.003	
MD/ME						

Figure 3: Package Outline Drawing

4.1.3 Layout Guidelines

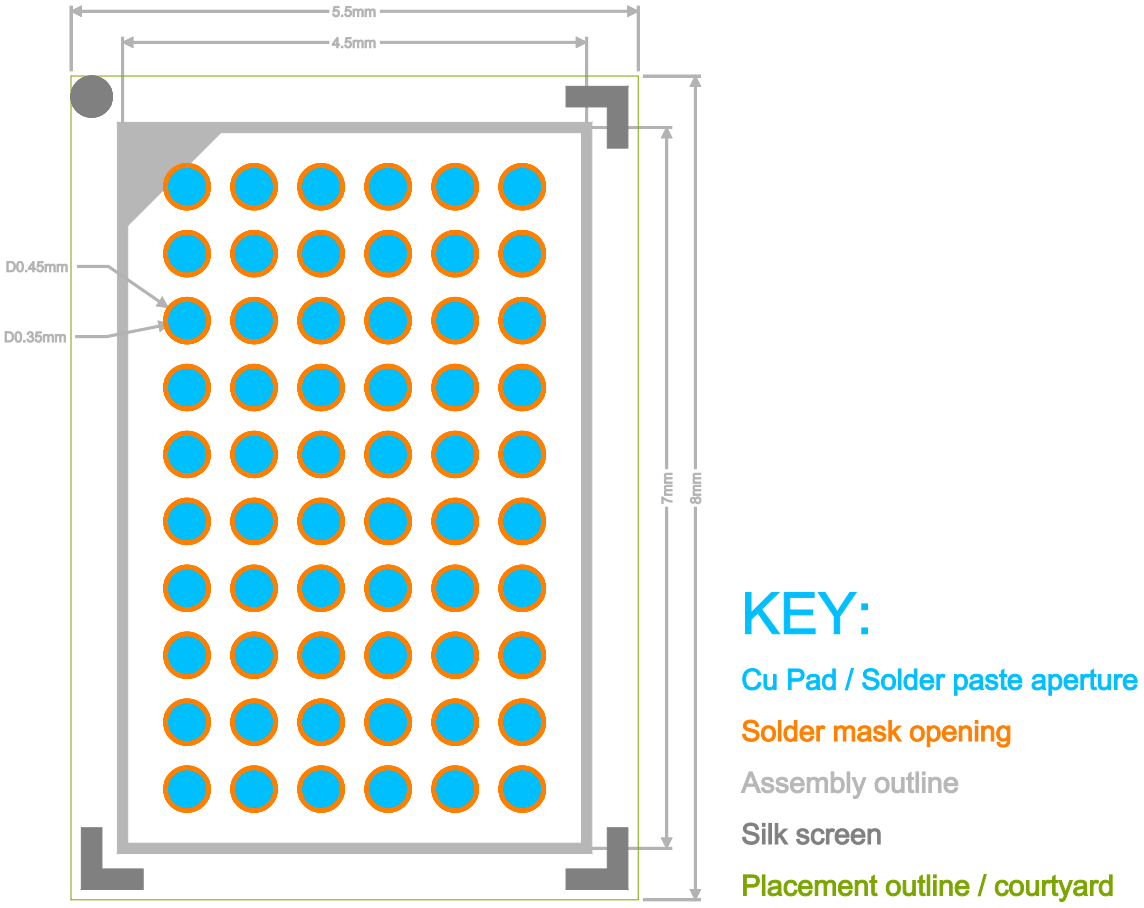


Figure 4: DA914x-A Footprint

4.2 Buck Converter

DA914x follows the standard buck layout procedure with output capacitors placed as close as possible to the load. Due to the device's ability to deliver high currents, a wide output trace for minimized parasitic impedance is recommended.

4.2.1 DA914x Input

In a buck converter layout, the input capacitor location is critical. Locate the input capacitor as close as possible to the device’s input and power GND pins to minimize the parasitic inductance.

In DA914x layout design, the input capacitor for each phase should be placed as close as possible to the PVDD<x> and PGND<x> pins, and on the same layer as the DA914x device.

If multiple layers are used, it is recommended to use at least four through-hole vias per phase (or at least twelve microvias per phase) to connect the input voltage (VSYS) between layers to minimize line resistance.

The DA914x has separate AVDD supply pins for the internal analog circuits. A 1 µF bypass capacitor (C14) should be placed close to the device’s AVDD pin. The AVDD pin input and buck converter input (PVDD<x>) share the same net, but it is important to separate these traces. Do not connect both traces directly on the same layer.

DA914x PCB Layout Recommendations

Ensure that the AVDD pin is connected to the input voltage (VSYS) plane far enough from the buck's input voltage plane so switching noise from the buck converter input (PVDD<x>) is not injected to the AVDD pin.

Figure 5 shows the input capacitor placement and routing recommendation.

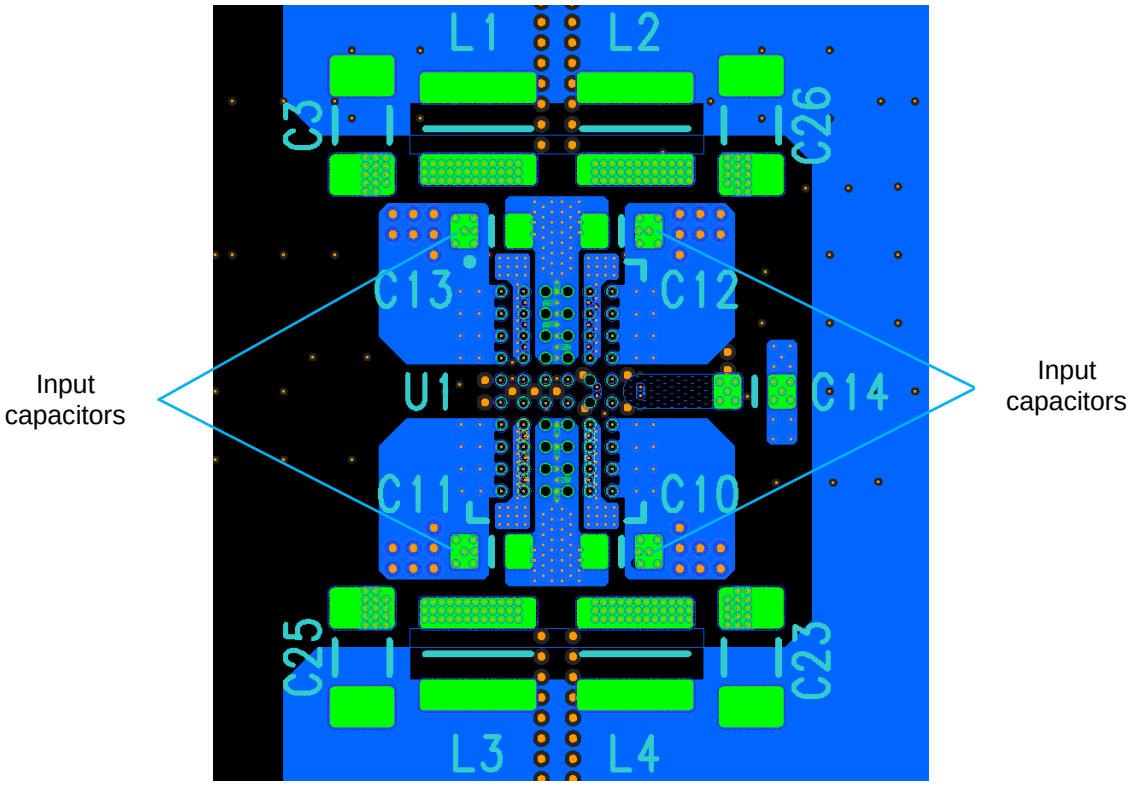


Figure 5: Recommended Input Capacitor Placement and Routing (Layer 1)

Figure 6 shows more details about the connection to the AVDD capacitor, connecting to a quiet ground plane on Layer 5 and a separate AVDD trace for connection to VSYS elsewhere on the board, far from the buck switching currents.

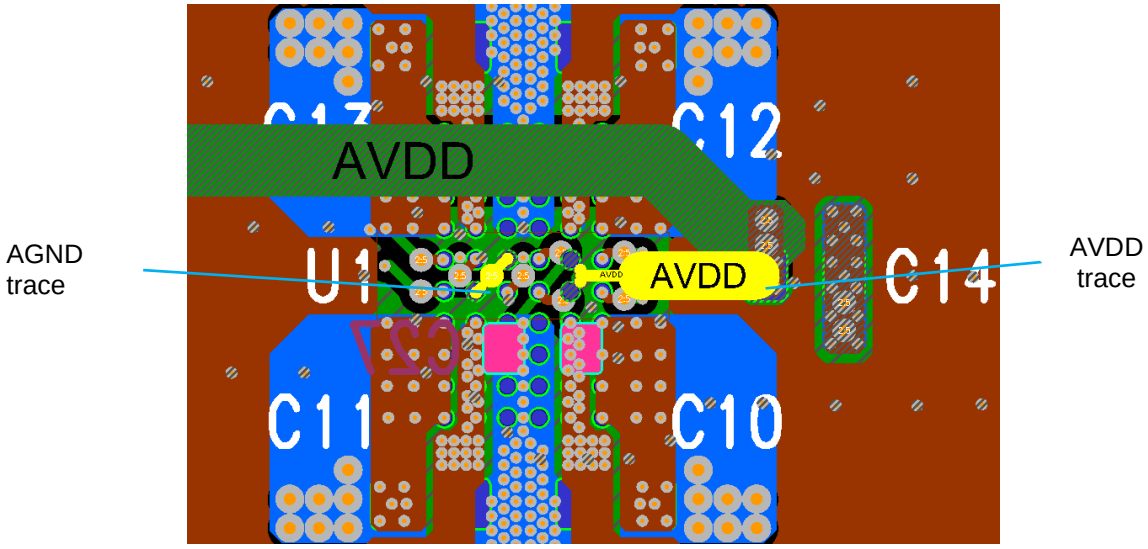


Figure 6: Recommended Input Capacitor Placement and Routing (Layers 1 and 5)

4.2.2 Ground Connections

Special care should be taken with ground connections because of the high current capability of DA914x, and because of the device's high-performance requirements.

The power GND terminals (PGND<x>) of the DA914x are placed between each phase's LX pin.

It is best practice to isolate quiet analog GND (AGND) from noisy power GND terminals (PGND<x>) and to connect them at a single point.

AGND is isolated from the power GND terminals (PGND<x>) at the top layer (component layer) and connected at a single point on the bottom layer. Figure 6 shows more details about the AGND connection to the quiet ground plane on Layer 5.

Layer 2 can be used as a return power GND plane, where the device's PGND pins and output capacitor GND can be connected. It is recommended to minimize the line impedance of the PGND pins and output capacitor GND connections by using as many vias as possible. This will also improve the heat dissipation.

An example of how to connect the GND terminals is illustrated in Figure 7.

NOTE
It is recommended to use copper plugged vias to achieve the minimum parasitic via impedance and best thermal performance.

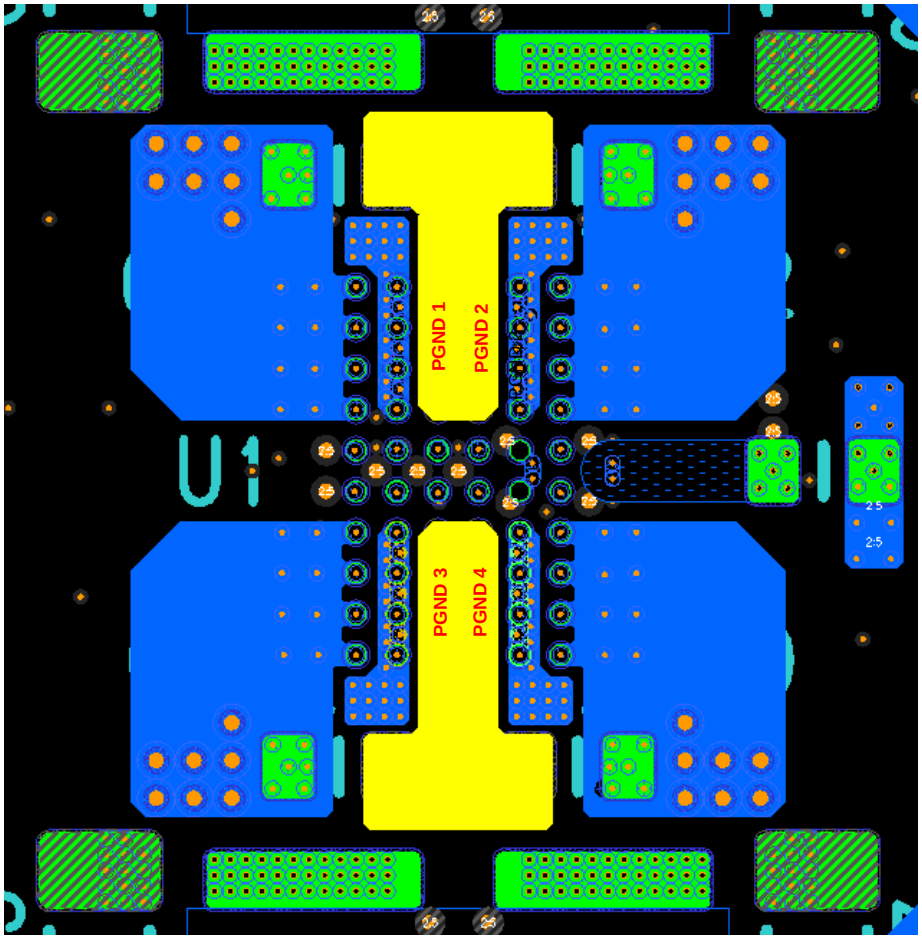


Figure 7: Recommended Power Ground Traces

4.2.3 LX Routing

Switch node/LX node traces (traces between LX pins and output inductors) need to be kept as short as possible since this node generates switching noise, which can interfere with buck converter stability. Very high current will flow through this trace and so the width of trace used for this LX node must be considered. Also, ensure that there are enough vias to deliver the current.

The LX node patterns on the DA9140 Evaluation Board are shown in the top level view in Figure 8.

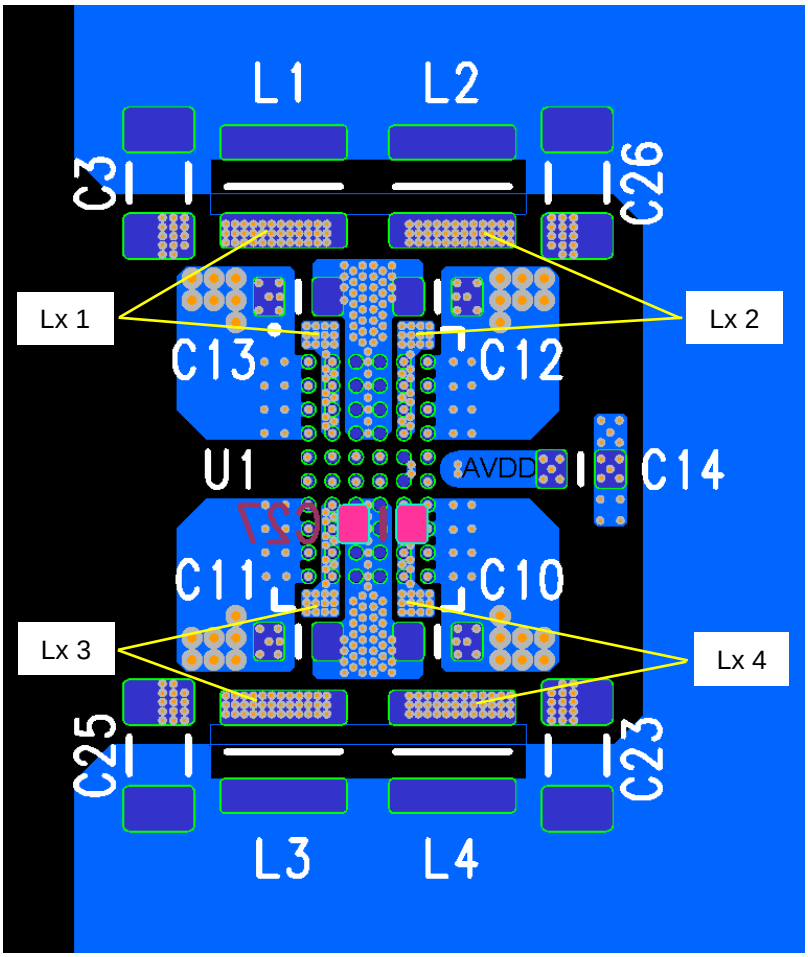


Figure 8: LX Node Pattern on DA9140 Evaluation Board (Layer 1)

On the bottom side in red the FB Bypass Capacitor C27 is visible. Figure 9 on the next page shows the traces of the Lx nodes of layer 2.

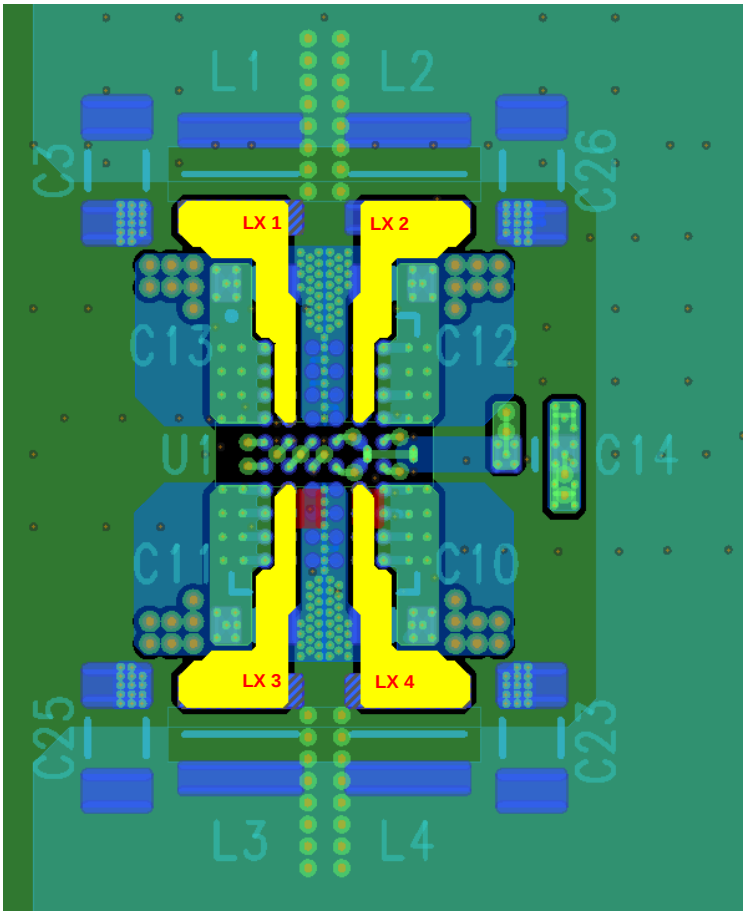


Figure 9: LX Node Traces on DA9140 Evaluation Board (Layer 2)

4.2.4 Buck Output

Output capacitors should be placed as close as possible to the load. However, minimizing the distance (which minimizes the line impedance) from the output inductors to the output capacitors (the load) is also important since it directly affects the efficiency and load transient response performance of the buck converter. Care must be taken with the size of the output traces since the output peak current can be up to 40 A for DA9141.

It is best practice to transfer the output current at the top layer directly without using any vias. This will give the best performance in terms of efficiency and load transient response performance.

4.2.5 Feedback Lines

Feedback lines must be routed as a differential pair far from any noise source (for example, output inductors, or LX node). It is strongly recommended to place a bypass capacitor (typically 1 nF) between the positive and negative sides of the differential feedback. The bypass capacitor should be placed as close as possible to the IC. It is useful for filtering noise which may be injected to the feedback lines due to a layout limitation (for example, a long feedback pattern or noise from other devices in the system).

Ensure that the feedback lines are not overlapping any noisy node traces (for example, the LX node trace) without an insulation plane in between. If DA914x is assembled on the top layer, it is recommended to route the feedback lines on Layer 4 or below when the traces are near to the IC and the switch node areas. It is also recommended that the feedback lines are shielded by a quiet ground on their routing layer to avoid lateral coupling to other signals.

NOTE
• The negative feedback trace is at ground potential and care should be taken not to connect any part of the trace to the ground plane. • The feedback lines must be routed directly from the load point in order to achieve the best voltage accuracy and stability.

Examples of output-voltage feedback-line routing, on the Dialog DA9140 Evaluation Board, are shown in Figure 10.

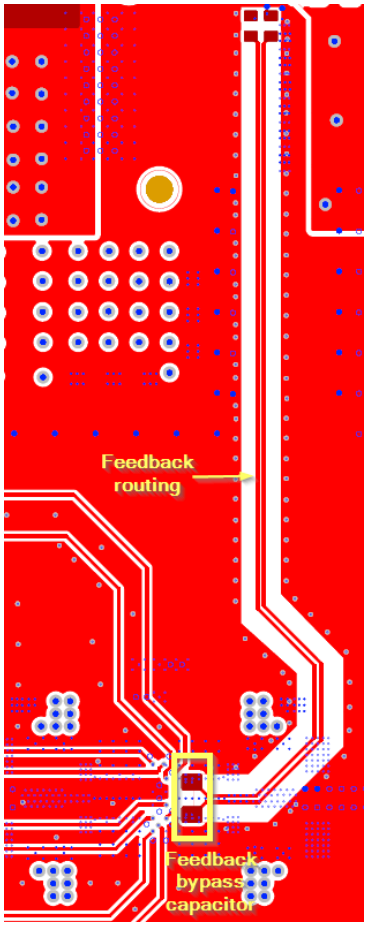


Figure 10: Output Voltage Feedback Line Routing on DA9140 Evaluation Board (Layer 6)

4.3 Communication Interface (I^2C)

It is recommended to route the communication interface far from any noise source.

Care must also be taken regarding the noise produced by the interface signal in order to avoid coupling to the sensitive analog references and feedbacks. The routing layer is not critical, but it is recommended to use the bottom or top layer.

4.4 GPIO Signals

Generally, GPIOs have the lowest routing priority. Any layer can be used for routing these signals.

However, care must be taken regarding the noise produced by the GPIOs in order to avoid coupling to the sensitive analog references and feedbacks.

Appendix A Input Network Parameters

The examples in this section are provided for reference. They use an evaluation board that follows the guidelines set by this document and can be taken as a target specification if the exact guidelines cannot be followed.

A.1 AVDD to AGND Loop

Figure 11 shows the impedance plot for the AVDD to AGND path including a GRM155R61A105KE15D capacitor. The effective inductance at 1 GHz should be kept below 250 pH.

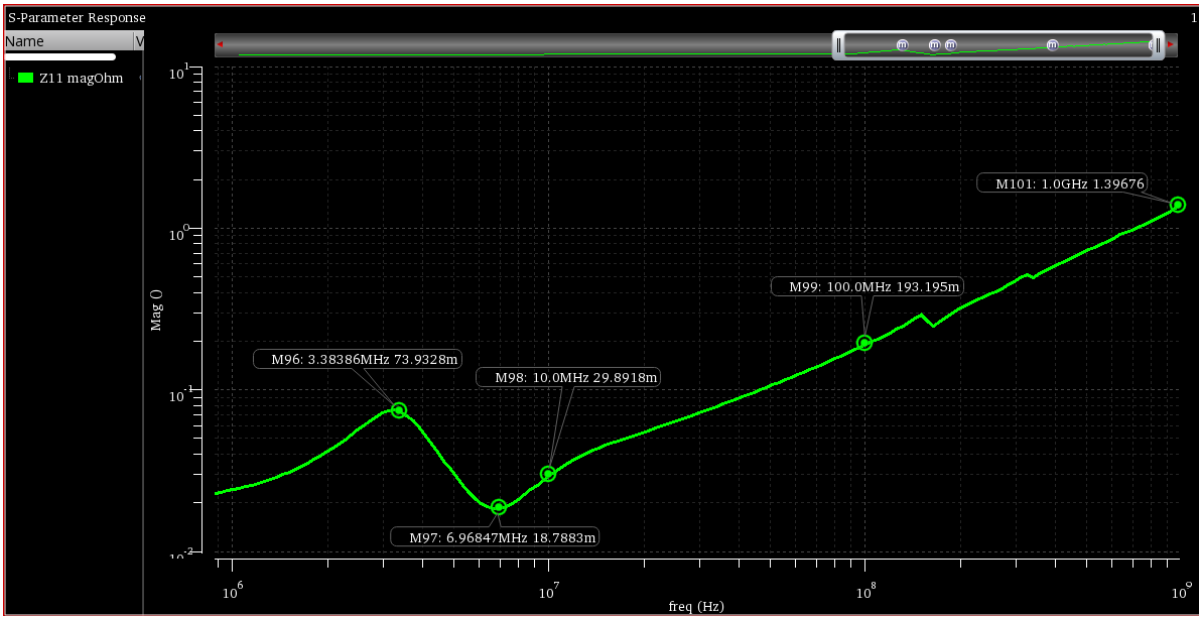


Figure 11: AVDD to AGND Path Impedance Including Capacitor

A.2 FBP to FBN Loop

Figure 12 shows the impedance plot for the FBP to FBN path including a GRM155R71H102KA01D capacitor.

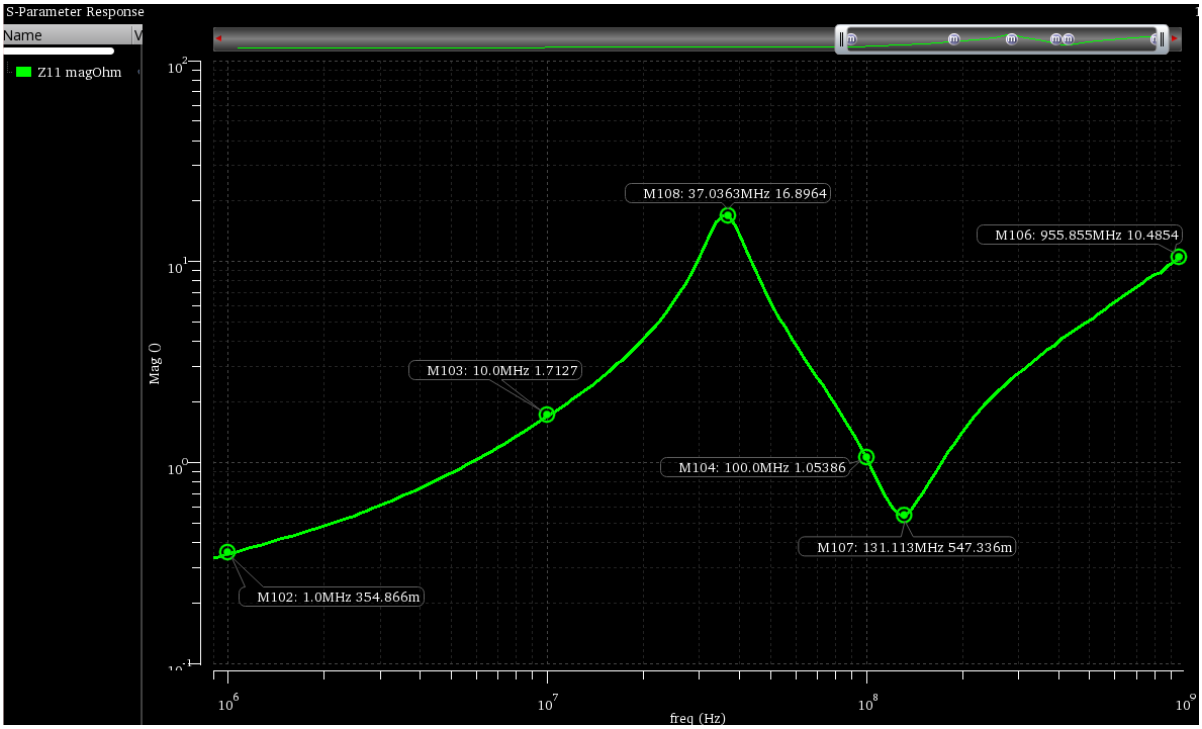


Figure 12: FBP to FBN Path Impedance Including Capacitor

A.3 PVDD to PGND loop

Figure 13 shows the impedance plot for the path from a single phase PVDD to its own PGND including two GRM188R61E106MA73 capacitors. The effective inductance at 1 GHz should be kept below 200 pH.

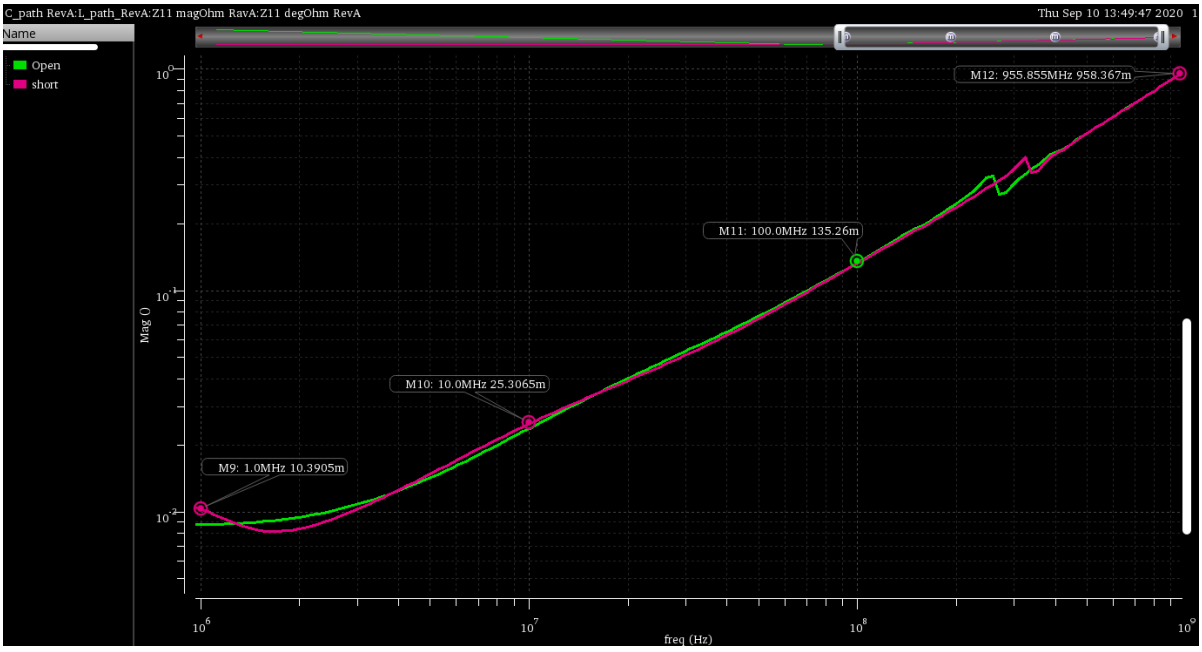


Figure 13: PVDD to PGND Path Impedance Including Capacitors

Revision History

Revision	Date	Description
1.1	06-Mar-2023	Added PCB Footprint
1.0	04-Feb-2022	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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