
R32C/116, 117, 118, 116A, 117A, and 118A Groups

Multi-Master I²C-bus Interface

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1. Abstract

This document describes how to use the multi-master I²C-bus interface (I²C-bus interface) function.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

MCUs: R32C/116 Group, R32C/117 Group, R32C/118 Group, R32C/116A Group, R32C/117A Group, and
R32C/118A Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above groups. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Overview

The I²C-bus interface is a serial communication circuit based on the I²C-bus data transmit/receive format, and is equipped with arbitration lost detection and clock synchronous functions.

3.1 General Call

A general call can be detected when the address data is all 0's.

A general call means that the master transmits general call address 00h to all slaves.

3.2 Addressing Format

7-bit addressing format is supported.

Only the 7 high-order bits of the I²C-bus slave address register (slave address) are compared with the address data.

3.3 I²C-bus Interface Related Pins

MSCL pin: Clock I/O pin of the I²C-bus interface.

MSDA pin: Data I/O pin of the I²C-bus interface.

3.4 Selectable Functions

The functions below can be selected when using the I²C-bus interface.

(1) Transmit/Receive modes

There are four transmit/receive modes available when performing data communication:

- Master-transmission mode: Start and stop conditions are generated (master mode). Address and control data are output to the MSDA in synchronization with the MSCL clock generated by the master device.
- Master-reception mode: Data from the transmitting device is received in synchronization with the MSCL clock generated by the master device.
- Slave-transmission mode: Start and stop conditions generated by the master device are received (slave mode). Control data is output in synchronization with the clock generated by the master device.
- Slave-reception mode: Data from the transmitting device is received in synchronization with the clock generated by the master device.

(2) SCL mode

SCL mode can be selected from Standard-mode (100 kHz or less) and Fast-mode (400 kHz or less).

(3) ACK clock

ACK clock can be selected from the following:

- ACK clock not available: No ACK clocks are generated after a data transfer.
- ACK clock available: The master generates an ACK clock each time 1 byte of data is transferred.

(4) Data format

Data format can be selected from the following:

- Addressing format: The received slave address and bits SAD6 to SAD0 in the I2CSAR register are compared. When an address match is found or when a general call is received, an interrupt request is generated and additional data is transmitted and received.
- Free data format: An interrupt request is generated and additional data is transmitted and received regardless of the received slave address.

4. Data Transmit/Receive Example

The data transmit/receive examples are described in this section. The conditions for the examples are below.

- Slave address: 7 bits
- Data: 8 bits
- ACK clock available
- Standard-mode, bit rate: 100 kbps (fIIC: 16 MHz; φIIC: 4 MHz)
16 MHz (fIIC) divided-by-4 = 4 MHz (φIIC)
4 MHz (φIIC) divided-by-8 and further divided-by-5 = 100 kbps (bit rate).
- In receive mode, ACK is returned for data other than the last data. NACK is returned after the last data is received.
- When receiving data, I²C-bus interrupt at the eighth clock (before the ACK clock): disabled
- Stop condition detection interrupt: enabled
- Timeout detection interrupt: disabled
- Set own slave address to the I2CSAR register.

While receiving data, if an interrupt is enabled at the eighth clock, ACK or NACK can be set after each byte of received data is checked.

4.1 Initial Settings

Follow the initial setting procedure below for 4.2 Master Transmission to 4.5 Slave Transmission.

- (1) Write own slave address to bits SAD6 to SAD0 in the I2CSAR register.
- (2) Write 85h to the I2CCR register (CCR value: 5, standard-mode selected, ACK clock generated).
- (3) Write 01h to the I2CCR2 register (φIIC: set bits ICK1 and ICK0 in the I2CCR1 register, timeout detector is disabled by the interrupt event).
- (4) Write 03h to the I2CCR1 register (φIIC: fIIC divided-by-2, successful receive interrupt is enabled and a stop condition detection interrupt is enabled).
- (5) Write 0Fh to the I2CSR register (transmit/receive mode: slave-receive mode).
- (6) Write 98h to the I2CSSCR register (SSC value: 18h; start condition/stop condition generating mode selection: long mode).
- (7) Write 08h to the I2CCR0 register (number of transmit/receive bits: 8, I²C-bus interface enabled, addressing format).

If the MCU uses a single-master system and the MCU itself is the master, start the initial setting procedures from step (2).

4.2 Master Transmission

Master transmission is described in this section. Programs (A) to (C) below refer to (A) to (C) in the following figure.

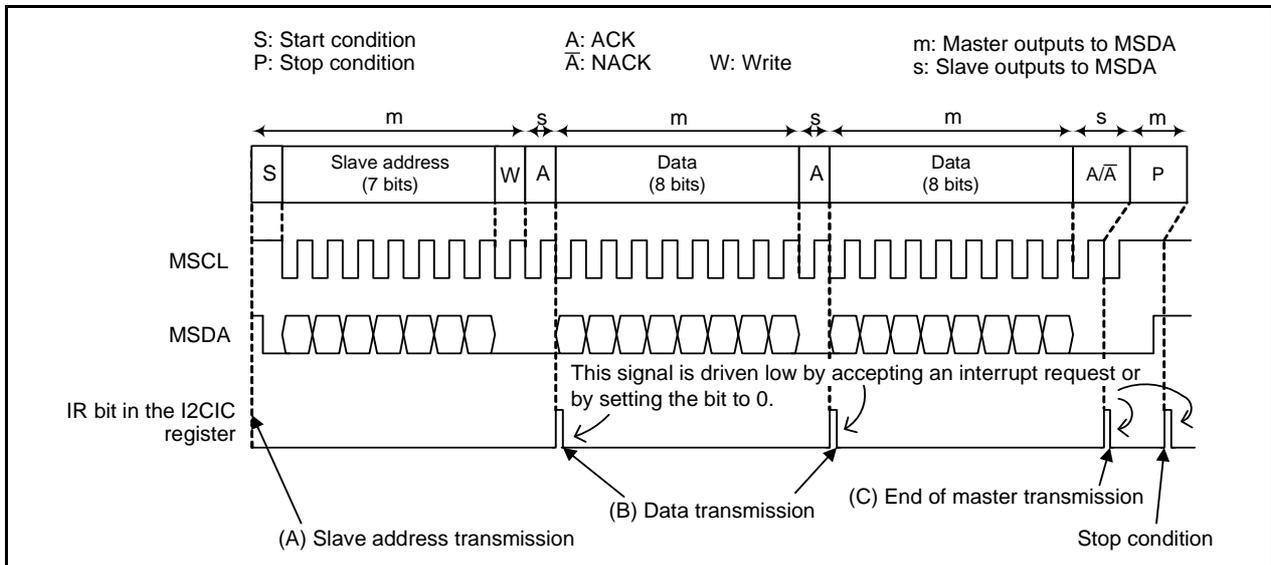


Figure 4.1 Example of Master Transmission

(A) Slave address transmission

- (1) The BBSY bit in the I2CSR register must be 0 (bus free).
- (2) Write E0h to the I2CSR register (start condition standby).
- (3) Write a slave address to the upper 7 bits and set the least significant bit (LSB) to 0 (start condition generated, then slave address transmitted).

After a stop condition is generated and the BBSY bit becomes 0, the I2CSR register is write disabled for 1.5 cycles of ϕ_{IIC} . Therefore, when writing E0h to the I2CSR register and a slave address to the I2CTRSR register, a start condition is not generated.

When generating a start condition immediately after the BBSY bit in the I2CSR register changes from 1 to 0, confirm that both the TRX and MST bits are 1 (transmission mode and master mode) after step (1), and then execute step (2).

(B) Data transmission (in the I²C-bus interrupt routine)

- (1) Write transmit data to the I2CTRSR register (data transmission).

(C) Completion of master transmission (in the I²C-bus interrupt routine)

- (1) Write C0h to the I2CSR register (stop condition standby).
- (2) Write dummy data to the I2CTRSR register (stop condition generated).

When the transmission is completed or ACK is not returned from the slave device (NACK returned), master transmission should be completed as shown in the example above.

4.3 Master Reception

Master reception is described in this section. Programs (A) to (D) below refer to (A) to (D) in the following figure.

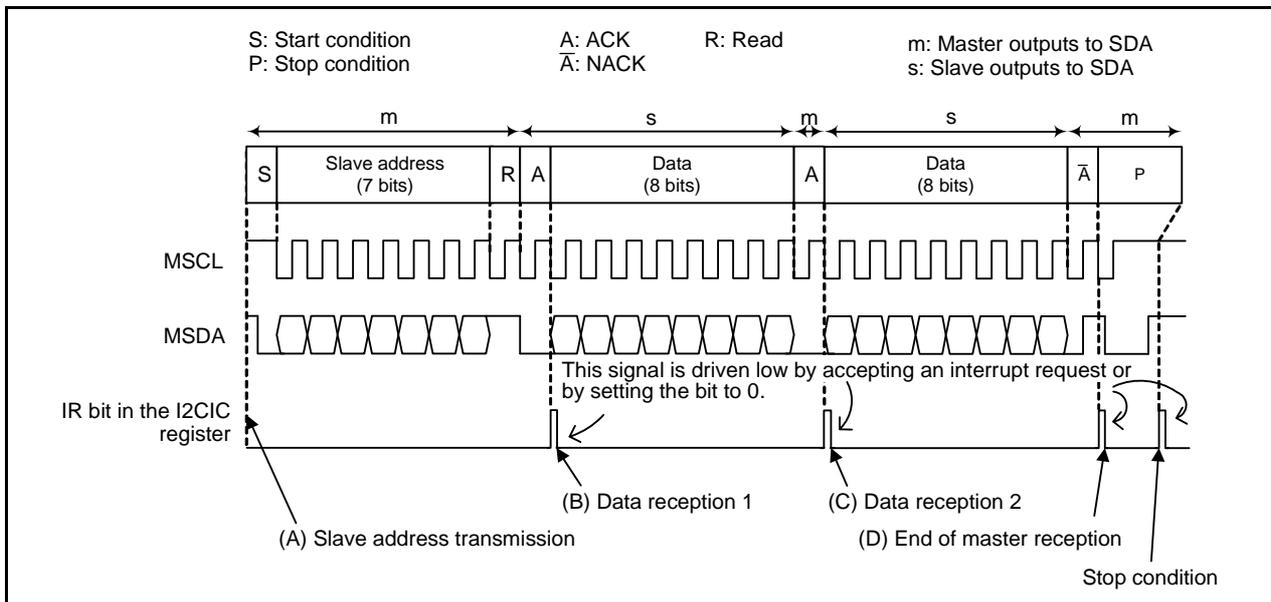


Figure 4.2 Example of Master Reception

(A) Slave address transmission

- (1) The BBSY bit in the I2CSR register must be 0 (bus free).
- (2) Write E0h to the I2CSR register (start condition standby).
- (3) Write a slave address to the upper 7 bits and set the least significant bit (LSB) to 1 (start condition generated, then slave address transmitted).

(B) Data reception 1 (after slave address transmission) (in the I²C-bus interrupt routine)

- (1) Write AFh to the I2CSR register (master receive mode).
- (2) Set the ACKD bit in the I2CCCR register to 0 (ACK sent) because the data is not the last one.
- (3) Write dummy data to the I2CTRSR register.

(C) Data reception 2 (data reception) (in the I²C-bus interrupt routine)

- (1) Read the received data from the I2CTRSR register.
- (2) Set the ACKD bit in the I2CCCR register to 1 (NACK sent) because the data is the last one.
- (3) Write dummy data to the I2CTRSR register.

(D) End of master reception (in the I²C-bus interrupt routine).

- (1) Read the received data from the I2CTRSR register.
- (2) Write C0h to the I2CSR register (stop condition standby state).
- (3) Write dummy data to the I2CTRSR register (stop condition generated).

4.4 Slave Reception

Slave reception is described in this section. Programs (A) to (C) below refer to (A) to (C) in the following diagram.

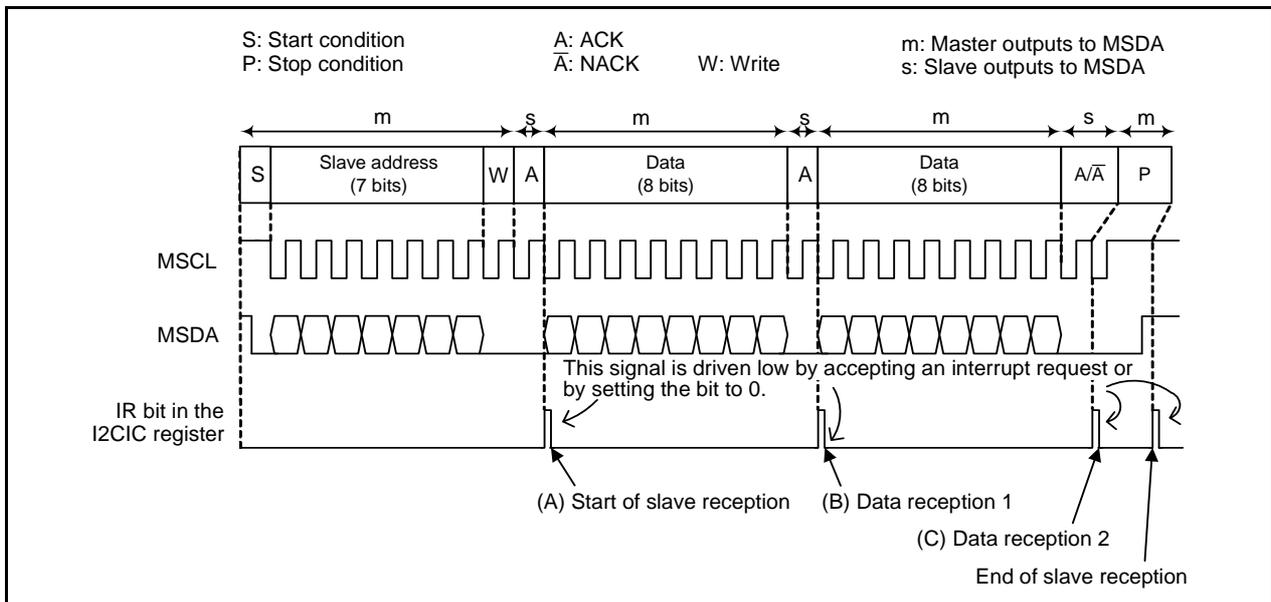


Figure 4.3 Example of Slave Reception

(A) Start of slave reception (in the I²C-bus interrupt routine)

- (1) Check the content of I2CSR register. When the TRS bit is 0, the I²C-bus interface is in slave receive mode.
- (2) Write dummy data to the I2CTRSR register.

(B) Data reception 1 (in the I²C-bus interrupt routine)

- (1) Read the received data from the I2CTRSR register.
- (2) Set the ACKD bit in the I2CCCR register to 0 (ACK sent) because the data is not the last one.
- (3) Write dummy data to the I2CTRSR register.

(C) Data reception 2 (in the I²C-bus interrupt routine)

- (1) Read the received data from the I2CTRSR register.
- (2) Set the ACKD bit in the I2CCCR register to 1 (NACK sent) because the data is the last one.
- (3) Write dummy data to the I2CTRSR register.

4.5 Slave Transmission

Slave transmission is described in this section. Programs (A) and (B) below refer to (A) and (B) in the following diagram.

When arbitration lost is detected, the TRS bit becomes 0 (receive mode) even when the bit after the slave address is 1 (read). Therefore, after arbitration lost is detected, read the I2CTRSR register. When bit 0 in the I2CTRSR register is 1, write 4Fh (slave transmit mode) to the I2CSR register and execute slave transmission.

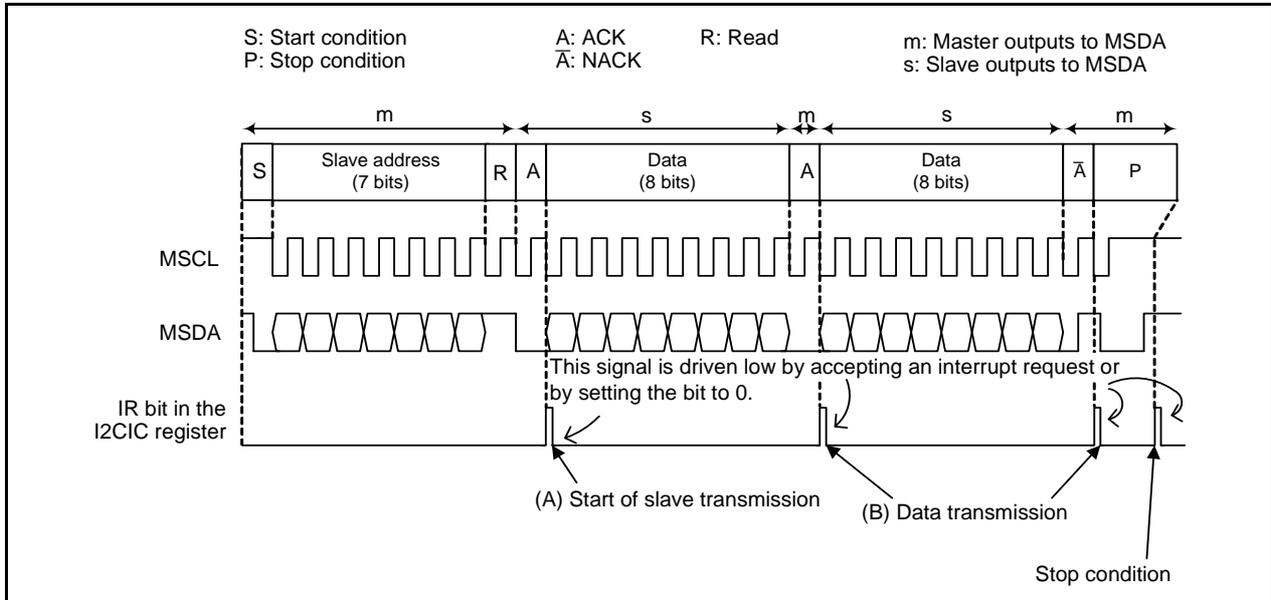


Figure 4.4 Example of Slave Transmission

(A) Start of slave transmission (in the I²C-bus interrupt routine)

- (1) Read the I2CSR register. When the TRS bit is 1, the I²C-bus interface is in slave transmit mode.
- (2) Write transmit data to the I2CTRSR register.

(B) Data transmission (in the I²C-bus interrupt routine)

- (1) Write transmit data to the I2CTRSR register.

Write dummy data to the I2CTRSR register even if an interrupt occurs at an ACK clock of the last transmit data. When the I2CTRSR register is written, the MSCL pin becomes high-impedance.

5. Arbitration Lost

The following describes the operation of the I²C-bus interface when arbitration lost occurs. Figure 5.1 shows the Operation Timing of the Arbitration Lost Detect Flag.

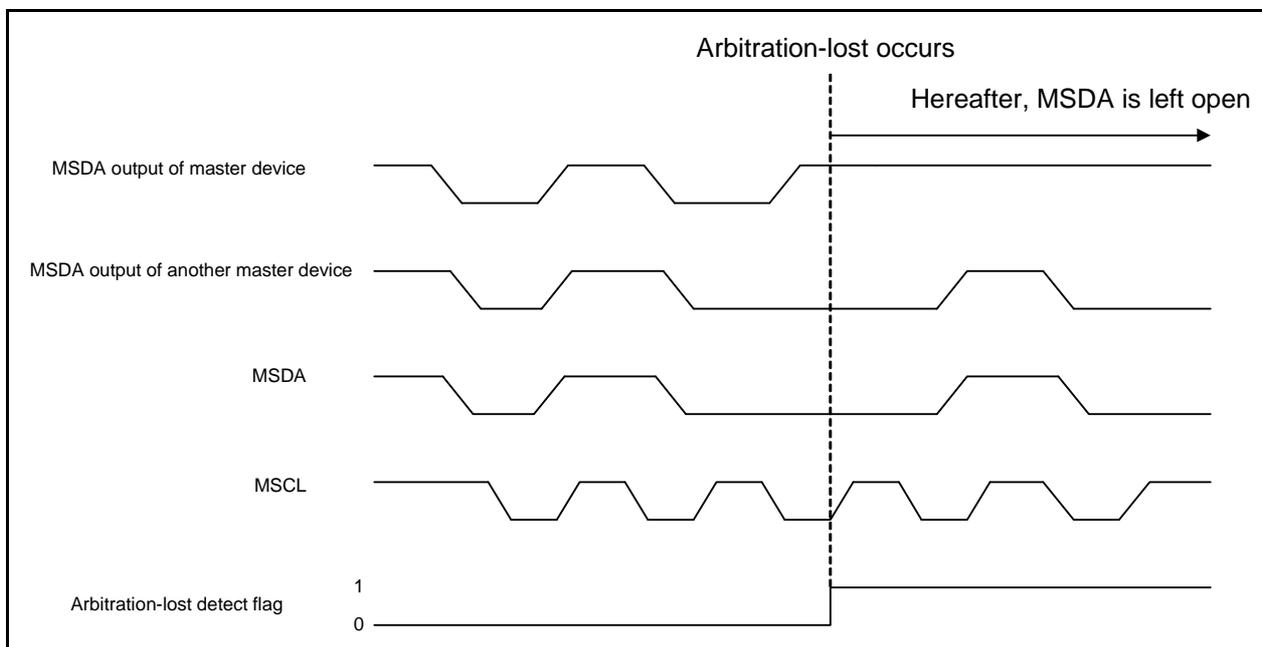


Figure 5.1 Operation Timing of the Arbitration Lost Detect Flag

When arbitration lost occurs, the arbitration lost detect flag becomes 1.

- (1) Arbitration lost occurs while transmitting a slave address.
When arbitration lost is detected, the communication mode automatically changes to slave reception, enabling the slave address to be received.
If the selected data format is the addressing format, the slave address can be resolved by reading the AAS bit in the I2CSR register.
- (2) Arbitration lost occurs while transmitting data following the slave address.
When arbitration lost is detected, the communication mode automatically changes to slave reception, enabling the data to be received.

6. Interrupts

The I²C-bus interface has the interrupt source listed below.

- (1) Interrupt when 9-bit transmission/reception is completed (including ACK/NACK)
The interrupt source can be determined by reading the RIE bit in the I2CCR1 register. When the RIE bit is 0, it is determined that the generated interrupt is attributable to this interrupt source.
- (2) Interrupt when 8 bits are received
Setting the RIE bit to 1 enables this interrupt source.
The interrupt source can be determined by reading the RIE bit. When the RIE bit is 1, it is determined that the generated interrupt is attributable to this interrupt source.
If no determination is made of ACK/NACK transmissions, there is no need to use this interrupt.
- (3) Interrupt when a stop condition is detected
Setting the STIE bit in the I2CCR1 register to 1 enables this interrupt source.
The interrupt source can be determined by reading the STOP bit in the I2CCR2 register. When a stop condition is detected, the STOP bit becomes 1.
- (4) Interrupt when the SCL clock is held high for a specified period of time during communication.
Setting the TOE bit in the I2CCR2 register to 1 enables this interrupt source.
The interrupt source can be determined by reading the TOF bit in the I2CCR2 register. When the MSCL clock remains high for more than a predetermined time during communication, the TOF bit becomes 1.

Figure 6.1 shows the I²C-bus Interface Interrupt Request Generation Timing.

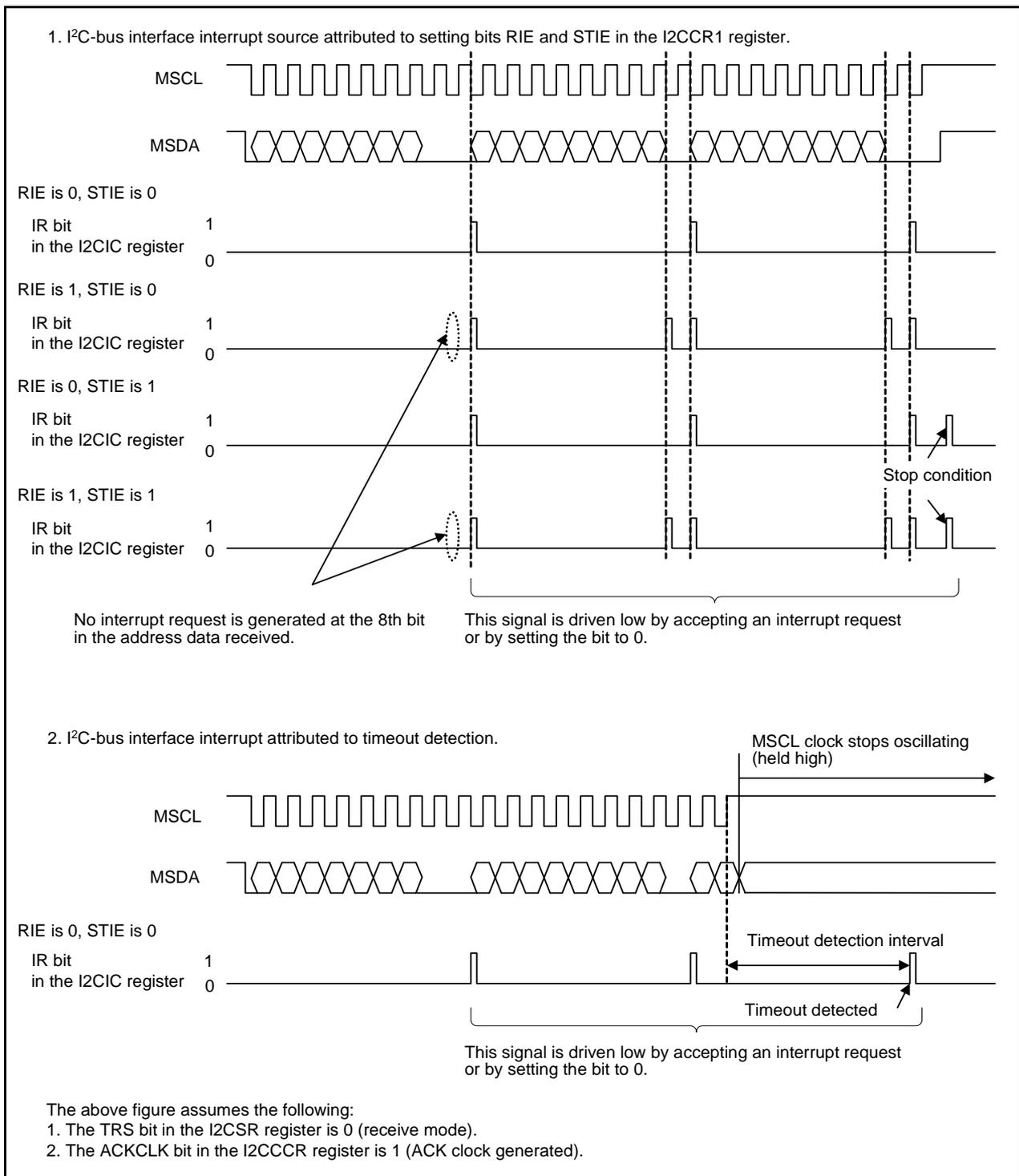


Figure 6.1 I²C-bus Interface Interrupt Request Generation Timing

7. Notes on I²C-bus Interface

7.1 Generating a Start Condition

After a stop condition is generated and the BBSY bit becomes 0 (bus free), the I2CSR register is write disabled for 1.5 cycles of ϕ IIC. Therefore, when writing E0h to the I2CSR register and a slave address to the I2CTRSR register, a start condition is not generated.

When generating a start condition immediately after the BBSY bit changes from 1 to 0, confirm that bits TRS and MST are both 1 after writing E0h in the I2CSR register, and then write a slave address to the I2CTRSR register.

8. Sample Program

8.1 Connection Example

Figure 8.1 shows a Connection Example.

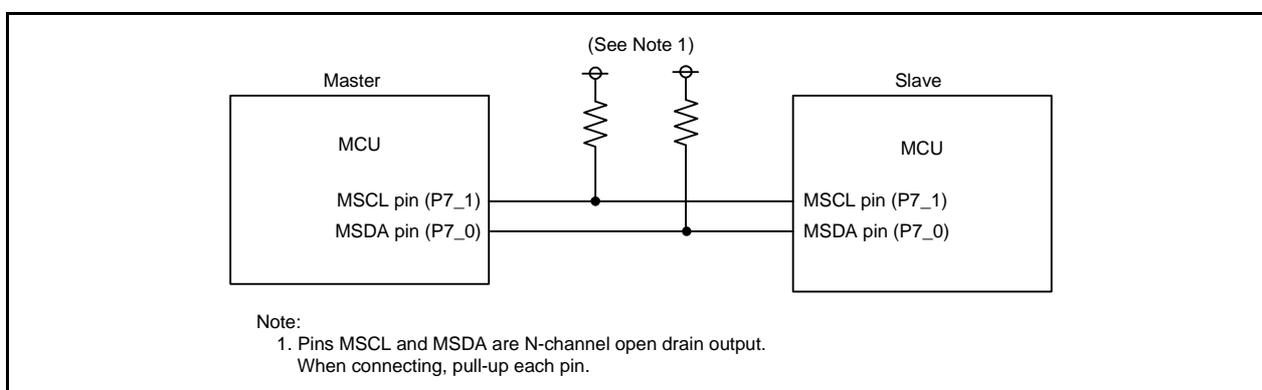


Figure 8.1 Connection Example

8.2 Operation Conditions

Table 8.1 lists the Sample Program Operation Conditions.

Table 8.1 Sample Program Operation Conditions

Item	Content
I ² C-bus interface clock (fIIC)	16 MHz (Xin: 16 MHz)
I ² C-bus system clock (ϕ IIC)	4 MHz (fIIC divided-by-5)
Bit rate	100 kbps (ϕ IIC divided-by-8 and further divided-by-5)
SCL mode	Standard-mode
Data format	Addressing format
Slave address compare	Only I2CSAR register enabled
Data receive interrupt	Enabled
Stop condition detect interrupt	Enabled
Timeout detector	Enabled

8.3 Setting Example

Four transmit/receive modes can be used in the sample program: master transmission, master reception, slave reception, and slave transmission. When calling the `mode_ini` function, the transmit/receive modes can be selected by setting arguments.

Set the other slave address and own slave address in the define declaration area in the sample program.

Figure 8.2 shows a Setting Example of Master Transmission. Figure 8.3 shows a Setting Example of Slave Address (0x09) and Own Slave Address (0x10).

```

/*"func comment"******/
/*  Main Program
/*"func comment end"******/
void main(void){

- Omitted -

/*=====*/
/*=  Modify start
/*=====*/

mode_ini(MASTER,SND);    /* First argument    */
                        /* MASTER : master  */
                        /* SLAVE  : slave   */
                        /* Second argument */
                        /* SND   : transfer */
                        /* REV   : receive  */

/*=====*/
/*=  Modify end
/*=====*/

```

Set the master (MASTER)/slave (SLAVE) as the first argument and send (SND)/receive (REV) as the second argument.

Figure 8.2 Transmit/Receive Mode Setting Example

```

/*******/
/*  DEFINE
/*******/
/*=====*/
/*=  Modify start
/*=====*/
#define SLAVE_ADD 0x09    /* Other slave address(7bit) */
#define SELF_ADD 0x10   /* My slave address(7bit) */

/*=====*/
/*=  Modify end
/*=====*/

```

Figure 8.3 Slave Address Setting Example

8.4 Operation Example

8.4.1 Master Transmission and Slave Reception

Figure 8.4 shows a Master Transmission and Slave Reception Operation Example.

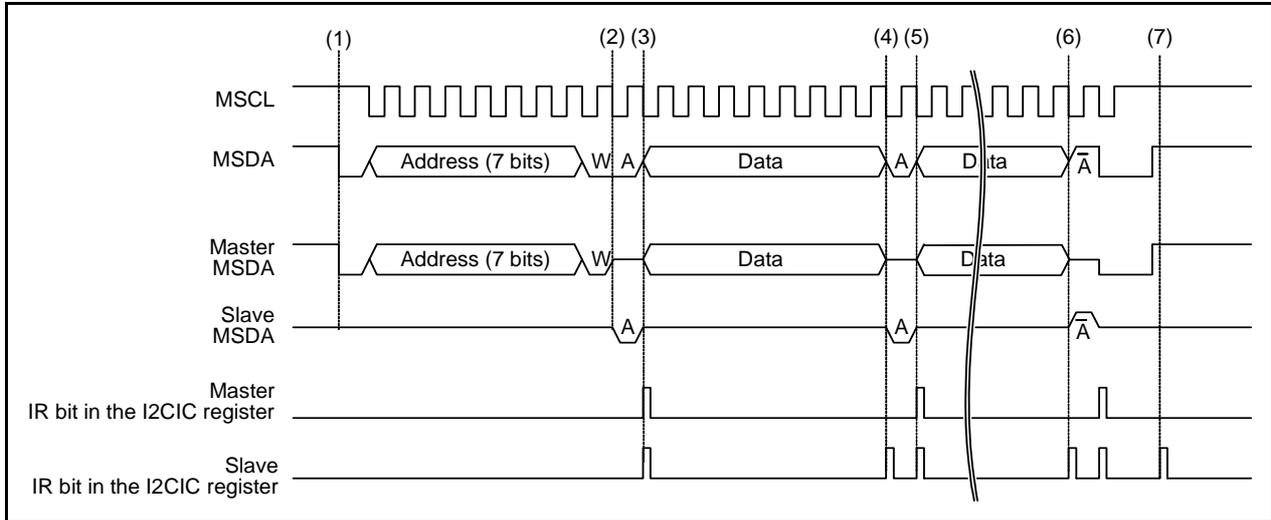


Figure 8.4 Master Transmission and Slave Reception Operation Example

- (1) Master: A start condition is generated after writing E0h to the I2CSR register and transmit data to the I2CTRSR register.
- (2) Master: The slave address set to bits b7 to b1 in the I2CTRSR register and the Write("0") set to b0 are output. Slave: ACK is output when a match is found between the received slave address and the value in the I2CSAR register.
- (3) Master: After ACK reception, the IR bit in the I2CIC register becomes 1. Slave: After ACK transmission, the IR bit becomes 1.
- (4) Slave: After data reception, the IR bit becomes 1. During interrupt handling, set the ACKD bit to 0 and ACK is output.
- (5) Master: After ACK reception, the IR bit becomes 1. Slave: After ACK transmission, the IR bit becomes 1.
- (6) Slave: After receiving 5 bytes, set the ACKD bit to 1 and NACK is output.
- (7) Master: A stop condition is generated. Slave: When detecting the stop condition, the IR bit becomes 1.

8.4.2 Master Reception and Slave Transmission

Figure 8.5 shows a Master Reception and Slave Transmission Operation Example.

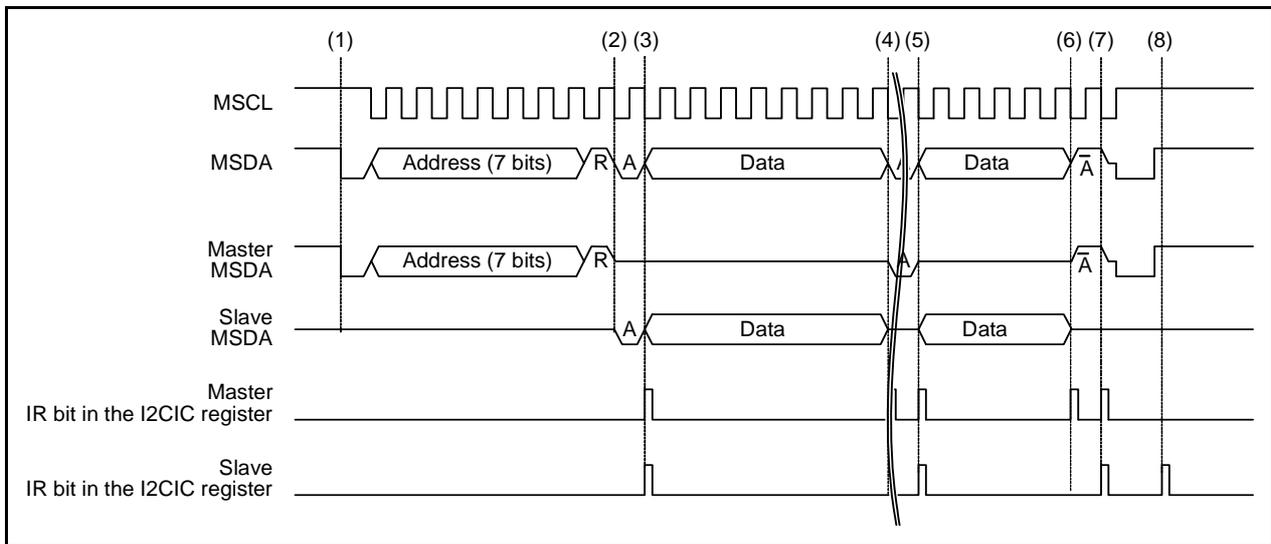


Figure 8.5 Master Reception and Slave Transmission Operation Example

- (1) Master: A start condition is generated after writing E0h to the I2CSR register and transmit data to the I2CTSR register.
- (2) Master: The slave address set to bits b7 to b1 in the I2CTSR register and Read("1") set to b0 are output.
Slave: ACK is output when a match is found between the received slave address and the I2CSAR register value.
The TRS bit in the I2CSR register becomes 1 (transmit mode) (only when the ALS bit in the I2CCR0 register is 1 (addressing mode)).
- (3) Master: After ACK reception, the IR bit in the I2CIC register becomes 1.
Slave: After ACK transmission, the IR bit becomes 1.
- (4) Slave: After data reception, the IR bit becomes 1. During interrupt handling, set the ACKD bit to 0 and ACK is output.
- (5) Master: After ACK transmission, the IR bit becomes 1.
Slave: After ACK reception, the IR bit becomes 1.
- (6) Slave: After receiving 5 bytes, set the ACKD bit to 1 and NACK is output.
- (7) Slave: After receiving NACK, the TRS bit becomes 0 (receive mode) only when the AAS bit is 1.
- (8) Master: A stop condition is generated.
Slave: When detecting the stop condition, the IR bit becomes 1.

8.5 Function Tables

Declaration	void iic_ini(unsigned char ini, unsigned char sub_address)	
Outline	I ² C-bus initialization function	
Argument	Argument name	Meaning
	ini	I ² C-bus function enabled/disabled ENABLED: I ² C-bus function enabled DISABLED: I ² C-bus function disabled
	sub_address	Slave address setting
Variable (global)	Variable name	Content
	iic_mode	For selecting transmit/receive modes
	iic_index	For the number of transfers
Returned value	None	
Function	Argument ini = When ENABLED (I ² C-bus function enabled), initialize the I ² C-bus before enabling interrupts. Argument ini = When DISABLED (I ² C-bus function disabled), disable the I ² C-bus interface and the I ² C-bus interrupt.	

Declaration	void mode_ini(unsigned char ms, unsigned char sr)	
Outline	Function for setting respective transmit/receive modes	
Argument	Argument name	Meaning
	ms	Select master or slave MASTER: Master SLAVE: Slave
		sr
	Variable name	
Variable (global)	iic_ram[]	Data storage alignment for master transmit
	iic_length	For transmit and receive size
Returned value	None	
Function	Set the respective transmit/receive modes.	

Declaration	unsigned char iic_master_start(unsigned char slave, unsigned char sr, unsigned char *buf, unsigned char len)	
Outline	Master start function	
Argument	Argument name	Meaning
	slave	Specified slave address (0x00 to 0x7f)
	sr	Select transmission or reception
		SND: Transmission mode REV: Reception mode
	*buf	Pointer for transmit buffer
len	Transmit/receive data size (0x00 to 0xff)	
Variable (global)	Variable name	Content
	iic_slave	Variable for storing slave address
	iic_length	For transmit and receive size
	iic_pointer	Pointer for transmission buffer
	iic_mode	For selecting transmit/receive modes
Returned value	Type	Meaning
	unsigned char	Master start failure/start successful
		FALSE: Master start failure TRUE: Master start successful
Function	Transmit the start condition and slave address after master setting.	

Declaration	void master_transfer(void)	
Outline	Master transmit function	
Argument	None	
Variable (global)	Variable name	Content
	iic_mode	For selecting transmit/receive modes
	iic_length	For transmit and receive size
	iic_pointer	Transmit buffer pointer
Returned value	None	
Function	Detect arbitration lost, confirming ACK/NACK reception, and transmitting data.	

Declaration	void master_receive(void)	
Outline	Master receive function	
Argument	None	
Variable (global)	Variable name	Content
	iic_mode	For selecting transmit/receive modes
	iic_length	For transmit and receive size
	iic_pointer	Receive buffer pointer
Returned value	None	
Function	Detecting arbitration lost, transmitting ACK/NACK, and receiving data.	

Declaration	void slave_receive(void)	
Outline	Slave receive function	
Argument	None	
Variable (global)	Variable name	Content
	iic_index	For the number of transfers
	iic_length	For transmit and receive size
	iic_pointer	Transmit buffer pointer
Returned value	None	
Function	Receive data and transmit ACK/NACK.	

Declaration	void slave_transfer(void)	
Outline	Slave transmit function	
Argument	None	
Variable (global)	Variable name	Content
	iic_index	For the number of transfers
	iic_pointer	Transmit buffer pointer
Returned value	None	
Function	Transmit data and receive ACK/NACK.	

Declaration	void idle_mode(void)	
Outline	Transmit and receive mode select function	
Argument	None	
Variable (global)	Variable name	Content
	iic_mode	For selecting transmit/receive modes
Returned value	None	
Function	Select transmit mode or receive mode when receiving data.	

Declaration	unsigned char* select_buffer(unsigned char RW)	
Outline	Function for obtaining transmit and receive buffer addresses	
Argument	Variable name	Meaning
	RW	Select transmit and receive buffer
		0: Slave receive buffer 1: Slave transmit buffer
Variable (global)	None	
Returned value	Type	Meaning
	unsigned char*	Transmit and receive buffer address
Function	Obtain transmit and receive buffer addresses.	

Declaration	void receive_stop_condition(void)	
Outline	Stop condition reception state processing function	
Argument	None	
Variable (global)	Variable name	Content
	iic_mode	For selecting transmit/receive modes
	iic_length	Number of transfers
	iic_index	For the number of transfers
Returned value	None	
Function	Clear the stop condition detection interrupt request bit and initialize the transmit/receive mode.	

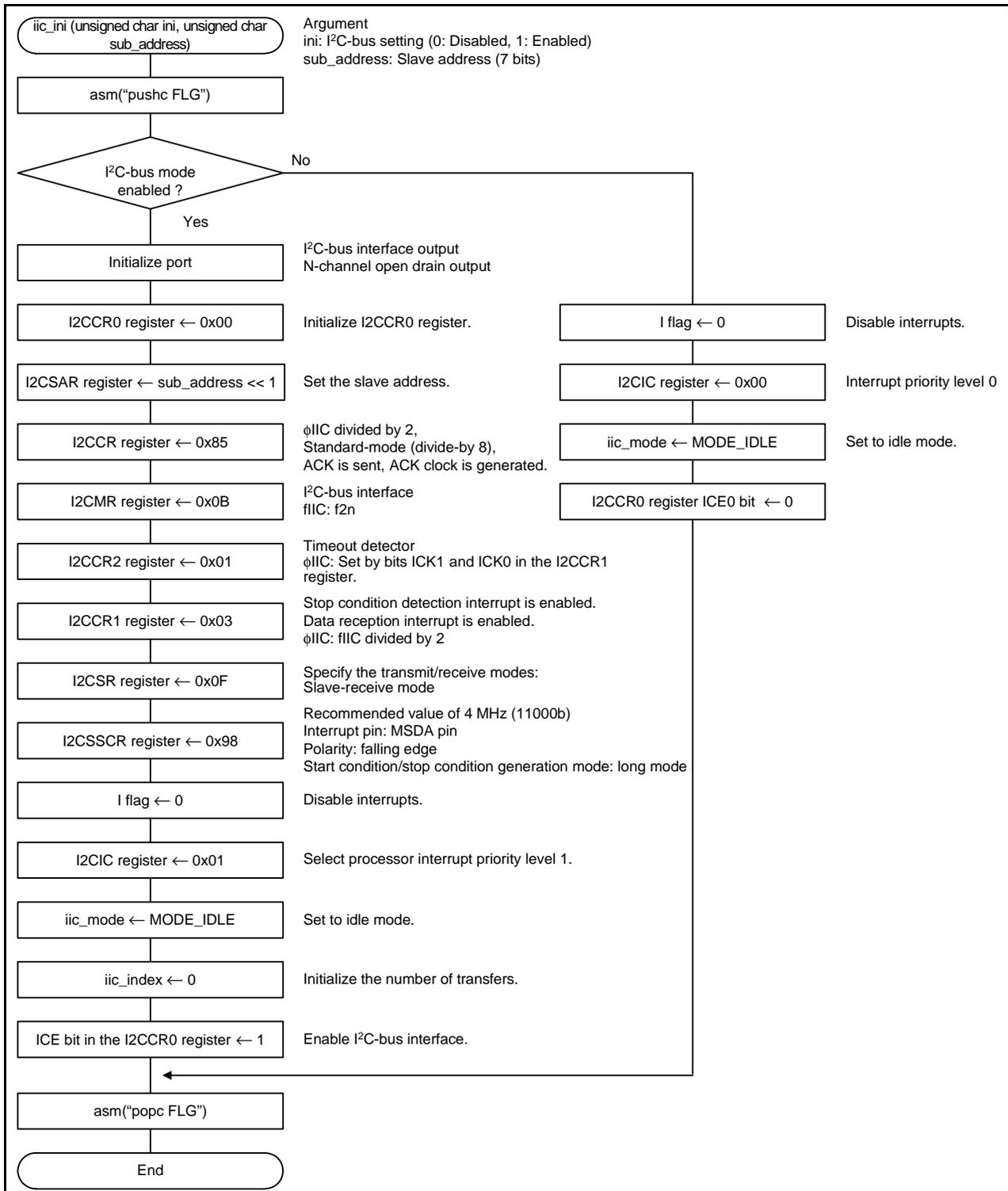
Declaration	void iic_master_end(unsigned char status)	
Outline	Master control completion function	
Argument	Argument name	Meaning
	status	Status after master control 0x10: Master transmission completed 0x11: Arbitration lost is detected during master transmission. 0x12: NACK is received during master transmission 0x20: Master reception completed 0x21: Arbitration lost is detected during master reception. 0x22: NACK is received during master reception
Variable (global)	None	
Returned value	None	
Function	Carry out the processing after master control is completed. This application note does not include any processing. Add if the need arises.	

Declaration	void iic_slave_end(unsigned char status)	
Outline	Slave control completion function	
Argument	Argument name	Meaning
	status	Status after slave control completed 0x10: Slave transmission completed
Variable (global)	None	
Returned value	None	
Function	Carry out the processing after slave control is completed. This application note does not include any processing. Add if the need arises.	

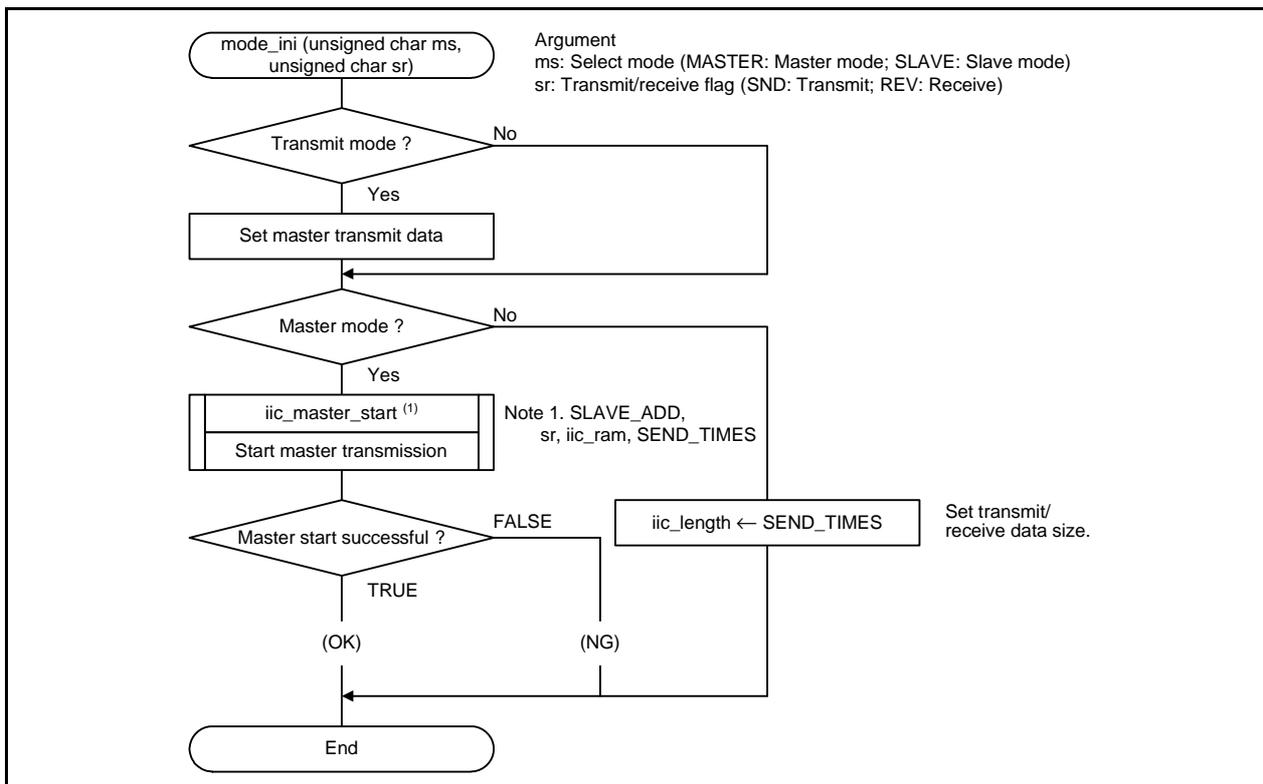
Declaration	void stop_condition(void)	
Outline	Stop condition generation function	
Argument	None	
Variable (global)	None	
Returned value	None	
Function	A stop condition is generated.	

8.6 Flowcharts

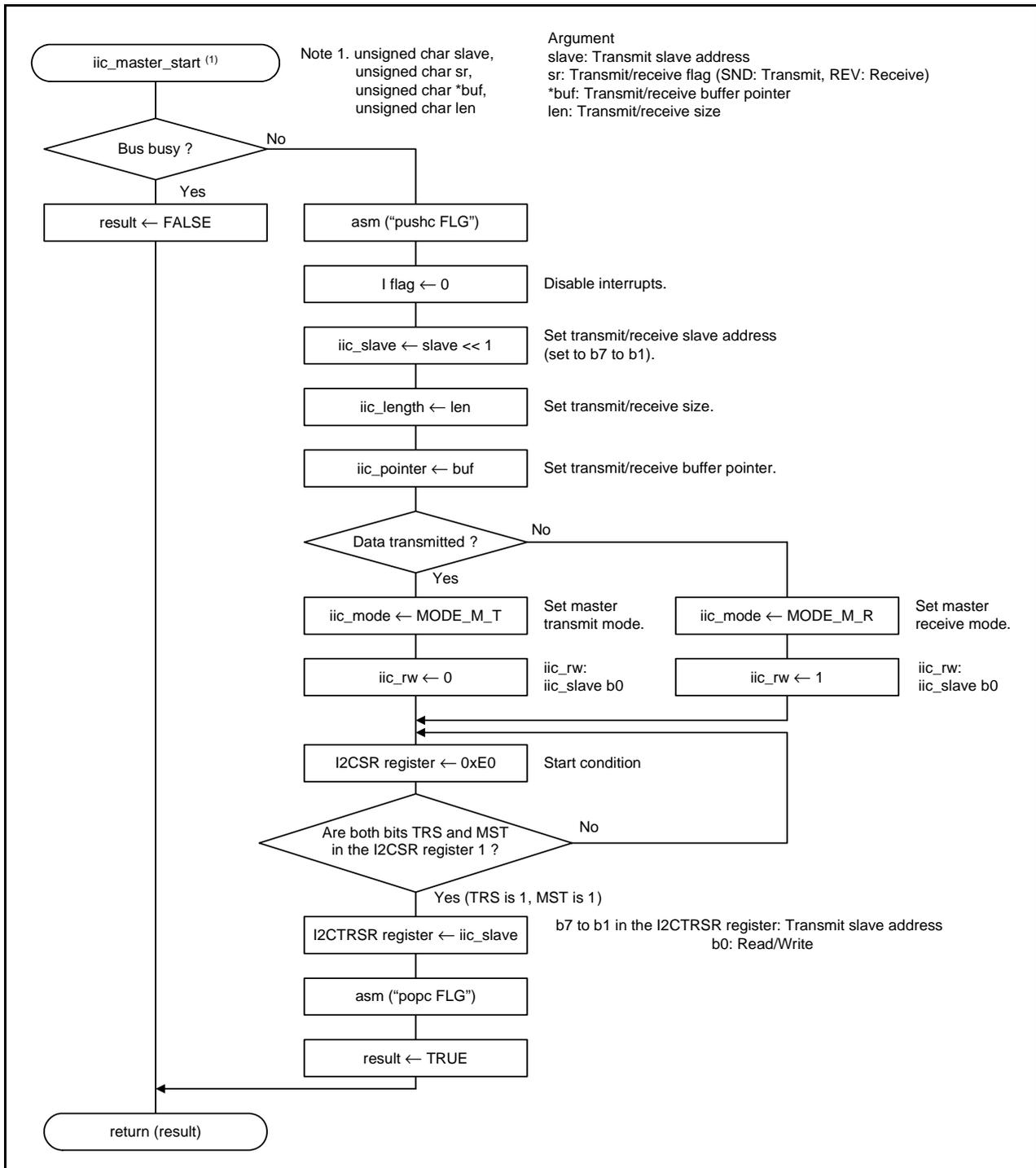
8.6.1 I²C-bus Initialization Function



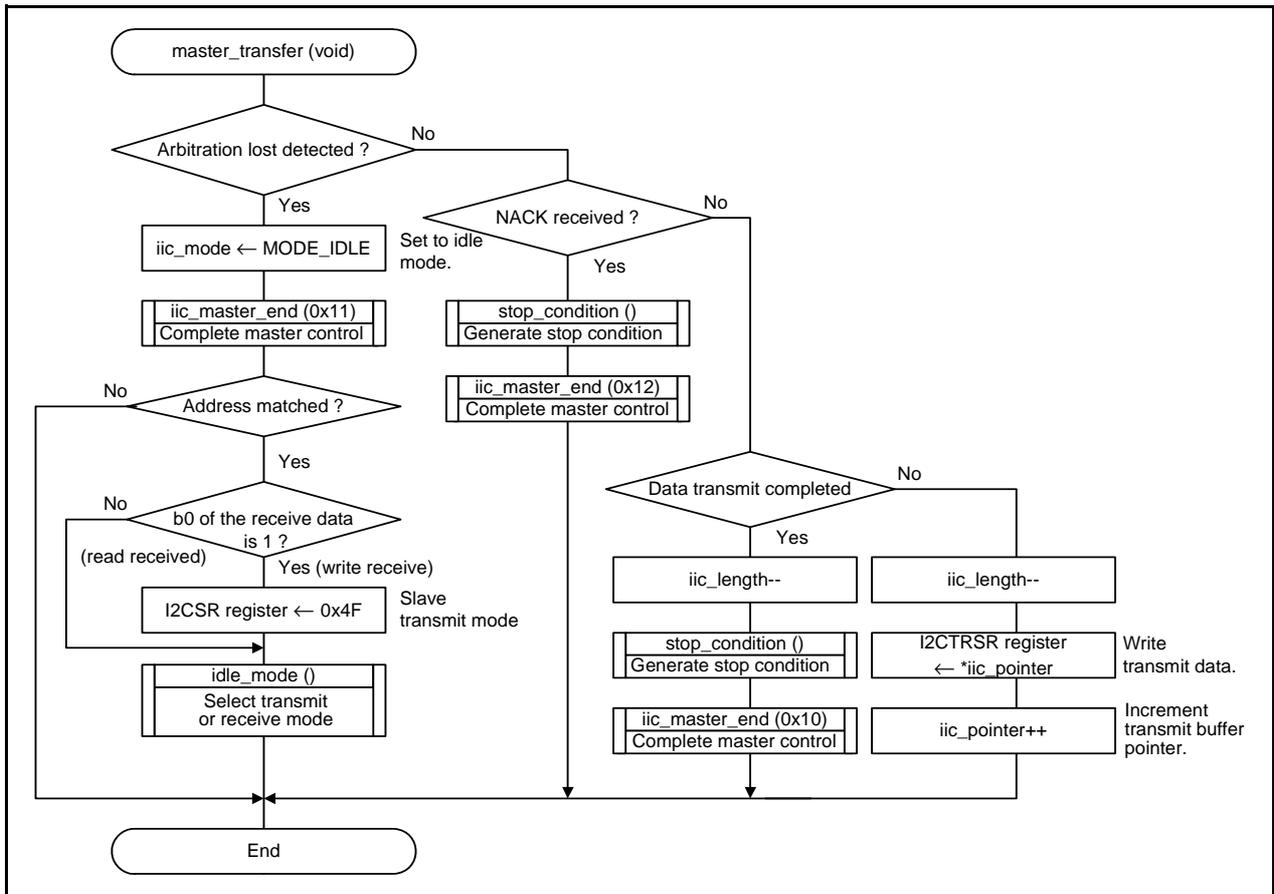
8.6.2 Function for Setting Respective Transmit/Receive Modes



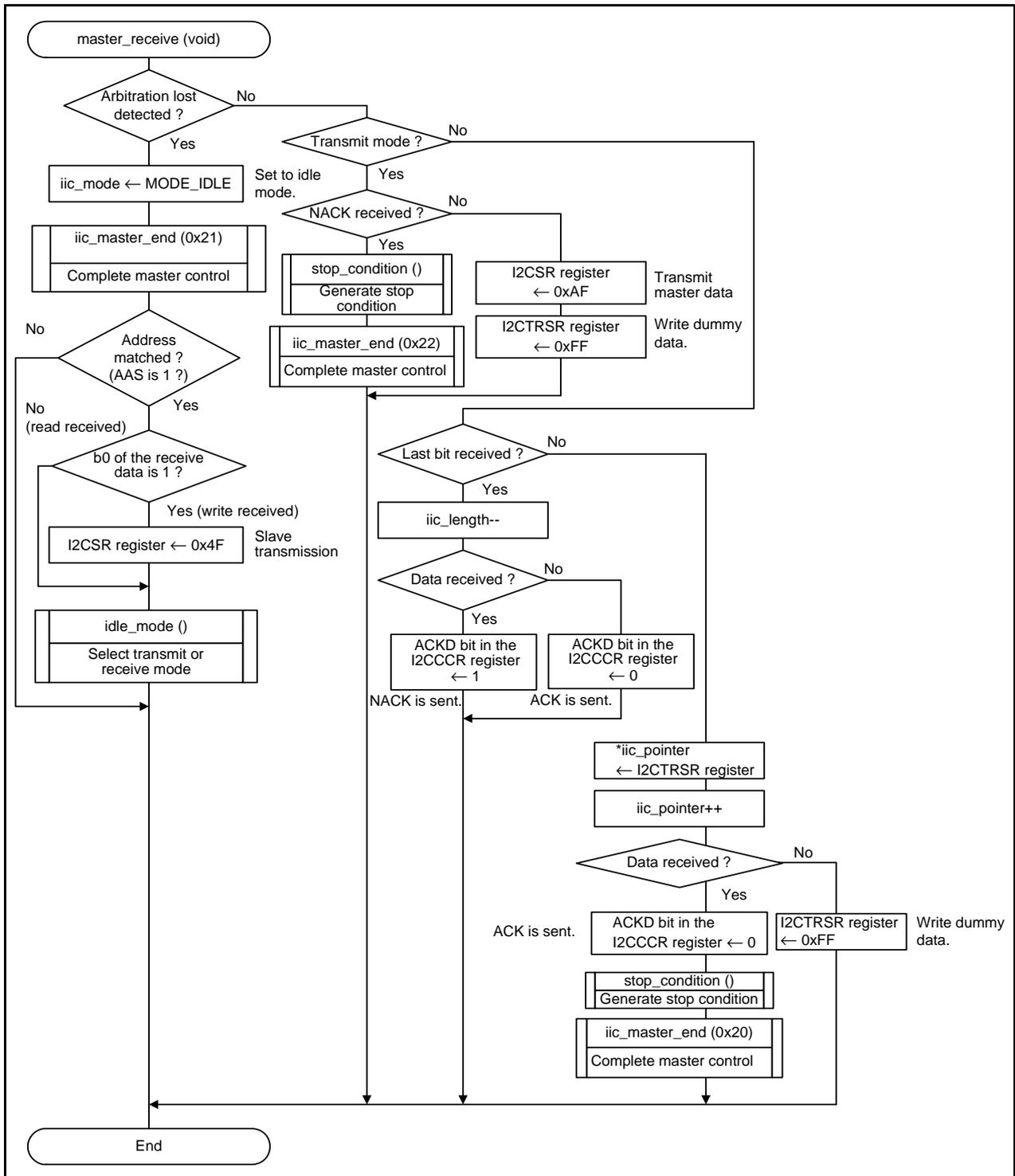
8.6.3 Master Start Function



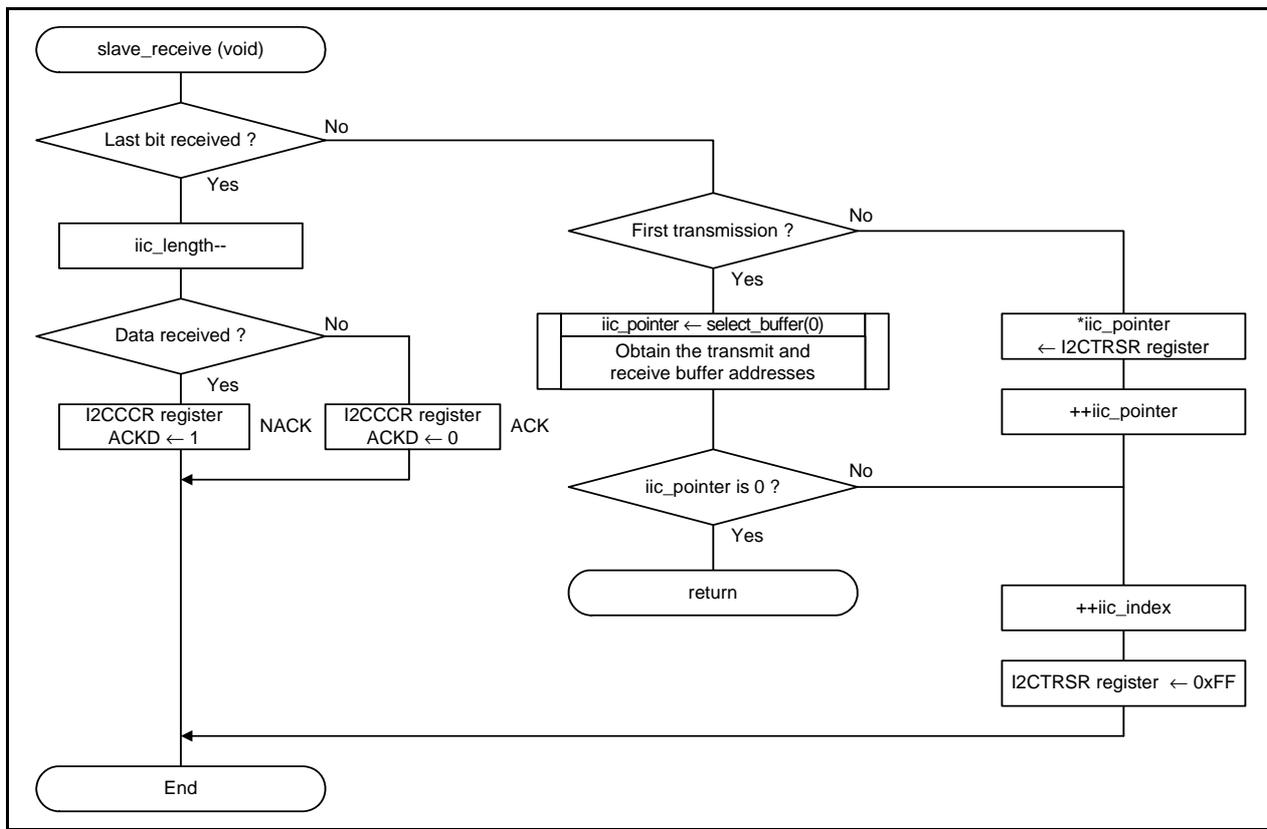
8.6.4 Master Transmit Function



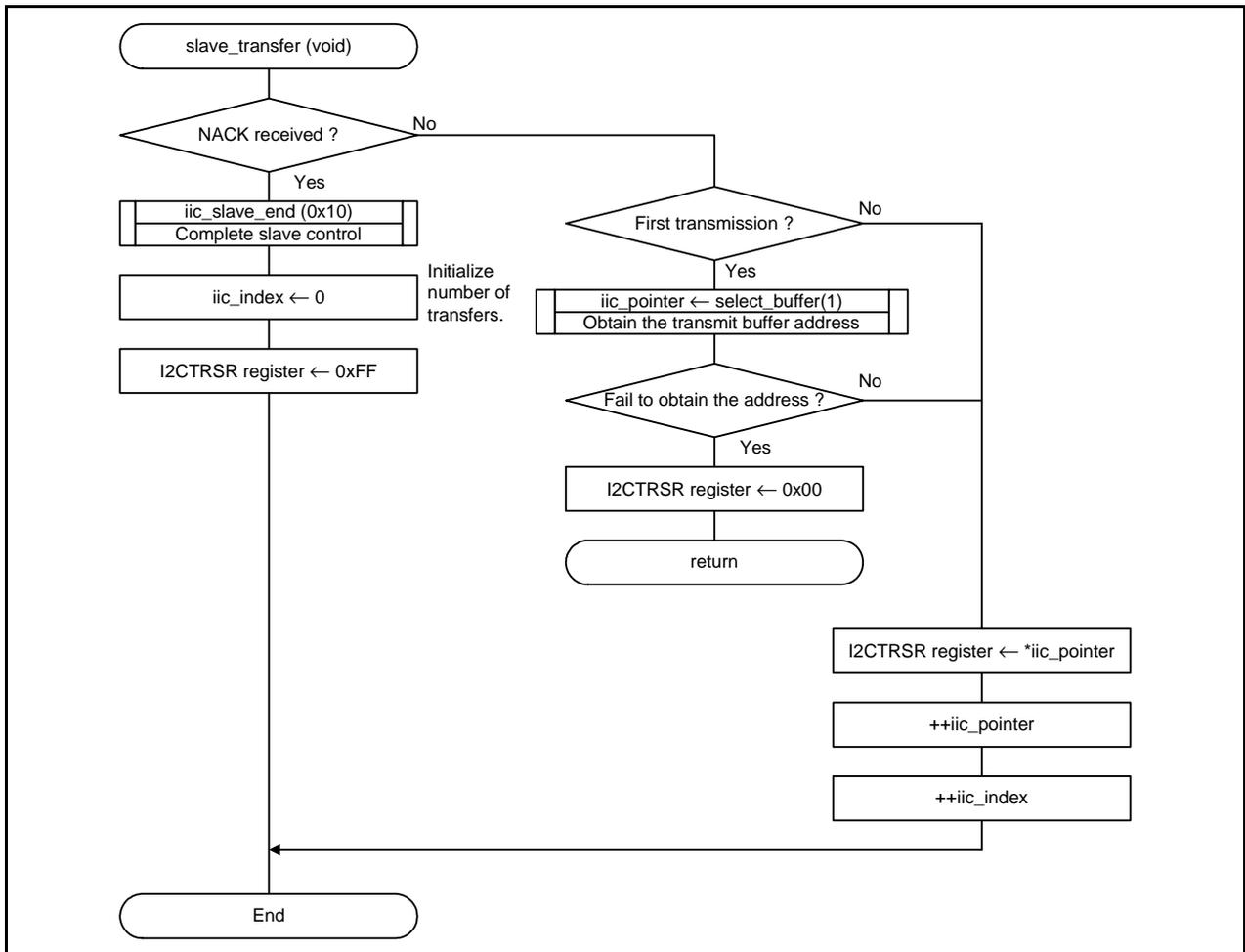
8.6.5 Master Receive Function



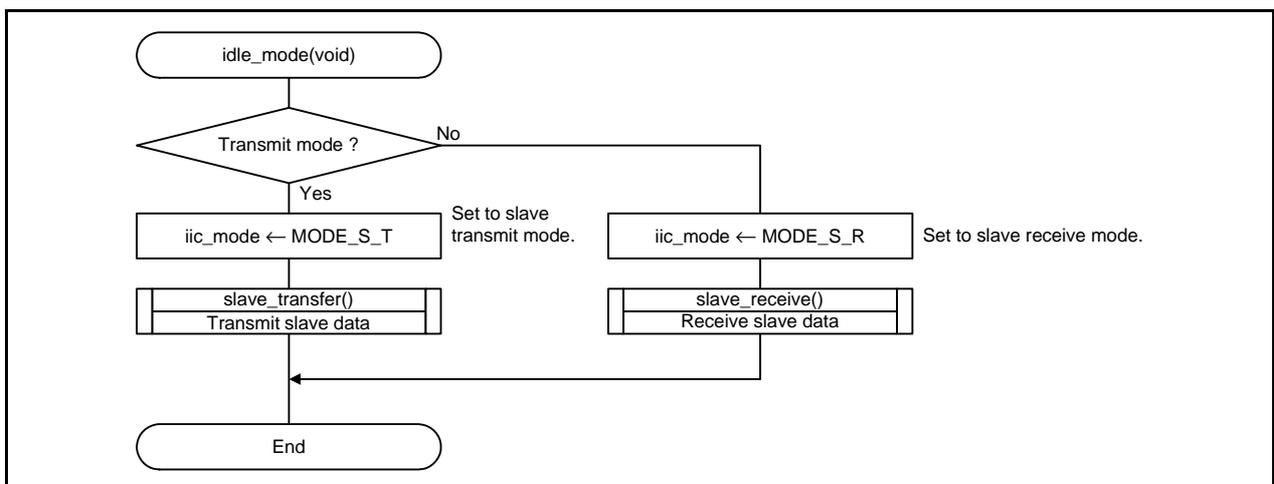
8.6.6 Slave Receive Function



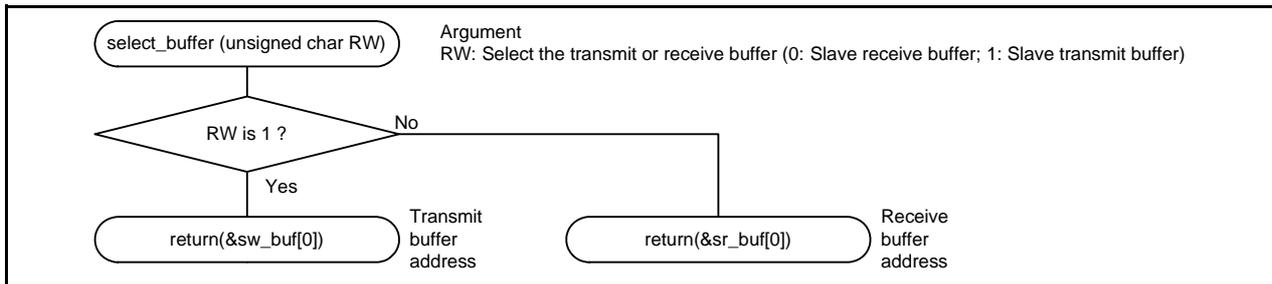
8.6.7 Slave Transmit Function



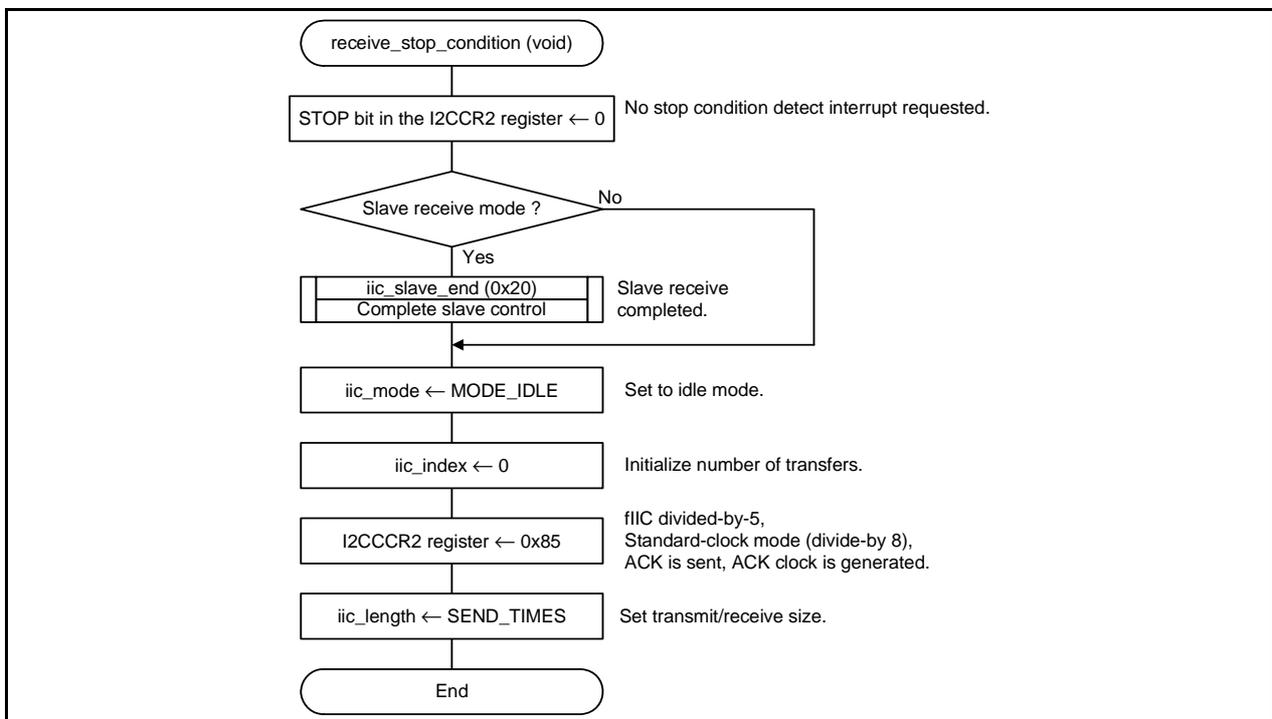
8.6.8 Transmit and Receive Mode Select Function



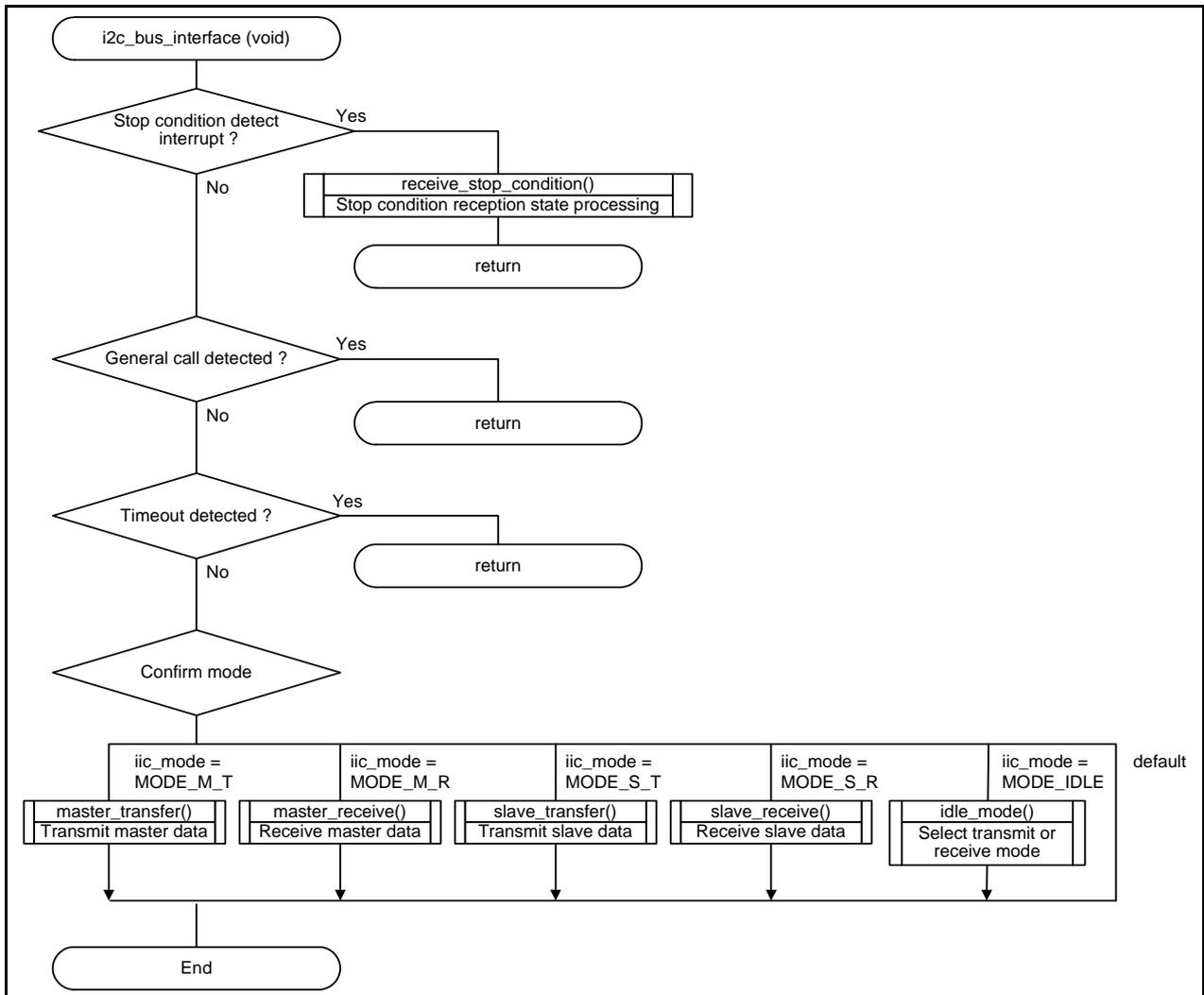
8.6.9 Function for Obtaining Transmit and Receive Buffer Addresses



8.6.10 Stop Condition Reception State Processing Function



8.6.11 I²C-bus Interface Interrupt Handling



9. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

10. Reference Documents

User's Manuals

R32C/118 Group User's Manual: Hardware Rev.1.00

R32C/117 Group User's Manual: Hardware Rev.1.00

R32C/116 Group User's Manual: Hardware Rev.1.00

R32C/118A Group User's Manual: Hardware Rev.1.00

R32C/117A Group User's Manual: Hardware Rev.1.00

R32C/116A Group User's Manual: Hardware Rev.1.00

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual

R32C/100 Series C Compiler Package V.1.02 C Compiler User's Manual Rev.2.00

The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website

<http://www.renesas.com/>

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REVISION HISTORY	R32C/116, 117, 118, 116A, 117A, and 118A Groups Multi-Master I ² C-bus Interface
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Rev.	Date	Description	
		Page	Summary
1.00	Aug 2, 2010	-	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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