

RL78/L13, RL78/L23

Migration Guide from RL78/L13 to RL78/L23

Introduction

This application note describes the functional differences that have been updated from the conventional RL78/L13 LCD microcontrollers in the RL78/L23 microcontrollers, and explains the points to note when replacing them.

Target Device

RL78/L13, RL78/L23

For detailed information on peripheral functions and electrical characteristics, refer to the User's Manual: Hardware and Technical Updates.

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1. Differences Summary

1.1 Function Difference

Table 1.1 shows the differences between the RL78/L23 and RL78/L13 functions. All functions are the same or upgraded. However, even if it is a register with the same name for a peripheral function with the same name, the bit format has been changed. Therefore, the ROM code developed for the RL78/L13 cannot be used with the RL78/L23. Points to note when migrating each function are shown in Chapter 2.

Table 1.1 Feature summary differences (1/2)

Item	RL78/L13	RL78/L23	Remarks
Power supply voltage	1.6~5.5V	←	
Operating ambient temperature	-40~105°C	←	
Package	64pins/80pins	44/48/52/64/80/100 Pins	
CPU core	S2 core	S3 core	S3 is upward compatible with S2 Multiply and Divid Instruction Extension
Operation clock	Max 24MHz TMKB is 48MHz	Max 32MHz TMKB is 64MHz	MOCO added : 4MHz/2MHz/1MHz LOCO : Change from 15 kHz to 32.768 kHz
Code Flash/ Data Flash	16KB to 128KB/ 4KB	64KB to 512KB/ 8KB	Variable boot area and dual-bank rewrite function correspondence
Ports	↳	Function enhanced	Added output current control port and 40-mA output ports
Switching the Flash Operating Mode	—	Operation State Control	Operating mode can be changed on the SW
Data Transfer function	DMA 4ch	DTC 24ch	Upgrade from DMA to DTC
Timer Array Unit	8ch	8ch	Added input from ELCL, Change input from fIL from ch3 to ch5
Realtime Clock	1ch	1ch	A 500ms output is available separately from the INTRTC for LCD flashing
Interval Timer	12-bit 1ch	32-bit 1ch + 8-bit 8ch to 16ch	Long-term support and additional number of channels
16-bit Timer KB	1ch	3ch	IH 3-channel output enabled. Operating frequency increase from 48MHz to 64MHz.
Timer RJ	—	2ch	Added a new generic timer
External Signal Sampler	—	1unit	Generates a sampling clock signal based on the timing of generation of the 8-bit interval timer
Clock Output/Buzzer Output Controller	1ch	←	
Watchdog Timer (WDT)	1ch	←	fIL changed from 15 kHz to 32.768 kHz Changed the Overflow Time

Note : New peripheral functions : Changed peripheral functions

—: There is no corresponding function.

Table 1.2 Feature summary differences (2/2)

Item	RL78/L13	RL78/L23	Remarks
A/D Converter	10-bit 9~12ch	12-bit 8 to 13ch	12 bits higher resolution
D/A Converter	—	3ch	
Comparator	2ch	←	Added D/A input path
Serial array unit	CSI:2ch UART:3~4ch Simplified I2C : 2ch	CSI : 5~8ch UART:3~4ch Simplified IIC : 6~8ch	Added UART loopback function
IICA(I2C)	2ch	←	Added all addresses match function
UARTA	—	1ch	UART capable of fSUB operation
LCD Controller/Driver	36 to 51segx4com 32 to 47segx8com	19 to 56segx4com 17 to 54segx6com 15 to 52segx8com	Added VL2 reference internal boost method and VL4 reference capacitance split method 6 common time slice output possible Blinking timing can be changed
Multiplier And Divider/ Multiply-Accumulate	MULTIPLIER AND DIVIDER/MULTIPLY-ACCUMULATE	CPU instruction	
Logic and event link controller(ELCL)	—	1unit	Arbitrarily connect peripheral inputs and outputs and pins with logic circuits
Interrupt Function	External 9ch Internal 32 to 35ch	External 9ch, Internal 47~52ch	Changing the interrupt factor due to differences in installed functions Increase alternative INTP number
Key Interrupt	5 to 8ch	2 to 8ch	
Standby function	↳	Function enhanced	Added HOCO High-speed wakeup and RAM shutdown mode.
Reset Function	↳	←	
Voltage Detector	1ch	2ch	Changed detection voltage
Safety Function	↳	Function enhanced	Added Flash memory guard function and UART loopback function
Security Function encryption	Flash rewriting prohibit function Flash shield window function	Function enhanced	Add True Random Number Generator, Customer ID and Unique ID function
SNOOZE Mode Sequencer (SMS)	—	New function	sequencer can process independently of the CPU
Capacitive Sensing Unit (CTS2La)	—	16 to 36ch	Capacitance measurement function of capacitive sensors
Regulator	1.8V and 2.1V	1.5V	Changed REGC voltage
Option Bytes	↳	Function enhanced	Changed WDT, LVD and Flah operation mode, Variable boot area function
On-chip Debugging	↳	←	Changed Supported Emulators 2-wire OCD Supported
BCD Correction circuit	↳	←	

Note : New peripheral functions : Changed peripheral functions

—: There is no corresponding function.

1.2 Pin function Difference

The RL78/L23 has a pin function similar to that of the RL78/L13, but there are some differences, so please check the table below for the pin functions used.

Table 1.3 Pin function Comparison of 64pin Products (1)

No	RL78/L13	RL78/L23
1	P45/IVREF0	P45/IVREF0/TxDA2 [‡] /SCK30/SCL30/EXSDO0
2	P44/IVCMP0/(SCK10)/(SCL10)	P44/IVCMP0/RxDA2 [‡] /SI30/SDA30/RxD3/EXSDO1/(TI04)/(TO04)/(INTP7)/(SCK11)/(SCL11)
3	P43/IVCMP1/(INTP7)/(SI10)/(RxD1)/(SDA10)	P43/IVCMP1/SO30/TxD3/(TI05)/(TO05)/(INTP4)/(RxDA1)/(SI11)/(SDA11)
4	P42/IVREF1/TI05/TO05/(SO10)/(TxD1)	P42/TI05/TO05/IVREF1/TRJO0/(INTP7)/(TxD1)/(SDA00)/(SO11)/(PCLBUZ1)
5	P40/TOOL0/(TI00)/(TO00)	P40/TOOL0/(TI00)/(TO00)/(SCL00)
6	RESET	RESET
7	P124/XT2/EXCLKS	P124/XT2/EXCLKS
8	P123/XT1	P123/XT1
9	P137/INTP0	P137/EI137/INTP0
10	P122/X2/EXCLK	P122/X2/EXCLK/EI122
11	P121/X1	P121/X1/VBAT0/EI121
12	REGC	REGC
13	VSS	VSS
14	VDD	VDD
15	P60/SCLA0/(TI01)/(TO01)	P60/SCLA0/(TI01)/(TO01)/CCD04/EO60/(INTP3)
16	P61/SDAA0/(TI02)/(TO02)	P61/SDAA0/(TI02)/(TO02)/CCD05/EO61/(INTP4)
17	P127/CAPH/(TI03)/(TO03)/(REMOOUT)	P62/SCLA1/CCD06/(TI03)/(TO03)/(REMOOUT)/(INTP5)
18	P126/CAPL/(TI04)/(TO04)	P63/SDAA1/CCD07/(TI04)/(TO04)/(INTP6)
19	VL1	P127/CAPH/TS00/(TI03)/(TO03)/(REMOOUT)
20	VL2	P126/CAPL/TS01/(TI04)/(TO04)/(INTP4)
21	VL4	P87/VL1/(TxD1)/(SO10)
22	P125/VL3/TI06/TO06	P86/VL2/(TI06)/(TO06)/(INTP3)/(RxD1)/(SI10)/(SDA10)/(PCLBUZ1)
23	P33/INTP4/SEG23	P85/VL4/(VCOUT0)/(INTP4)/(SCK10)/(SCL10)/(SCL30)
24	P32/SEG22/TI01/TO01	P125/VL3/TS02/(TI06)/(TO06)/(VCOUT1)/(INTP7)/(SDA30)/(PCLBUZ1)
25	P31/INTP3/SEG21/RTC1HZ	P31/INTP3/RTC1HZ/SEG21/TS07/(TI01)/(TO01)
26	P30/SEG20/TI03/TO03/REMOOUT	P30/TI03/TO03/SEG20/REMOOUT/TS08/(INTP3)/(RTC1HZ)
27	P77/KR7/SEG19/TKBO01-0	P77/KR7/SEG19/TS09/CCD00/TKBO01/SO20/TxD2/EI77/EO77/(TKBO21) [‡]
28	P76/KR6/SEG18/TKBO01-1	P76/KR6/SEG18/TS10/CCD01/TKBO00/SI20/SDA20/RxD2/EI76/EO76/(INTP2)/(RTC1HZ)/(EXSDO1)
29	P75/KR5/SEG17/TKBO01-2	P75/KR5/SEG17/TS11/CCD02/SCK20/SCL20/(TKBO11) [‡] /(TKBO01)/(TI03)/(TO03)/(REMOOUT)/(INTP0)
30	P74/KR4/SEG16/TKBO00	P74/KR4/SEG16/TS12/CCD03/TKBO11 [‡] /(TKBO01)
31	P70/KR0/SEG12	P70/KR0/SEG12/TS16/TKBO20 [‡]
32	P57/INTP6/SEG11	P57/INTP6/SEG11/TSCAP/(TI03)/(TO03)/(REMOOUT)
33	P54/SEG8/TI02/TO02	P54/TI02/TO02/SEG8/TS19/SCK01/SCL01/(INTP0)/(PCLBUZ0)
34	P53/INTP2/SEG7	P53/INTP2/SEG7/TS20/SI01/SDA01/(TI07)/(TO07)/(PCLBUZ0)
35	P52/INTP1/SEG6/TI00/TO00	P52/TI00/TO00/INTP1/SEG6/TS21/SO01/(PCLBUZ1)
36	COM7/SEG3	P97/COM7/SEG3/TS24/(TI05)/(TO05)/(SCK01)/(SCL01)/(SCLA1)
37	COM6/SEG2	P96/COM6/SEG2/TS25/(INTP5)/(SI01)/(SDA01)/(SDAA1)/(PCLBUZ0)
38	COM5/SEG1	P95/COM5/SEG1/TS26/(TI02)/(TO02)/(INTP1)/(SO01)
39	COM4/SEG0	P94/COM4/SEG0/TS27/(INTP2)/(SI01)/(SDA01)/(TI06)/(TO06)
40	COM3	P93/COM3/TS28/(INTP3)/(SCK01)/(SCL01)

Remarks: Locations where function pins have been deleted or moved are shown in red, and minor changes such as channel changes are shown in yellow.

Note : Products with code flash memory of 128 KB or less are not equipped.

Table 1.4 Pin function Comparison of 64pin Products (2)

No	RL78/L13	RL78/L23
41	COM2	P92/COM2/TS29/(TI01)/(TO01)
42	COM1	P91/COM1/TS30/(INTP2)
43	COM0	P90/COM0/TS31/(TI00)/(TO00)/(INTP1)
44	P07/SEG50/SO10/TxD1/(PCLBUZ0)	P07/SO10/TxD1/SEG50/TS32/EI07/(PCLBUZ0)
45	P06/SEG49/SI10/RxD1/SDA10	P06/SI10/RxD1/SDA10/SEG49/TS33/EI06/(PCLBUZ1)
46	P05/SEG48/SCK10/SCL10	P05/SCK10/SCL10/SEG48/TS34/EO05
47	P04/VCOU1/SEG47/TxD2	P04/SEG47/VCOU1/TS35/(INTP6)/(SO20)/(TxD2)/(PCLBUZ0)
48	P03/VCOU0/SEG46/RxD2	P03/SEG46/VCOU0/TRJIO0/(RxD2)/(SI20)/(SDA20)/(SI31)/(SDA31)
49	P02/PCLBUZ0/INTP7/SEG45	P02/INTP7/PCLBUZ0/SEG45/(TKBO21) [‡] /(SCK20)/(SCL20)/(SCK31)/(SCL31)
50	P01/PCLBUZ1/INTP5/SEG44/(TI05)/(TO05)	P01/PCLBUZ1/SEG44/(TI05)/(TO05)/(TKBO11) [‡] /(INTP5)/(SO31)
51	P00/TOOLTxD/SEG43/SO00/TxD0	P00/SEG43/SO00/TxD0/TOOLTxD/EI00/EO00/EXSDI0/(TKBO01)/(TRJIO0)
52	P17/TOOLRxD/SEG42/SI00/RxD0/SDA00	P17/SEG42/SI00/RxD0/TOOLRxD/SDA00/EI17/EO17/EXSDI1/(TKBO01)/(TRJIO0)
53	P16/SEG41/SCK00/SCL00	P16/SEG41/SCK00/SCL00/EI16/(VCOU0)/(TKBO01)/(RTC1HZ)
54	P15/SEG40/TI07/TO07	P15/TI07/TO07/SEG40
55	P14/SEG39/TI04/TO04	P14/TI04/TO04/SEG39/ANI26
56	P13/ANI25/SEG38	P13/ANI25/SEG38
57	P12/ANI24/SEG37	P12/ANI24/SEG37/EI12/CLKA0/SO11/(VCOU1)/(TKBO00)/(TRJIO1) [‡]
58	P11/ANI23/SEG36	P11/ANI23/SEG36/RxDA0/SI11/SDA11/(TKBO11) [‡] /(TRJIO1) [‡] /(INTP1)
59	P10/ANI22/SEG35	P10/ANI22/SEG35/TxDA0/SCK11/SCL11/(TKBO10) [‡] /(INTP0)
60	P27/ANI21/SEG34	P27/ANI21/SEG34/ANO1/EI27/RxDA1/SO21/(TKBO21) [‡]
61	P26/ANI20/SEG33	P26/ANI20/SEG33/ANO0/EI26/TxDA1/SI21/SDA21/(TKBO20) [‡] /(INTP5)/(RxD0)/(SI00)/(SDA00)/(EXSDI0)
62	P22/ANI16/SEG29	P22/ANI16/SEG29/SCK21/SCL21/(SCK00)/(SCL00)/(INTP7)
63	P21/ANI0/AVREFP	P21/ANI0/AVREFP/VBAT1/EI21/(TO00)/(INTP6)/(PCLBUZ0)
64	P20/ANI1/AVREFM	P20/ANI1/AVREFM/EI20/(TI00)/(INTP7)/(PCLBUZ1)

Remarks: Locations where function pins have been deleted or moved are shown in **red**, and minor changes such as channel changes are shown in **yellow**.

Note : Products with code flash memory of 128 KB or less are not equipped.

Table 1.5 Pin function Comparison of 80pin Products (1)

No	RL78/L13	RL78/L23
1	P130/SEG28/(SO00)/(TxD0)	P130/SEG28/TRJO1/(TxDA0)/(SO21)/(SO01)
2	P47/SEG27/(SI00)/(RxDO)/(SDA00)	P47/SEG27/(RxDA0)/(SI21)/(SDA21)/(SDA01)/(SI01)/(INTP1)
3	P46/SEG26/(SCK00)/(SCL00)	P46/SEG26/(SCK21)/(SCL21)/(SCL01)/(SCK01)
4	P45/IVREF0	P45/IVREF0/TxDA2/SCK30/SCL30/EXSDO0
5	P44/IVCMP0/(SCK10)/(SCL10)	P44/IVCMP0/RxDA2/SI30/SDA30/RxD3/EXSDO1/(TI04)/(TO04)/(INTP7)/(SCK11)/(SCL11)
6	P43/IVCMP1/(INTP7)/(SI10)/(RxD1)/(SDA10)	P43/IVCMP1/SO30/TxD3/(TI05)/(TO05)/(INTP4)/(RxDA1)/(SI11)/(SDA11)
7	P42/IVREF1/TI05/TO05/(SO10)/(TxD1)	P42/TI05/TO05/IVREF1/TRJO0/(INTP7)/(TxDA1)/(SCLA0)/(RxDO)/(TxD1)/(SI00)/(SDA00)/(SO11)/(PCLBUZ1)
8	P41/(TI07)/(TO07)	P41/(TI07)/(TO07)/(INTP6)/(TxD0)/(SDAA0)/(SO00)/(RxD1)
9	P40/TOOL0/(TI00)/(TO00)	P40/TOOL0/(TI00)/(TO00)/(SCK00)/(SCL00)
10	RESET	RESET
11	P124/XT2/EXCLKS	P124/XT2/EXCLKS
12	P123/XT1	P123/XT1
13	P137/INTP0	P137/EI137/INTP0
14	P122/X2/EXCLK	P122/X2/EXCLK/EI122
15	P121/X1	P121/X1/VBAT0/EI121
16	REGC	REGC
17	VSS	VSS
18	VDD	VDD
19	P60/SCLA0/(TI01)/(TO01)	P60/SCLA0/CCD04/EO60/(TI01)/(TO01)/(INTP3)
20	P61/SDAA0/(TI02)/(TO02)	P61/SDAA0/CCD05/EO61/(TI02)/(TO02)/(INTP4)
21	P127/CAPH/(TI03)/(TO03)/(REMOOUT)	P62/SCLA1/CCD06/(TI03)/(TO03)/(REMOOUT)/(INTP5)
22	P126/CAPL/(TI04)/(TO04)	P63/SDAA1/CCD07/(TI04)/(TO04)/(INTP6)
23	VL1	P127/CAPH/TS00/(TI03)/(TO03)/(REMOOUT)
24	VL2	P126/CAPL/TS01/(TI04)/(TO04)/(INTP4)
25	VL4	P87/VL1/(TxD1)/(SO10)
26	P125/VL3/(TI06)/(TO06)	P86/VL2/(TI06)/(TO06)/(INTP3)/(RxD1)/(SI10)/(SDA10)/(PCLBUZ1)
27	P35/SEG25/TxD3	P85/VL4/(VCOUT0)/(INTP4)/(SCK10)/(SCL10)/(SCK30)/(SCL30)
28	P34/SEG24/RxD3	P125/VL3/TS02/(TI06)/(TO06)/(VCOUT1)/(INTP7)/(RxD3)/(SI30)/(SDA30)/(PCLBUZ1)
29	P33/INTP4/SEG23	P35/SEG25/TS03/(VCOUT0)/(INTP4)/(SO30)/(TxD3)
30	P32/SEG22/TI01/TO01	P34/SEG24/TS04/(TI01)/(TO01)/(INTP0)/(RxD3)
31	P31/INTP3/SEG21/RTC1HZ	P31/INTP3/RTC1HZ/SEG21/TS07/(TI01)/(TO01)
32	P30/SEG20/TI03/TO03/REMOOUT	P30/TI03/TO03/SEG20/REMOOUT/TS08/(INTP3)/(RTC1HZ)
33	P77/KR7/SEG19/TKBO01-0	P77/KR7/SEG19/TS09/CCD00/TKBO01/SO20/TxD2/EI77/EO77/(TKBO21)/(TI07)/(TO07)/(INTP1)/(EXSDO0)
34	P76/KR6/SEG18/TKBO01-1	P76/KR6/SEG18/TS10/CCD01/TKBO00/SI20/SDA20/RxD2/EI76/EO76/(INTP2)/(RTC1HZ)/(EXSDO1)
35	P75/KR5/SEG17/TKBO01-2	P75/KR5/SEG17/TS11/CCD02/SCK20/SCL20/(TKBO11)/(TKBO01)/(TI03)/(TO03)/(REMOOUT)/(INTP0)
36	P74/KR4/SEG16/TKBO00	P74/KR4/SEG16/TS12/CCD03/TKBO11/(TKBO01)
37	P73/KR3/SEG15	P73/KR3/SEG15/TS13/TKBO10
38	P72/KR2/SEG14	P72/KR2/SEG14/TS14/TKBO21
39	P71/KR1/SEG13	P71/KR1/SEG13/TS15
40	P70/KR0/SEG12	P70/KR0/SEG12/TS16/TKBO20

Remarks: Locations where function pins have been deleted or moved are shown in **red**, and minor changes such as channel changes are shown in **yellow**.

Note : Products with code flash memory of 128 KB or less are not equipped.

Table 1.6 Pin function Comparison of 80pin Products (2)

No	RL78/L13	RL78/L23
41	P57/INTP6/SEG11	P57/INTP6/SEG11/TSCAP/(TI03)/(TO03)/(REMOOUT)
42	P56/SEG10/TI06/TO06	P56/TI06/TO06/SEG10/TS17
43	P55/INTP5/SEG9	P55/INTP5/SEG9/TS18/(TI02)/(TO02)
44	P54/SEG8/TI02/TO02	P54/TI02/TO02/SEG8/TS19/SCK01/SCL01/(INTP0)/(PCLBUZ0)
45	P53/INTP2/SEG7	P53/INTP2/SEG7/TS20/SI01/SDA01/(TI07)/(TO07)/(PCLBUZ0)
46	P52/INTP1/SEG6/TI00/TO00	P52/TI00/TO00/INTP1/SEG6/TS21/SO01/(PCLBUZ1)
47	P51/SEG5	P51/SEG5/TS22/RxDA3/(INTP6)
48	P50/SEG4	P50/SEG4/TS23/TxDA3
49	COM7/SEG3	P97/COM7/SEG3/TS24/(TI05)/(TO05)/(SCK01)/(SCL01)/(SCLA1)
50	COM6/SEG2	P96/COM6/SEG2/TS25/(INTP5)/(SI01)/(SDA01)/(SDAA1)/(PCLBUZ0)
51	COM5/SEG1	P95/COM5/SEG1/TS26/(TI02)/(TO02)/(INTP1)/(SO01)
52	COM4/SEG0	P94/COM4/SEG0/TS27/(INTP2)/(SI01)/(SDA01)/(TI06)/(TO06)
53	COM3	P93/COM3/TS28/(INTP3)/(SCK01)/(SCL01)
54	COM2	P92/COM2/TS29/(TI01)/(TO01)
55	COM1	P91/COM1/TS30/(INTP2)
56	COM0	P90/COM0/TS31/(TI00)/(TO00)/(INTP1)
57	P07/SEG50/SO10/TxD1/(PCLBUZ0)	P07/SO10/TxD1/SEG50/TS32/EI07/(PCLBUZ0)
58	P06/SEG49/SI10/RxD1/SDA10	P06/SI10/RxD1/SDA10/SEG49/TS33/EI06/(PCLBUZ1)
59	P05/SEG48/SCK10/SCL10	P05/SCK10/SCL10/SEG48/TS34/EO05
60	P04/VCOU1/SEG47/TxD2	P04/SEG47/VCOU1/TS35/(INTP6)/(SO20)/(TxD2)/(PCLBUZ0)
61	P03/VCOU0/SEG46/RxD2	P03/SEG46/VCOU0/TRJIO0/(RxD2)/(SI20)/(SDA20)/(SI31)/(SDA31)
62	P02/PCLBUZ0/INTP7/SEG45	P02/INTP7/PCLBUZ0/SEG45/(TKBO21)/(SCK20)/(SCL20) /(SCK31)/(SCL31)
63	P01/PCLBUZ1/SEG44/(INTP5)/(TI05)/(TO05)	P01/PCLBUZ1/SEG44/(TI05)/(TO05)/(TKBO11)/(INTP5)/(SO31)
64	P00/TOOLTxD/SEG43/SO00/TxD0	P00/SEG43/SO00/TxD0/TOOLTxD/EI00/EO00/EXSDI0/(TKBO01)/(TRJ00)
65	P17/TOOLRxD/SEG42/SI00/RxD0/SDA00	P17/SEG42/SI00/RxD0/TOOLRxD/SDA00/EI17/EO17/EXSDI1/(TKBO01) /(TRJIO0)
66	P16/SEG41/SCK00/SCL00	P16/SEG41/SCK00/SCL00/EI16/(VCOU0)/(TKBO01)/(RTC1HZ)
67	P15/SEG40/TI07/TO07	P15/TI07/TO07/SEG40
68	P14/SEG39/TI04/TO04	P14/TI04/TO04/SEG39/ANI26
69	P13/ANI25/SEG38	P13/ANI25/SEG38
70	P12/ANI24/SEG37	P12/ANI24/SEG37/EI12/CLKA0/SO11/(VCOU1)/(TKBO00)/(TRJO1) /(PCLBUZ1)
71	P11/ANI23/SEG36	P11/ANI23/SEG36/RxDA0/SI11/SDA11/(TKBO11)/(TRJIO1)/(INTP1)
72	P10/ANI22/SEG35	P10/ANI22/SEG35/TxDA0/SCK11/SCL11/(TKBO10)/(INTP0)
73	P27/ANI21/SEG34	P27/ANI21/SEG34/ANO1/EI27/RxDA1/SO21/(TKBO21)/(INTP4)/(TxD0) /(SO00)/(EXSDI1)
74	P26/ANI20/SEG33	P26/ANI20/SEG33/ANO0/EI26/TxDA1/SI21/SDA21/(TKBO20)/(INTP5)/(RxD0) /(SI00)/(SDA00)/(EXSDI0)
75	P25/ANI19/SEG32	P25/ANI19/SEG32/CLKA1
76	P24/ANI18/SEG31	P24/ANI18/SEG31
77	P23/ANI17/SEG30	P23/ANI17/SEG30/TRJIO1
78	P22/ANI16/SEG29	P22/ANI16/SEG29/SCK21/SCL21/(SCK00)/(SCL00)/(INTP7)
79	P21/ANI0/AVREFFP	P21/ANI0/AVREFFP/VBAT1/EI21/(TO00)/(INTP6)/(PCLBUZ0)
80	P20/ANI1/AVREFM	P20/ANI1/AVREFM/EI20/(TI00)/(INTP7)/(PCLBUZ1)

Remarks: Locations where function pins have been deleted or moved are shown in **red**, and minor changes such as channel changes are shown in **yellow**.

Note : Products with code flash memory of 128 KB or less are not equipped.

2. Notes for migration

This chapter describes the points to be aware of when developing programs for functions that have been partially changed. Since the bit assignment of peripheral function registers has been changed even if they are registers with the same name, it is recommended to use the code output again using the Smart Configurator (SC) note for peripheral function settings. For details on the new functions of the RL78/L23, refer to the User's Manual, Hardware.

Note: Code Generator (CG), which is an RL78/L13 development tool, is not supported.

2.1 Port Function

The table below shows the new, changed, or deleted registers.

Additional capacitive unit functions, logic and event link controllers, output current control ports, and registers for setting up 40 mA port outputs have been added as port dual functions.

Since alternative functions that are not used at the same time are not selected, the description of the registers that control the port function is omitted from this chapter onwards.

Table 2.1 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	remarks
—	Port digital input disable registers (PDIDISxx)	Registers prevent through-current flowing into input buffers
Port mode control registers (PMCxx)	Port mode control A registers (PMCAxx)	Registers to select digital input/output or analog functions
—	Port mode control T registers (PMCTxx)	Registers to select digital input/output or capacitance measurement functions
—	Port mode control E registers (PMCExx)	Registers to select digital input/output or ELCL output functions
—	Port function output enable registers (PFOEx)	Registers that connect peripheral outputs only to ELCL inputs
A/D port configuration register (ADPC)	—	Registers to select digital input/output or analog input
—	Output current control enable registers (CCDE)	Registers to be set for the output current control port
—	Output current select registers (CCSx)	Registers that select the low-level output current of the output current control port selected by the CCDE register
—	40-mA port output control register (PTDC)	Register to set the allowable output current at low-level output to 40 mA.

Remarks: :Add, :Change, : Delete, — : No corresponding register

Note : PMxx, Pxx, PUxx, PIMx, POMxx, PIORx, PMS, PFSEGx, ISCLCD registers are common, but some changes such as bit assignment have been made.

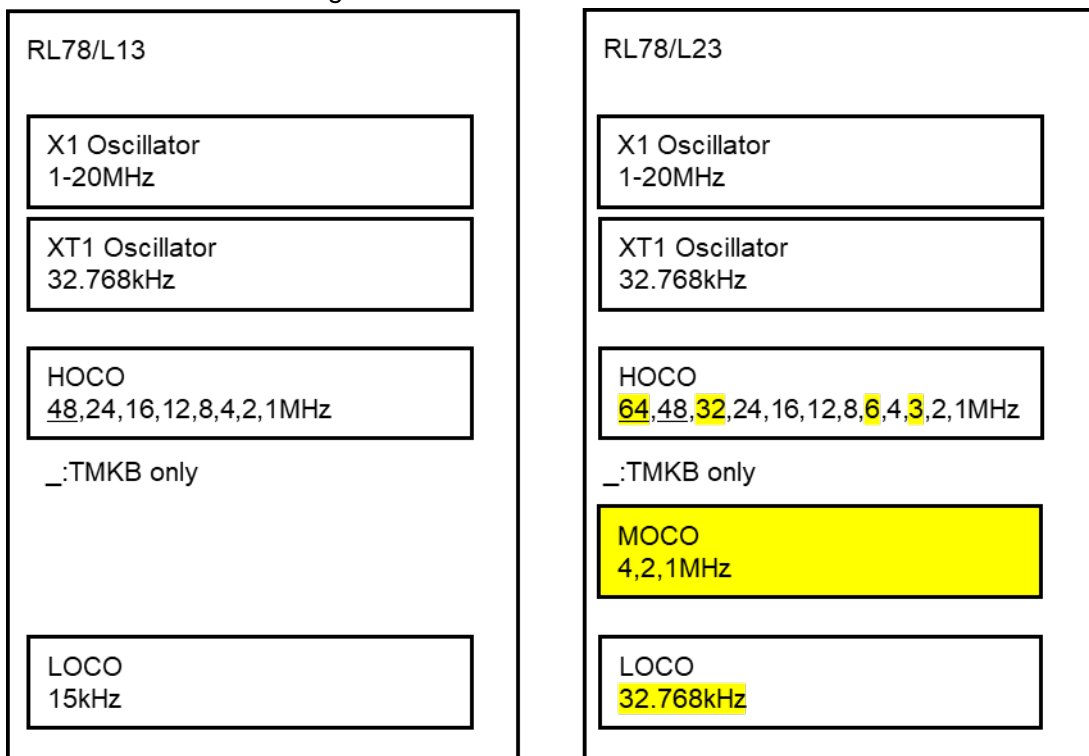
For details of each register function, refer to the User's Manual: Hardware.

2.2 Clock Generator

The maximum frequency of the high-speed on-chip oscillator (HOCO) has been changed from 48 MHz to 64 MHz. The maximum operating frequency of the CPU has been changed from 24 MHz to 32 MHz. Please refer to the figure below.

In addition, the middle-speed on-chip oscillator MOCO (4 MHz, 2 MHz, 1 MHz) was added, and the low-speed on-chip oscillator frequency was changed from 15 kHz to 32.768 kHz. Please refer to the figure below.

Figure 2.1 Clock Generator Difference



Remarks: :Add & Change

In addition, in the L23, the PERx register's function becomes a clock supply control only, and a new PRRx register has been installed as a reset control register for peripheral functions.

Note: 64 MHz (RL78/L23) and 48 MHz (RL78/L13) are clocks that can be used with the 16-bit timer KB20.

The new registers for the RL78/L23 are shown in the table below.

Table 2.2 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
—	Peripheral enable register 2 (PER2)	Peripheral clock supply registers
—	Subsystem clock select register (CKSEL)	Subsystem clock selection settings register
—	High-speed on-chip oscillator frequency select register (HOCODIV)	HOCO clock divide setting register
—	Middle-speed on-chip oscillator frequency select register (MOSODIV)	MOCO clock divide setting register
—	Middle-speed on-chip oscillator trimming register (MIOTRM)	MOCO trimming settings register
—	Low-speed on-chip oscillator trimming register (LIOTRM)	LOCO trimming setting register
—	Standby mode release setting register (WKUPMD)	HOCO's start timing of release from STOP mode setting register
—	XT1 oscillator margin checking control register (SOMRG)	Setting register for margin check of oscillator.

Remarks: : Add, — : No corresponding register

Note : CMC, CKC, CSC, OSTC, OSTs, PER0, PER1, OSMC, HOCODIV, HIOTRM registers are common, but some changes such as bit assignment have been made.

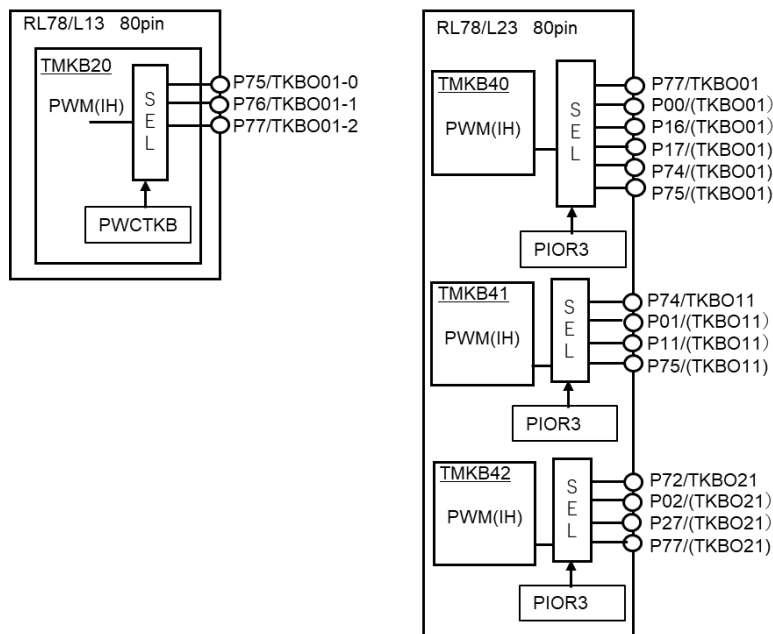
For details of each register function, refer to the User's Manual: Hardware.

2.4 16-BIT TIMER KB20

The RL78/L23 has three 16-bit timers, KB40, KB41, and KB42, and has been expanded to include functional enhancements.

As for the IH output, the RL78/L13 can output up to 1 channel 3, but the RL78/L23 can output up to 3 channels and 11 outputs. However, since it is a selectable output, the number of channels that can be output at the same time is the number of channels.

Figure 2.3 16-bit timer KB20 IH output difference



The table below shows the new and changed registers for the RL78/L23.

Table 2.4 RL78/L23 Change Registers (1)

RL78/L13	RL78/L23	
Register name	Register name	Remarks
Peripheral enable register 1 (PER1)	Peripheral enable register 2 (PER2)	Changing the Registers to Clock Control
—	Peripheral reset control register (PRR2)	Registers to initialize SFR for timer KB4n
16-bit timer KB2 operation control register 00 (TKBCTL00)	16-bit timer KB2 operation control register n0 (TKBCTLn0) (n=0 to 2)	Increase registers due to 3-ch and Format change
16-bit timer KB2 operation control register 01q (TKBCTL01)	16-bit timer KB2 operation control register n1 (TKBCTLn1) (n=0 to 2)	Increase registers due to 3-ch and Format change
16-bit timer KB2 output control register 00 (TKBIOC00)	16-bit timer KB2 output control register n0 (TKBIOCn0) (n=0 to 2)	Increase registers due to 3-ch
16-bit timer KB2 output control register 01 (TKBIOC01)	16-bit timer KB2 output control register n1 (TKBIOCn1) (n=0 to 2)	Increase registers due to 3-ch and Format change
16-bit timer KB2 flag register 0 (TKBFLG0)	16-bit timer KB2 flag register n (TKBFLGn) (n = 0 to 2)	Increase registers due to 3-ch
16-bit timer KB2 trigger register 0 (TKBTRG0)	16-bit timer KB2 trigger register n (TKBTRGn) (n=0 to 2)	Increase registers due to 3-ch

Remarks : : Change to 3ch, : Add, : Change, — : No corresponding register
 Note : For details of each register function, refer to the User's Manual: Hardware.

Table 2.5 RL78/L23 Change Registers (2)

RL78/L13	RL78/L23	
Register name	Register name	Remarks
16-bit timer KB flag clear trigger register 0 (TKBCLR0)	16-bit timer KB flag clear trigger register n (TKBCLRn) (n = 0 to 2)	Increase registers due to 3-ch
16-bit timer KB dithering count register 00,01 (TKBDNR00, TKBDNR01)	16-bit timer KB dithering count register np (TKBDNRnp) (n = 0 to 2; p = 0, 1)	Increase registers due to 3-ch
16-bit timer KB compare 1L & dithering count register 00 (TKBCRLD00)	16-bit timer KB compare 1L & dithering count register n0 (TKBCRLDn0) (n = 0 to 2)	Increase registers due to 3-ch
16-bit timer KB2 compare 3L & dithering count register 01 (TKBCRLD01)	16-bit timer KB compare 3L & dithering count register n1 (TKBCRLDn1) (n = 0 to 2)	Increase registers due to 3-ch
16-bit timer KB2 smooth start initial duty registers 00, 01 (TKBSIR00, TKBSIR01)	16-bit timer KB smooth start initial duty register np (TKBSIRnp) (n = 0 to 2; p = 0, 1)	Increase registers due to 3-ch
16-bit timer KB2 smooth start step width registers 00, 01 (TKBSSR00, TKBSSR01)	16-bit timer KB smooth start step width register np (TKBSSRnp) (n = 0 to 2; p = 0, 1)	Increase registers due to 3-ch
16-bit timer KB2 maximum frequency limit setting register 0 (TKBMFR0)	16-bit timer KB maximum frequency limit setting register n (TKBMFRn) (n = 0 to 2)	Increase registers due to 3-ch
16-bit timer KB2 counter restart select register (ELSELRn) (n= 0 to 9)	16-bit timer KB operation control register n2 (TKBCTLn2) (n = 0 to 2)	Increase registers due to 3-ch and Format change
16-bit timer KB2 output switch register (PWCTKB)	Peripheral I/O redirection registers (PIORx)	Change this setting to a register of the port function
—	16-bit timer KB skipping control register n (TKBTCTLn) (n=0 to 2)	Registers for skipping interrupt / A/D trigger signals
—	16-bit timer KB times-of-skipping setting register n(TKBTCMPn) (n= 0 to 2)	Registers for skipping interrupt / A/D trigger signals
—	External interrupt control register x (INTPCTLx) (x = 0 to 7)	Registers for filtering external interrupt pins (INTPx)
Forced output stop function control register 0 (TKBPACTL00)	Forced output stop function control register np (TKBPACTLnp) (n = 0 to 2; p = 0, 1)	Increase registers due to 3-ch and Function changed
Forced output stop function control register 1 (TKBPACTL01)		
Forced output stop function control register 2 (TKBPACTL02)		
Forced output stop function flag register 0 (TKBPAFLG0)	Forced output stop function flag register n (TKBPAFLGn) (n = 0 to 2)	Increase registers due to 3-ch
Forced output stop function 1 Start register (TKBPAHFS0)	Forced output stop function start trigger register n (TKBPAHFSn) (n = 0 to 2)	Increase registers due to 3-ch
Forced output stop function 1 stop register (TKBPAHFT0)	Forced output stop function cancel trigger register n (TKBPAHFTn) (n = 0 to 2)	Register increase by 3-ch and support for stop function 2

Remarks : : Change to 3ch, : Add, : Change, — : No corresponding register

Note : For details of each register function, refer to the User's Manual: Hardware.

2.5 Realtime Clock

It is now possible to select 128Hz created from fRTC as the operating clock. In addition, 500 ms signal generation function for LCD flashing display has been added. Due to the addition of this function, some of the registers have been changed.

Table 2.6 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
Subsystem clock supply mode control register (OSMC)	Subsystem clock supply mode control register (OSMC)	Added bit 128Hz operation as the operating clock.
Realtime clock control register 0 (RTCC0)	Realtime clock control register 0 (RTCC0)	Added bit to 128Hz operation with OSMC

Note : For details on each register function, refer to the User's Manual Hardware.

2.6 Watchdog Timer

There is no change in the control specifications, but the override time and window open time specifications have been changed because the count clock has been changed from 15 kHz (TYP.) to 32.768 kHz (TYP.).

Table 2.7 Overflow Time Comparison

WDCS2-0 setting	Overflow time	
	RL78/L13 (fIL=17.25 kHz (Max case))	RL78/L23 (fIL=37.683 (Max case))
000	$2^6/fIL$ (3.71 ms)	$2^7/fIL$ (3.39 ms)
001	$2^7/fIL$ (7.42 ms)	$2^8/fIL$ (6.79 ms)
010	$2^8/fIL$ (14.84 ms)	$2^9/fIL$ (13.58 ms)
011	$2^9/fIL$ (29.68 ms)	$2^{10}/fIL$ (27.17 ms)
100	$2^{11}/fIL$ (118.72 ms)	$2^{12}/fIL$ (108.69 ms)
101	$2^{13}/fIL$ (474.89 ms)	$2^{14}/fIL$ (434.78 ms)
110	$2^{14}/fIL$ (949.79 ms)	$2^{15}/fIL$ (869.56 ms)
111	$2^{16}/fIL$ (3799.18 ms)	$2^{17}/fIL$ (3478.26 ms)

2.7 A/D Converter

It has been changed to an A/D converter with 12-bit resolution.

The 16-bit timer KB4x A/D trigger signal and ELCL event input have been added to the selectable hardware triggers. Please refer to the table below for register differences.

Table 2.8 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
—	Peripheral reset control register 0 (PRR0)	Register to reset the A/D converter
A/D converter mode register 1 (ADM1)	A A/D converter mode register 1 (ADM1)	Added selectable hardware triggers
—	A/D converter mode extension register 1 (ADM1EX)	Register that selects a hardware trigger with the ADM1 register.
A/D converter mode register 2 (ADM2)	A/D converter mode register 2 (ADM2)	Added 12-bit conversion
10-bit A/D conversion result register (ADCR)	12-bit/10-bit A/D conversion result register (ADCR0)	Register name change.
8-bit A/D conversion result register (ADCRH)	8-bit A/D conversion result register (ADCR0H)	Register name change.
A/D port configuration register (ADPC)	—	Delete

Remarks: :Add, :Change, : Delete, — : No corresponding register

Note : For details on each register function, refer to the User's Manual Hardware.

2.8 Serial Array Unit

There is no change in the functions that can be achieved with the RL78/L13. A loopback function has been added to UART communication. In addition, functions such as the ability to input an output signal from ELCL have been added.

Table 2.9 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
—	Peripheral reset control register 0 (PRR0)	Register to reset the Serial Array Unit
—	UART loopback select register (ULBS)	Added function that UART output to the receive shift register
Input switch control register (ISC)	Input switch control register (ISC)	Input to CSI00,01 the input clock and data have been enhanced.

Remarks : :Add, — : No corresponding register

Note :For details on each register function, refer to the User's Manual Hardware.

2.9 Serial Interface IICA

There is no change in the functions that can be achieved with the RL78/L13.

Table 2.10 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
—	Peripheral reset control register 0 (PRR0)	Register to reset the Serial Interface IICA

Remarks : :Add, — : No corresponding register

Note :For details on each register function, refer to the User's Manual Hardware.

2.10 LCD Controller/Driver

The VL2 reference method has been added to the internal boost method, and the VL4 reference method has been added to the capacitance split method, and 6 common output is now possible. As a result, some of the register specifications have been changed.

The switching timing of the LCD flashing display has been added to the 0.5 second period and the arbitrarily set ELCITL2 period. The relationship between the RL78/L13 port number and the SEG output number remains unchanged for the SEG ports that exist in the RL78/L23, but two SEG ports have been deleted. In addition, Changed the output ports of COM0-3 to be used as a I/O digital port as well. With the exception of SEG0-SEG4, all SEG/COM pins have been changed to multiplexed I/O ports. Please refer to the table below.

Table 2.11 LCD display function ports (64 pins products)

Item	RL78/L13								RL78/L23							
	Segment signal outputs : 36 (32) ^{Note} Common signal outputs : 8								Segment signal outputs : 34 (30) ^{Note} Common signal outputs : 8							
Multiplexed I/O port	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44	SEG 43	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44	SEG 43
P1	SEG 42	SEG 41	SEG 40	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 42	SEG 41	SEG 40	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35
P2	SEG 34	SEG 33	—	—	—	SEG 29	—	—	SEG 34	SEG 33	—	—	—	SEG 29	—	—
P3	—	—	—	—	SEG 23	SEG 22	SEG 21	SEG 20	—	—	—	—	—	—	SEG 21	SEG 20
P4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P5	SEG 11	—	—	SEG 8	SEG 7	SEG 6	—	—	SEG 11	—	—	SEG 8	SEG 7	SEG 6	—	—
P7	SEG 19	SEG 18	SEG 17	SEG 16	—	—	—	SEG 12	SEG 19	SEG 18	SEG 17	SEG 16	—	—	—	SEG 12
P9	—	—	—	—	—	—	—	—	SEG3/COM7	SEG2/COM6	SEG1/COM5	SEG0/COM4	COM3	COM2	COM1	COM0
Not multiplexed with I/O port																
COM0	—								—							
COM1	—								—							
COM2	—								—							
COM3	—								—							
COM4	SEG0								—							
COM5	SEG1								—							
COM6	SEG2								—							
COM7	SEG3								—							

Note : () indicates the number of signal output pins when 8 com is used.

Remarks: :Change, : Delete, — : No corresponding register

Table 2.12 LCD display function ports (80 pins products)

Item	RL78/L13								RL78/L23							
LCD Controllers / Driver	Segment signal outputs : 51 (47) ^{Note} Common signal outputs : 8								Segment signal outputs : 49 (45) ^{Note} Common signal outputs : 8							
Multiplexed I/O port	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44	SEG 43	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44	SEG 43
P1	SEG 42	SEG 41	SEG 40	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 42	SEG 41	SEG 40	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35
P2	SEG 34	SEG 33	SEG 32	SEG 31	SEG 30	SEG 29	—	—	SEG 34	SEG 33	SEG 32	SEG 31	SEG 30	SEG 29	—	—
P3	—	—	SEG 25	SEG 24	SEG 23	SEG 22	SEG 21	SEG 20	—	—	SEG 25	SEG 24	—	—	SEG 21	SEG 20
P4	SEG 27	SEG 26	—	—	—	—	—	—	SEG 27	SEG 26	—	—	—	—	—	—
P5	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4
P7	SEG 19	SEG 18	SEG 17	SEG 16	SEG 15	SEG 14	SEG 13	SEG 12	SEG 19	SEG 18	SEG 17	SEG 16	SEG 15	SEG 14	SEG 13	SEG 12
P9	—	—	—	—	—	—	—	—	SEG3/ COM7	SEG2/ COM6	SEG1/ COM5	SEG0/ COM4	COM3	COM2	COM1	COM0
P13	—	—	—	—	—	—	—	SEG 28	—	—	—	—	—	—	—	SEG 28
Not multiplexed with I/O port																
COM0	—								—							
COM1	—								—							
COM2	—								—							
COM3	—								—							
COM4	SEG0								—							
COM5	SEG1								—							
COM6	SEG2								—							
COM7	SEG3								—							

Note : () indicates the number of signal output pins when 8 com is used.

Remarks: :Change, : Delete, — : No corresponding register

Also, please note that the control register specifications have been changed.

Table 2.13 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
LCD mode register 0 (LCDM0)	LCD mode register 0 (LCDM0)	Changed the format of the LCD Drive voltage generation selection
—	LCD mode register 2 (LCDM2)	Register to set the switching timing of the LCD flashing display
LCD clock control register 0 (LCDC0)	LCD clock control register 0 (LCDC0)	Changed the LCD Clock Selection Format
LCD boost level control register (VLCD)	LCD boost level control register (VLCD)	Changed LCD drive voltage method and contrast adjustment format of a Selection
Input switch control register (ISCLCD)	Input switch control register (ISCLCD)	Increase in the number of applicable setting pins
LCD port function registers (PFSEGx)	LCD port function registers (PFSEGx)	Changed the format of the register to select the port or the LCD function pin

Remarks : :Add, — : No corresponding register

Note :For details on each register function, refer to the User's Manual Hardware.

2.11 Interrupt functions

There is no change in the basic function of interrupts, but since the peripheral functions have been significantly increased in the RL78/L23, the format of the interrupt factor, its vector table, and the register corresponding to the interrupt request source has also changed significantly. For flags related to each interrupt source, please refer to the RL78/L23 User's Manual before developing the software.

Table 2.14 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
Interrupt request flag registers (IFxx)	Interrupt request flag registers (IFxx)	Format changed
Format of Interrupt Mask Flag Registers (MKxx)	Format of Interrupt Mask Flag Registers (MKxx)	Format changed
Priority specification flag registers (PRxx)	Priority specification flag registers (PRxx)	Format changed

Note :For details on each register function, refer to the User's Manual Hardware.

2.12 Standby Function

A function that can shut down RAM and a setting that can quickly start a high-speed on-chip oscillator at the time of release of standby mode have been added. Please refer to the table below.

Table 2.15 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
—	Standby mode release setting register (WKUPMD)	Register to Setting for starting the high-speed on-chip oscillator at the times of release from standby mode
—	Power Reduction Control Register(PSMCR)	Register to shut down a partial RAM

Remarks: :Add, — : No corresponding register

Note : For details on each register function, refer to the User's Manual Hardware.

2.13 Reset Function

A register has been added to initialize the SFR of peripheral functions. Please refer to the table below.

Table 2.16 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
—	Peripheral reset control register 0 (PRR0)	Registers for initializing peripheral function (SFR)
—	Peripheral reset control register 1 (PRR1)	Registers for initializing peripheral function (SFR)

Remarks: :Add, — : No corresponding register

Note : For details on each register function, refer to the User's Manual Hardware.

2.14 Voltage Detector

The voltage detection circuit has been changed from one (LVD) to two (LVD0, LVD1). LVD0 was still set by an option byte, and LVD1 was set by a voltage detection level register.

Table 2.17 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
<u>User option byte</u> 000C1H/010C1H (Settings related to LVD.)	<u>User option byte</u> 000C1H/Swap dest. address (Settings related to LVD.)	Changed the Format
Voltage detection register (LVIM)	Voltage detection register (LVIM)	LVIOMSK function removed, and voltage detection and interrupt detect bits added to the second voltage-detect circuit.
—	LVD detection flag clearing register (LVDFCLR)	Function registers to clear the interrupt detection flag of each LVD detection circuit
Voltage detection level register (LVIS)	Voltage detection level register (LVIS)	Changed LVD1 Operation and Detect voltage settings

Remarks: :Add, :Change, — : No corresponding register

Note : For details on each register function, refer to the User's Manual Hardware.

2.15 Safety Functions

Flash Memory Guard, Unauthorized Memory Access Detection and Control Register (IAWCTL) Guard and UART loopback functions have been added.

The table below shows the newly added registers.

Table 2.18 RL78/L23 Change Registers

RL78/L13	RL78/L23	
Register name	Register name	Remarks
—	Code flash memory guard register (GFLASH0)	Register to protect writes to code flash memory
—	Data flash memory guard register (GFLASH1)	Register to protect writes to data flash memory
—	Flash security area guard register (GFLASH2)	Register that protect the flash security area that contains the security settings of the flash memory
—	Invalid memory access detection control register (GIAWCTL)	Register to protect the enable/disable of the illegal memory access detection function
—	UART loopback select register (ULBS)	Register to enable the UART loopback function

Remarks: : Add, — : No corresponding register

Note : For details on each register function, refer to the User's Manual Hardware.

2.16 Regulator

The regulator output voltage has been changed from (1.8V, 2.1V) to 1.5V. There are no notes.

2.17 Option Bytes

The functions have been expanded and some specifications have been changed, so please check the User's Manual Hardware for details. When using boot swap, it is necessary to set an option byte for the boot swap destination address, but since the RL78/L23 can selectively set the boot swap area, the setting address changes according to the boot swap setting. The following table shows the difference between the option bytes.

2.18 RL78/L23 Instruction

With the adoption of the S3 core in the RL78/L23, Multiplication and accumulation register (MACR)" used in the multiply-accumulate operation instruction has been added. (The MACR register consists of Multiplication and accumulation register (H)/(L): MACRH/MACRL.)

3. Documents for Reference

RL78/L13 User's Manual: Hardware (R01UH0382)

RL78/L23 User's Manual: Hardware (R01UH1082)

RL78 Family User's Manual: Software (R01US0015)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov.11.24	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

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