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H8/38124 Group

Low-Voltage Detection with a Low-Voltage Detection Circuit (Internal Reference Voltage Used)

Introduction

The H8/38124 uses a low-voltage detection circuit to detect a power supply voltage drop. The circuit uses an internal reference voltage as the reference voltage and a voltage generated by an internal resistance ladder as the power-supply voltage detection level. When the power-supply voltage drops to the power-supply drop detection voltage (Vint(D)), the H8/38124 switches from the active (high-speed) mode to the standby mode. When the power-supply voltage rises again to the power supply rise detection voltage (Vint(U)) without dropping to the reset detection voltage (Vreset1), the H8/38124 cancels the standby mode, returns to the active (high-speed) mode, releases the low-voltage detection circuit, and then terminates processing.

Target Device

H8/38124

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1. Specifications

- The H8/38124 uses the low-voltage detection interrupt circuit (LVDI) to detect a power supply voltage drop.
- The H8/38124 uses the voltage generated by the internal resistance ladder as the power supply drop detection voltage (Vint(D)) and the power supply rise detection voltage (Vint(U)) and internal reference voltage as the reference voltage of the low-voltage detection circuit.
- When the power-supply voltage drops to the power supply drop detection voltage (Vint(D)) in the active (high-speed) mode, the H8/38124 switches from the active (high-speed) mode to the standby mode. Thereafter, when the power-supply voltage rises again to the power supply rise detection voltage (Vint(U)) without dropping to the reset detection voltage (Vreset1), the H8/38124 transitions from the standby mode to the active (high-speed) mode, stops the low-voltage detection circuit, and then terminates processing.
- An LED is turned on by connecting the LED to the P90 pin and outputting a low-level signal from the pin. In the standby mode, the LED goes off because the port output enters the high-impedance state.
- Low-voltage detection with the low-voltage detection circuit (using the internal reference voltage) is shown in figure 1.

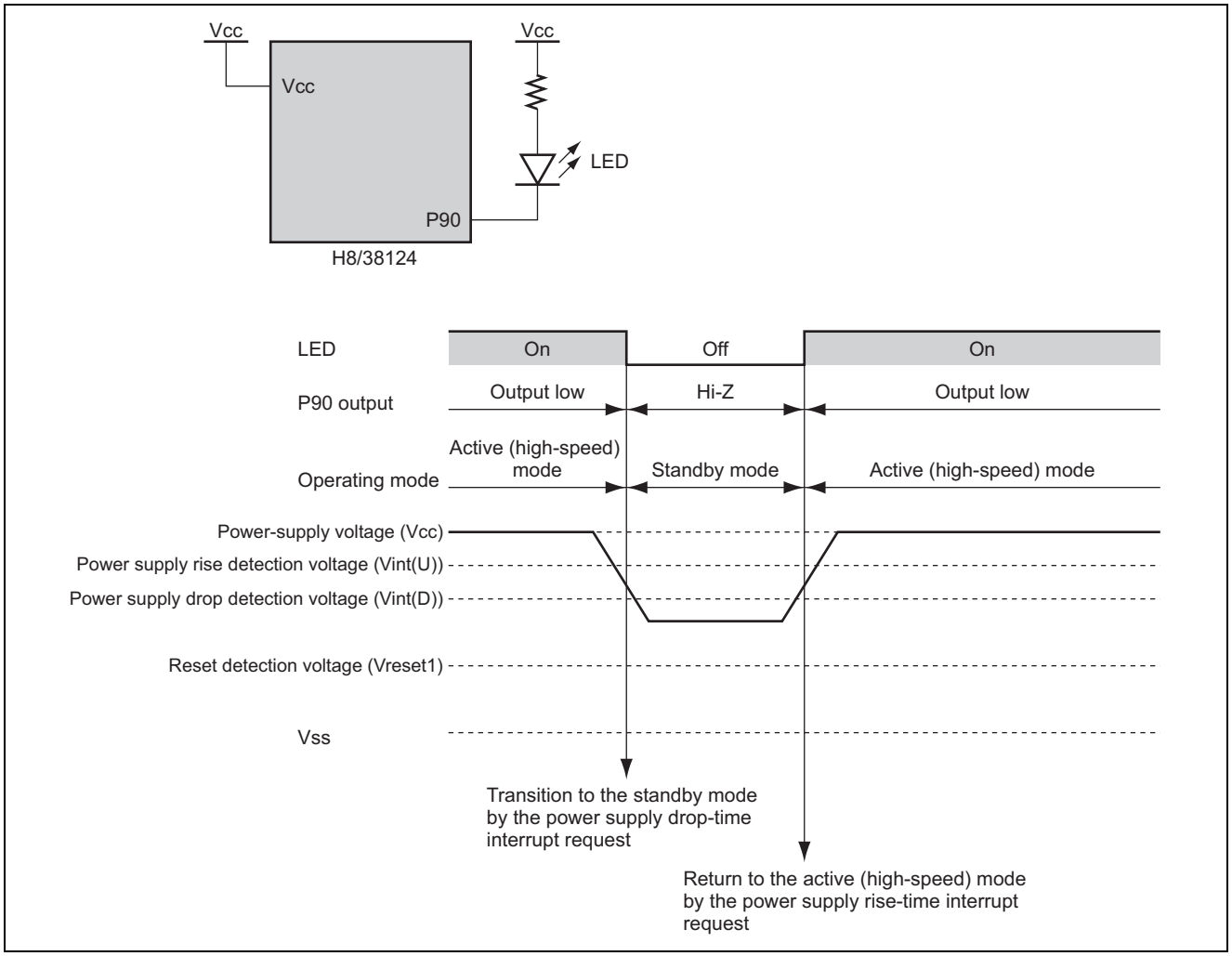


Figure 1 Low-Voltage Detection with Low-Voltage Detection Circuit (Internal Reference Voltage Used)

2. Description of Functions Used

2.1 Functions Used

This section describes the H8/38124 functions used in this sample task.

(1) Low-voltage detection circuits

The low-voltage detection circuits consists of a low-voltage detection interrupt (LVDI: Interrupt by Low Voltage Detect) circuit and a low-voltage detection reset (LVDR: Reset by Low Voltage Detect) circuit. These circuits are used to prevent abnormal LSI operation (runaway) resulting from a power-supply voltage drop and to restore the state present before the power-supply voltage drop when the power-supply voltage rises again.

Even if the power-supply voltage drops, the low-voltage detection circuit operates and the H8/38124 enters the standby mode during normal operation before the voltage exceeds the guaranteed operating voltage. This prevents an unstable state from occurring when the power-supply voltage falls below the guaranteed operating voltage. Thus, system safety can be improved. If the power supply voltage drops further, the H8/38124 automatically enters the reset state. If the power-supply voltage rises again, the reset state is maintained for a given length of time and then the system automatically switches to the active mode.

The following are features of the low-voltage detection circuits:

- Low-voltage detection reset circuit. This circuit monitors the power-supply voltage. When the power-supply voltage drops below a specified value, an internal reset signal is generated.
- Low-voltage detection interrupt circuit. This circuit monitors the power-supply voltage. When the power-supply voltage drops below or rises above respective specified values, an interrupt is generated.

There are two selections of reset generation voltage detection levels; one for stand-alone use of the low-voltage detection reset circuit and the other for combined use of the low-voltage detection interrupt circuit and low-voltage detection reset circuit. The detection levels can also be set as desired because the power supply rise detection voltage, power supply drop detection voltage, and reference voltage can be input from an external LSI.

The low-voltage detection circuit registers are described below.

- Low-Voltage Detection Control Register (LVDCR)
  LVDCR is an 8-bit readable/writable register. This register controls whether to use the low-voltage detection circuit (the LVDE bit), setting of the external input of detection levels when the power-supply voltage drops or rises (the VINTDSEL and VINTUSEL bits), setting of detection levels for the low-voltage detection reset circuit (LVDR) (the LVDSEL bit), whether to enable or disable a reset triggered by the low-voltage detection reset circuit (LVDR) (the LVDRE bit), and whether to enable or disable interrupts when power-supply voltage drops and rises (the LVDDE and LVDUE bits).
- Low-Voltage Detection Status Register (LVDSR)
  LVDSR is an 8-bit readable/writable register. This register is used to select an external input of the reference voltage (the VREFSEL bit), indicate that the reference voltage is stable (the OVF bit) and whether the power-supply voltage goes below or above a specified range (the LVDDF and LVDUF bits).
- Low-voltage detection counter (LVDCNT)
  LVDCNT is an 8-bit read-only up-counter. LVDCNT starts counting when 1 is written to the LVDE bit of the LVDCR register. LVDCNT increments using $\phi/4$ as the clock source. When LVDCNT overflows from H'FF to H'00, the OVF bit of LVDSR is set to 1, indicating that the internal reference voltage generation circuit has stabilized. To use the LVD function, it is necessary to wait until this counter overflows. The initial value of the counter is H'00.

A block diagram of the low-voltage detection circuit is shown in figure 2.

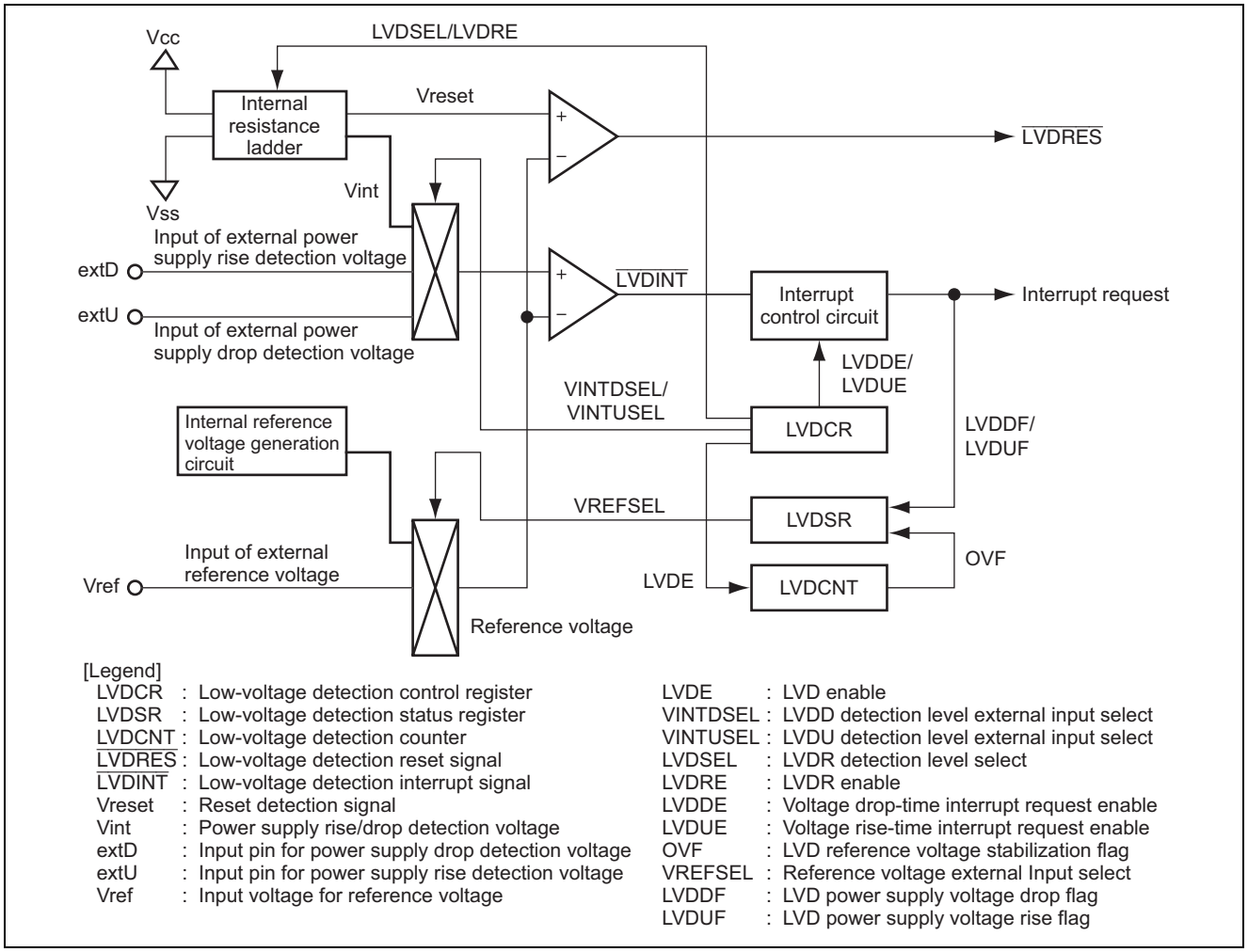


Figure 2 Block Diagram of Low-Voltage Detection Circuit

Use the following procedure to set the circuit for normal operation and release of the low-voltage detection circuit. The timing for setting operation and release of the low-voltage detection circuit are shown in figure 3, the flow is shown in figure 4.

1. To start operation of the low-voltage detection circuit, first set the LVDE bit of the LVDCR register to 1.
2. Wait until the reference voltage and the low-voltage detection power supply stabilize (t_{LVDON} = 150 µs) (that is, until LVDCNT overflows), clear the LVDDF and LVDUF bits of the LVDSR register to 0, and set the LVDRE, LVDDE, and LVDUE bits of the LVDCR register to 1 as required.
3. To release the low-voltage detection circuit, clear the LVDRE, LVDDE, and LVDUE bits to 0 then clear the LVDE bit to 0. Do not clear the LVED bit simultaneously with the LVDRE, LVDDE, and LVDUE bits, since doing so will result in a malfunction.

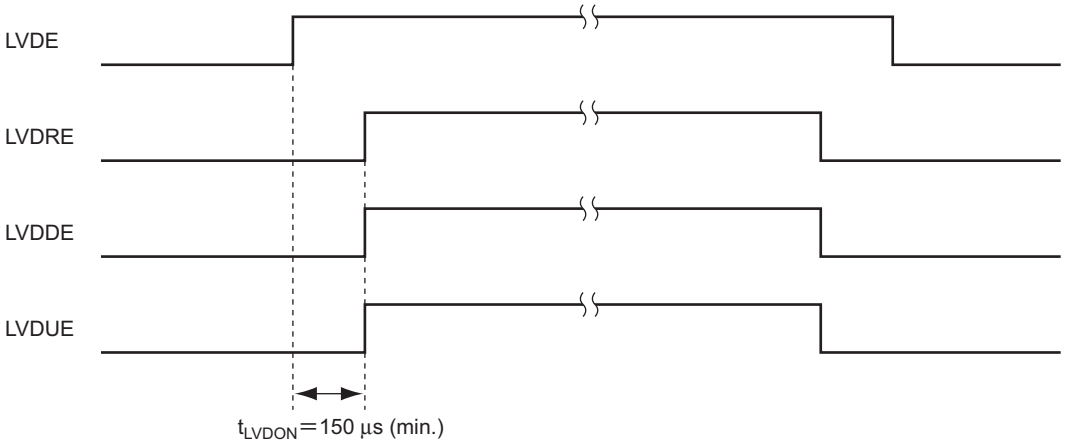
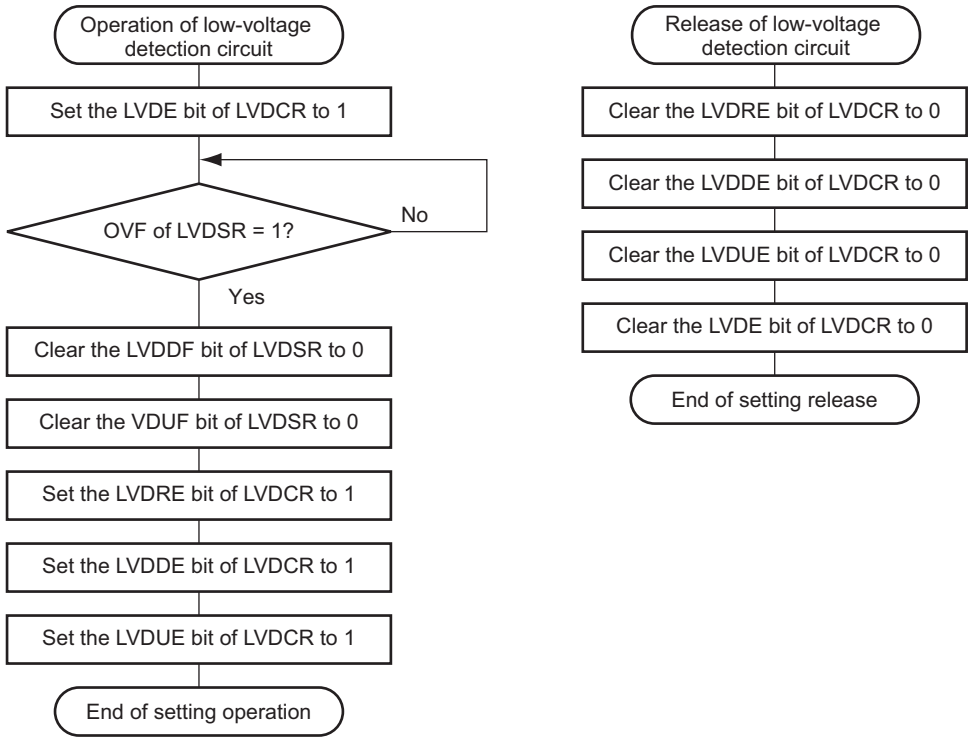


Figure 3 Timing for Setting Low-Voltage Detection Circuit Operation and Release



Note: Do not clear the LVDE bit of LVDCR to 0 simultaneously with the LVDRE, LVDDE, and LVDUE bits, since doing so will result in a malfunction .

Figure 4 Flow of Procedures for Setting Low-Voltage Detection Circuit Operation and Release

(2) Watchdog timer

The H8/38124 has an internal watchdog timer. When a reset is cleared, the watchdog timer is turned on, and Timer Counter W (TCW) is incremented. When TCW overflows, the H8/38124 is internally reset. In this sample task, the watchdog timer function is stopped because it is not used. The watchdog timer registers are described below.

- Timer Control/Status Register W (TCSRW)
  TCSRW is an 8-bit readable/writable register. This register controls TCSRW and writing to TCW (the B6WI, TCWE, B4WI, TCSRWE, B2WI, B0WI bits), controls watchdog timer operation (the WDON bit), and indicates the operating state of the watchdog timer (the WRST bit).
- Timer Counter W (TCW)
  TCW is an 8-bit readable/writable up-counter. This counter is incremented based on the internal clock that is input. The clock that is input is selected according to the settings of Timer Mode Register W (TMW) when the WDCKS bit (Watchdog Timer Source Clock Select) of PMR2 (Port Mode Register 2) is 0. When the WDCKS bit is 1, $\phi w/32$ is selected. TCW values can always be read from and written to by the CPU. When TCW overflows (H'FF→H'00), an internal reset signal is generated and the WRST bit of the TCSRW register is set to 1. TCW is initialized to H'00 when a reset occurs.
- Timer Mode Register W (TMW)
  TMW selects a TCW input clock according to combinations of CKS3 to CKS0 (Clock Select). This selection is valid only when the WDCKS bit of PMR2 is 0.

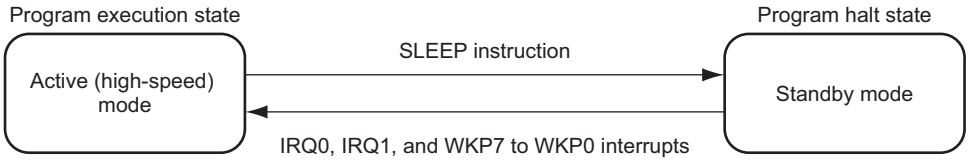
(3) Power-down mode (standby mode)

If a SLEEP instruction is executed in the active mode when the SSBY bit of the System Control Register 1 (SYSCR1) is 1, the LSON bit of the same register is 0, and the TMA3 bit of the TMA register is 0, the H8/38124 enters the standby mode. In the standby mode, the CPU and internal peripheral modules stop because clock supply from the clock generation circuit is stopped. As long as the stipulated voltage is supplied, data in all CPU registers, some of the internal registers of the internal peripheral modules, and data in the internal RAM are retained. Also, as long as the voltage stipulated as the RAM data retention voltage is supplied, internal RAM data is retained. In the standby mode, the I/O port goes to the high-impedance state.

The standby mode is canceled by an interrupt (IRQ1, IRQ0, WKP7 to WKP0) or an input of the $\overline{\text{RES}}$ signal.
For release of the standby mode by an interrupt, when an interrupt request is issued, system clock oscillation is started, stable system clock pulses are supplied to the entire LSI after the time set by the STS2 to STS0 bits of the SYSCR1 register has elapsed, and the standby mode is canceled. At this point, interrupt exception handling is initiated. When the MSON bit of the System Control Register 2 (SYSCR2) is 0, the H8/38124 switches to the active (high-speed) mode. When this bit is 1, the H8/38124 switches to the active (medium-speed) mode. However, the standby mode is not canceled if the I bit of the Condition Code Register (CCR) is 1 or acceptance of the relevant interrupt is disabled by the setting of the Interrupt Enable Register.

For release of the standby mode by the $\overline{\text{RES}}$ signal, when the $\overline{\text{RES}}$ signal is driven low, system clock oscillation is started. When the $\overline{\text{RES}}$ signal goes high after the time for oscillation stabilization has elapsed, the CPU starts reset exception handling. When system clock oscillation is started, system clocks are supplied to the entire LSI at the same time. Make sure that the $\overline{\text{RES}}$ signal is held low until system clock oscillation has become stable.
The power-down mode registers are described below. A block diagram of the transition from the active (high-speed) mode to the standby mode is shown in figure 5.

- System Control Register 1 (SYSCR1)
  SYSCR1 controls the power-down mode jointly with the SYSCR2 register.
- System Control Register 2 (SYSCR2)
  SYSCR2 controls the power-down mode jointly with the SYSCR1 register.



SLEEP instruction execution conditions

LSON	MSON	SSBY	TMA3	DTON
0	0	1	0	0

Figure 5 Transition from the Active (High-Speed) Mode to the Standby Mode

(4) Power-down mode (module standby mode)

The module standby mode can be set separately for each peripheral module. All the internal peripheral modules can be set to the module standby mode. When a peripheral module is set to the module standby mode, system clock supply to the module is halted. The peripheral module stops and then enters the same state as the standby mode.

The module standby mode is set by clearing the corresponding bit of Clock Stop Register 1 (CKSTPR1) and Clock Stop Register 2 (CKSTPR2) to 0.

This sample task sets all peripheral modules other than LVD (low-voltage detection circuit) to the module standby mode.

Module standby mode registers are described below.

- Clock Stop Register 1 (CKSTPR1)
  CKSTPR1 controls setting of the following: the timer A module standby mode (the TACKSTP bit), the timer C module standby mode (the TCCKSTP bit), the timer F module standby mode (the TFCKSTP bit), the timer G module standby mode (the TGCKSTP bit), the A/D converter module standby mode (the ADCKSTP bit), and the SCI3 module standby mode (the S32CKSTP bit). Clearing each bit to 0 sets the corresponding module in the module standby mode. Setting each bit to 1 takes the corresponding module out of the module standby mode. After a reset is cleared, the CKSTPR1 register is initialized to H'FF.
- Clock Stop Register 2 (CKSTPR2)
  CKSTPR2 controls setting of the following: the LCD module standby mode (the LDCKSTP bit), the PWM1 module standby mode (the PW1CKSTP bit), the watchdog timer module standby mode (the WDCKSTP bit), the asynchronous event counter module standby mode (the AECKSTP bit), the PWM2 module standby mode (the PW2CKSTP bit), and the LVD module standby mode (the LVDCKSTP bit). Clearing each bit to 0 sets the corresponding module in the module standby mode. Setting each bit to 1 takes the corresponding module out of the module standby mode. After a reset is cleared, the CKSTPR2 register is initialized to H'FF.

(5) Exception handling (IRQ0 interrupt)

The voltage drop- and rise-time interrupt requests used in this sample task are issued as IRQ0 interrupt requests.

(6) I/O port (port 9)

In this sample task, an LED is connected to the P90 pin. This LED lights when a low level signal is output from this pin. When the active (high-speed) mode switches to the standby mode, the P90 pin enters the high-impedance state. The port 9 register is described below.

- Port Data Register 9 (PDR9)
  PDR9 is an 8-bit register in which data for the P95 to P90 pins of port 9 is stored. When a reset occurs, the PDR9 register is initialized to H'FF.

2.2 Function Assignment

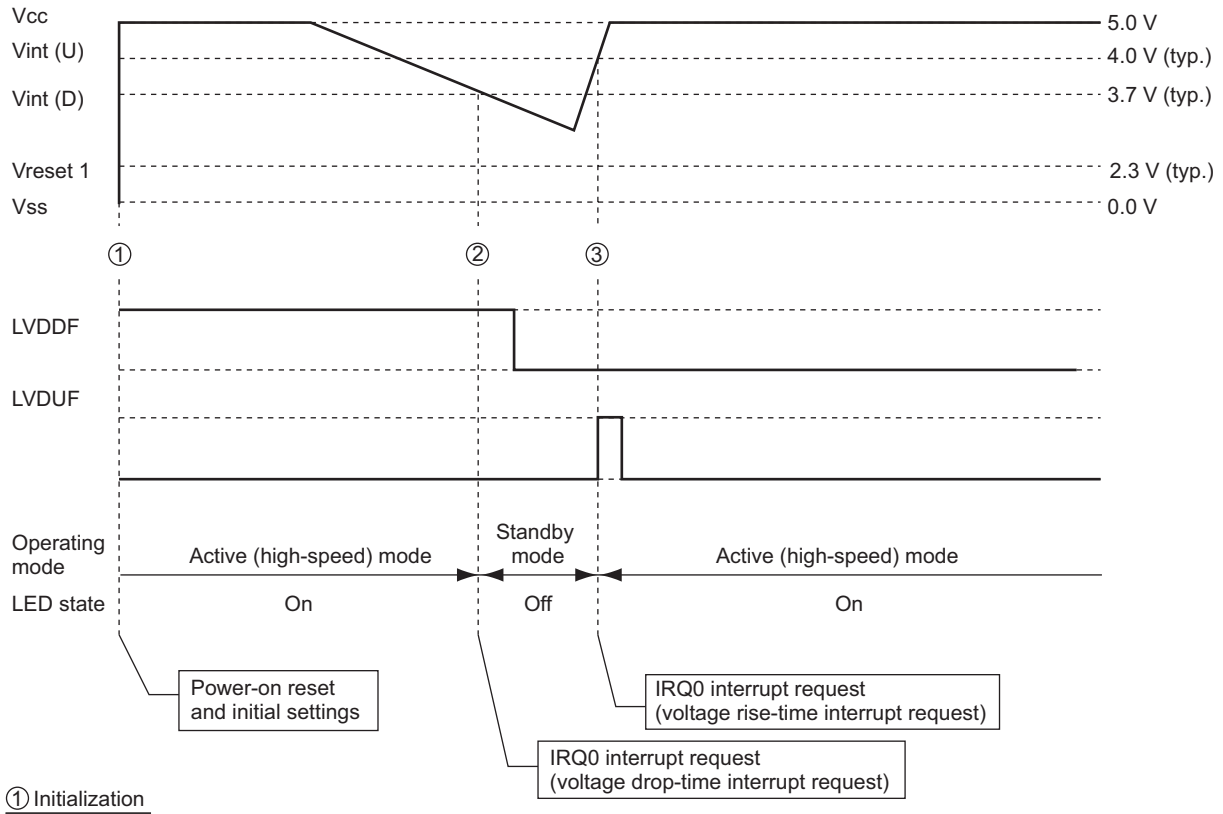
Function assignments in this sample task are listed in table 1.

Table 1 Assignment of Functions

Element	Description
LVDCR	Sets whether to use the low-voltage detection circuit, sets the power-supply voltage drop and rise detection levels to the voltage generated by the internal resistance ladder, sets the reset detection voltage to 2.3 V (typ.), enables reset by LVDR, and enables power-supply voltage drop and rise interrupts.
LVDSR	Determines reference voltage stabilization and power-supply voltage drop and rise, and sets the reference voltage to be generated by the internal circuit.
LVDCNT	Determines stabilization of the internal reference voltage generation circuit by waiting for an counter overflow.
TCSRW	Sets watchdog timer operation to be disabled.
SYSCR1	Controls the transition between the active (high-speed) mode and the standby mode jointly with the SYSCR2 register.
SYSCR2	Controls the transition between the active (high-speed) mode and the standby mode jointly with the SYSCR1 register.
CKSTPR1	Sets timers A, C, F, and G, the A/D converter, and the SCI3 to the module standby mode.
CKSTPR2	Sets LCD, PWM1, the watchdog timer, the asynchronous event counter, and the PWM2 to the module standby mode and takes the LVD out of the module standby mode.
PDR9	Sets the data to be output from the P90 output pin.

3. Principles of Operation

The principles of operation of low-voltage detection (with an internal reference voltage used) using the low-voltage detection circuit are illustrated in figure 6.



① Initialization

The low-voltage detection interrupt circuit (LVDI) enters the module standby mode after a power-on reset is canceled. LVDI operation is started by setting the LVDE bit of LVDCR to 1, waiting until the reference voltage and low-voltage detection power supply have stabilized (t_{LVDON} = 150 µs) (that is, until LVDCNT overflows), and then setting the LVDDE and LVDUE bits of LVDCR to 1.
After these operations, the port must be set to output.

② When the power-supply voltage drops

When the power-supply voltage drops to Vint(D) (typ. = 3.7 V) or lower, LVDI sets the LVDDF bit of LVDSR to 1. At this time, if the LVDDE bit is 1, LVDI issues an IRQ0 interrupt request. After IRQ0 interrupt processing, LVDI clears the LVDDF bit to 0 and the H8/38124 switches to the standby mode.

③ When the power-supply voltage rises

If the LVDUE bit is 1 when the power-supply voltage rises to Vint(U) (typ. = 4.0 V) or higher without dropping to Vreset1 (typ. = 2.3 V), LVDI sets the LVDUF bit of LVDSR to 1 and, at the same time, issues an IRQ0 interrupt request. After IRQ0 interrupt processing, LVDI clears the LVDUF bit to 0 and the H8/38124 returns to the active (high-speed) mode.

Note: When the power-supply voltage drops to Vreset 1 (typ. = 2.3 V) or lower, the H8/38124 performs a low-voltage detection reset operation and prescaler S is reset. The low-voltage detection reset state continues until a power-on reset is initiated. When the power-supply voltage rises again to Vreset1 or higher, prescaler S starts incrementing, counts ϕ 131,072 times, and cancels the internal reset signal. At this point, the LVDE, LVDSEL, and LVDRE bits of the LVDCR register are not initialized. Note that if the power supply voltage drops to $V_{LVDRmin}$ = 1.0 V or lower and rises again from that level, low-voltage detection reset may not be operated. Furthermore, if the power-supply voltage drops to Vpor = 100 mV or lower, the H8/38124 performs a power-on reset.

Figure 6 Principles of Operation

4. Description of Software

4.1 Description of Modules

The modules of this sample task are described in table 2.

Table 2 Modules

Function Name	Description
main	Stops the watchdog timer, sets the module standby mode, initializes the low-voltage detection circuit, sets LED output, enables interrupts, switches the active (high-speed) mode to the standby mode or vice versa, and releases the low-voltage detection circuit.
int_irq0	Determines the IRQ0 and LVD interrupt routines, voltage drop time, and voltage rise time.

4.2 Description of Internal Registers Used

This section describes the internal registers used in this sample task.

- Low Voltage Detection Control Register (LVDCR) Address: H'FF86

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	LVDE	0*	R/W	LVD Enable Controls operation and stopping of the low-voltage detection circuit. 0: Does not use the low-voltage detection circuit (standby state). 1: Uses the low-voltage detection circuit.	1
5	VINTDSEL	0	R/W	LVDD Detection Level External Input Select Selects a power-supply voltage drop detection level. 0: Generates an LVDD detection level with the internal resistance ladder. 1: Inputs an LVDD detection level from the extD pin.	0
4	VINTUSEL	0	R/W	LVDU Detection Level External Input Select Selects a power-supply voltage rise detection level. 0: Generates an LVDU detection level with the internal resistance ladder. 1: Inputs an LVDU detection level from the extU pin.	0
3	LVDSEL	0*	R/W	LVDR Detection Level Select Selects an LVDR detection level. 0: Reset detection voltage of 2.3 V (typ.) 1: Reset detection voltage of 3.3 V (typ.)	0
2	LVDRE	0*	R/W	LVDR Enable Enables or disables reset by LVDR. 0: Disables reset by LVDR. 1: Enables reset by LVDR.	1
1	LVDDE	0	R/W	Voltage Drop-Time Interrupt Request Enable Enables or disables voltage drop-time interrupt requests. 0: Disables voltage drop-time interrupt requests. 1: Enables voltage drop-time interrupt requests.	1
0	LVDUE	0	R/W	Voltage Rise-Time Interrupt Request Enable Enables or disables voltage rise-time interrupt requests. 0: Disables voltage rise-time interrupt requests. 1: Enables voltage rise-time interrupt requests.	1

Note: * This bit is not initialized even if a reset by LVDR is performed. This bit is initialized by a power-on reset or a watchdog timer reset.

- Low-Voltage Detection Status Register (LVDSR) Address: H'FF87

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	OVF	0*	R/W	LVD Reference Voltage Stabilization Flag Indicates that the low-voltage detection counter (LVDCNT) overflowed. [Clearing condition] When 0 is written to this bit after 1 has been read. [Setting condition] When the low-voltage detection counter (LVDCNT) overflows.	0
3	VREFSEL	0	R/W	Reference Voltage External Input Select Selects the reference voltage. 0: Uses the voltage of the internal circuit as the reference voltage. 1: Inputs the reference voltage from the Vref external pin.	0
1	LVDDF	0*	R/W	LVD Power Supply Voltage Down Flag Indicates that a power supply voltage drop was detected. [Clearing condition] When 0 is written to this bit after 1 has been read. [Setting condition] If the power-supply voltage drops to Vint(D) or lower.	0
0	LVDUF	0*	R/W	LVD Power Supply Voltage Up Flag Indicates that a power supply voltage rise was detected. [Clearing condition] When 0 is written to this bit after 1 has been read. [Setting condition] If the power-supply voltage drops to Vint(D) or lower while the LVDUE bit of LVDCR set to 1 and then rises to Vint(U) or higher before it drops to Vreset1 or lower.	0

Note: * This bit is initialized when a reset by LVDR is performed.

- Low-Voltage Detection Counter (LVDCNT) Address: H'FFC3

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	CNT7	0	R	LVDCNT is an 8-bit read-only up-counter. When a 1 is written to LVDE, LVDCNT starts counting. LVDCNT increments using ϕ/4 as the clock source. When LVDCNT overflows from H'FF to H'00, the OVF bit of LVDSR is set to 1, indicating that the internal reference voltage generation circuit became stable. To use the LVD function, you must wait until this counter overflows.	—
6	CNT6	0	R		—
5	CNT5	0	R		—
4	CNT4	0	R		—
3	CNT3	0	R		—
2	CNT2	0	R		—
1	CNT1	0	R		—
0	CNT0	0	R		—

- Timer Control/Status Register W (TCSRW) Address: H'FFB2

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	B6WI	1	R	Bit 6 Write Disable Enables/disables writing of data to bit 6 of TCSRW. 0: Enables writing to TCWE. 1: Disables writing to TCWE.	1
6	TCWE	0	R/(W)*	Timer Counter W Write Enable Enables/disables writing of data to TCW. 0: Disables writing to TCW. 1: Enables writing to TCW.	0
5	B4WI	1	R	Bit 4 Write Disable Enables/disables writing of data to bit 4 of TCSRW. 0: Enables writing to TCSRWE. 1: Disables writing to TCSRWE.	0
4	TCSRWE	0	R/(W)*	Timer Control/Status Register W Write Enable Enables/disables writing of data to bit 2 of TCSRW. 0: Disables writing to WDON and WRST. 1: Enables writing to WDON and WRST.	1
3	B2WI	1	R	Bit 2 Write Disable Enables/disables writing of data to bit 2 of TCSRW. 0: Enables writing to WDON. 1: Disables writing to WDON.	0
2	WDON	1	R/(W)*	Watchdog Timer On Enables/disables watchdog timer operation. 0: Disables watchdog timer operation. [Clearing condition] If a reset is performed, or 0 is written to WDON when 0 is written to B2WI while TCSRWE is set to 1. 1: Enables watchdog timer operation. [Setting condition] If 1 is written to WDON when 0 is written to B2WI while TCSRWE is set to 1.	0
1	B0WI	1	R	Bit 0 Write Disable Enables/disables writing to bit 0 of TCSRW. 0: Enables writing to WRST. 1: Disables writing to WRST.	1

0	WRST	0	R/W*	Watchdog Timer Reset Indicates that TCW overflowed and that an internal reset signal occurred. [Clearing conditions] (1) If a reset by the $\overline{\text{RES}}$ signal is performed. (2) If 0 is written to WRST when 0 is written to B0WI while TCSRWE is set to 1. [Setting condition] If TCW overflows and an internal reset signal is generated.	0

Note: * Writing is enabled only when the write conditions are satisfied.

- System Control Register 1 (SYSCR1) Address: H'FFF0

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	SSBY	0	R/W	Software Standby Specifies a transition to the standby mode or the watch mode. 0: Specifies a transition to the sleep mode after the SLEEP instruction has been executed in the active mode. Alternatively, specifies a transition to the sub-sleep mode after the SLEEP instruction has been executed in the sub-active mode. 1: Specifies a transition to the standby mode or the watch mode after the SLEEP instruction has been executed in the active mode. Alternatively, specifies a transition to the watch mode after the SLEEP instruction has been executed in the sub-active mode.	1
6	STS2	0	R/W	Standby Timer Select 2 to 0 Specifies the time during which the CPU and peripheral functions must wait until the H8/38124 cancels the standby mode or the watch mode and then switches to the active mode with a specified interrupt. Specify this standby time so that it is equal to or greater than the oscillation stabilization time that is determined by the operating frequency. 000: Standby time = 8,192 states 001: Standby time = 16,384 states 010: Standby time = 32,768 states 011: Standby time = 65,536 states 100: Standby time = 131,072 states 101: Standby time = 2 states 110: Standby time = 8 states 111: Standby time = 16 states Note: This sample task uses a 4.194304-MHz crystal oscillator as the system clock.	0
5	STS1	0	R/W		1
4	STS0	0	R/W		1
3	LSON	0	R/W	Low Speed On Flag Selects whether to use the system clock (ϕ) or the sub-clock (ϕ_{SUB}) as the CPU operating clock when the watch mode is canceled. The CPU operating clock is determined by combinations of other control bits and interrupt inputs. 0: Uses the system clock (ϕ) as the CPU operating clock. 1: Uses the sub-clock (ϕ_{SUB}) as the CPU operating clock.	0

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
1	MA1	1	R/W	Active (Medium-Speed) Mode Clock Select	1
0	MA0	1	R/W	Selects an active or sleep (medium-speed) mode operating clock. Writing a value to MA1 and MA0 is valid only in the active (high-speed) mode or the sub-active mode. 00: ϕosc/16 01: ϕosc/32 10: ϕosc/64 11: ϕosc/128	1

- System Control Register 2 (SYSCR2) Address: H'FFF1

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
4	NESEL	1	R/W	Noise Elimination Sampling Frequency Select Selects the watch clock (ϕ_W) generated by a sub-clock oscillator or the OSC clock (ϕ_{OSC}) generated by a system clock oscillator to sample frequencies. If ϕ_{OSC} is 2 to 20 MHz, 0 is set. 0: Uses the ϕ_{OSC} divide-by-16 to sample frequencies. 1: Uses the ϕ_{OSC} divide-by-4 to sample frequencies.	0
3	DTON	0	R/W	Direct Transfer On Flag Specifies whether to permit direct transition between the active (high-speed) mode, the active (medium-speed) mode, and the sub-active mode when the SLEEP instruction is executed. The operating mode switched to after the SLEEP instruction is executed is determined from combinations of the control bits other than this bit. 0: (1) Switches to the standby mode, watch mode, or sleep mode when the SLEEP instruction is executed in the active mode. (2) Switches to the watch mode or the sleep mode when the SLEEP instruction is executed in the sub-active mode. 1: (1) Directly switches to the active (medium-speed) mode (when SSBY = 0, MSON = 1, and LSON = 0) or the sub-active mode (when SSBY = 1, TMA3 = 1, and LSON = 1) when the SLEEP instruction is executed in the active (high-speed) mode. (2) Directly switches to the active (high-speed) mode (when SSBY = 0, MSON = 0, and LSON = 0) or the sub-active mode (when SSBY = 1, TMA3 = 1, and LSON = 1) when the SLEEP instruction is executed in the active (medium-speed) mode. (3) Directly switches to the active (high-speed) mode (when SSBY = 1, TMA3 = 1, LSON = 0, and MSON = 0) or the active (medium-speed) mode (SSBY = 1, TMA3 = 1, LSON = 0, and MSON = 1) when the SLEEP instruction is executed in the sub-active mode.	0

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
2	MSON	0	R/W	Middle Speed On Flag Selects whether to operate the system in the active (high-speed) mode or in the active (medium-speed) mode after the standby mode, watch mode, and sleep mode are canceled. 0: Operates the system in the active (high-speed) mode. 1: Operates the system in the active (medium-speed) mode.	0
1	SA1	0	R/W	Sub-Active Mode Clock Select	0
0	SA0	0	R/W	Selects a CPU operating clock for the sub-active mode. The SA1 and SA0 values are not updated even if data is written in the sub-active mode. 00: $\phi_W/8$ 01: $\phi_W/4$ 1x: $\phi_W/2$ Note: x: Don't care	0

- Clock Stop Register 1 (CKSTPR1) Address: H'FFFA

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
5	S32CKSTP	1	R/W	SCI3 Module Standby Mode Control 0: Sets SCI3 to the module standby mode. 1: Cancels the module standby mode for SCI3.	0
4	ADCKSTP	1	R/W	A/D Converter Module Standby Mode Control 0: Sets the A/D converter to the module standby mode. 1: Cancels the module standby mode for the A/D converter.	0
3	TGCKSTP	1	R/W	Timer G Module Standby Mode Control 0: Sets timer G to the module standby mode. 1: Cancels the module standby mode for timer G.	0
2	TFCKSTP	1	R/W	Timer F Module Standby Mode Control 0: Sets timer F to the module standby mode. 1: Cancels the module standby mode for timer F.	0
1	TCCKSTP	1	R/W	Timer C Module Standby Mode Control 0: Sets timer C to the module standby mode. 1: Cancels the module standby mode for timer C.	0
0	TACKSTP	1	R/W	Timer A Module Standby Mode Control 0: Sets timer A to the module standby mode. 1: Cancels the module standby mode for timer A.	0

- Clock Stop Register 2 (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	LVDCKSTP	1	R/W	LVD Module Standby Mode Control 0: Sets LVD to the module standby mode. 1: Cancels the module standby mode for LVD.	1
4	PW2CKSTP	1	R/W	PWM2 Module Standby Mode Control 0: Sets PWM2 to the module standby mode. 1: Cancels the module standby mode for PWM2.	0
3	AECKSTP	1	R/W	AEC Module Standby Mode Control 0: Sets AEC to the module standby mode. 1: Cancels the module standby mode for AEC.	0
2	WDCKSTP	1	R/W	WDT Module Standby Mode Control 0: Sets WDT to the module standby mode. 1: Cancels the module standby mode for WDT.	0
1	PW1CKSTP	1	R/W	PWM1 Module Standby Mode Control 0: Sets PWM1 to the module standby mode. 1: Cancels the module standby mode for PWM1.	0
0	LDCKSTP	1	R/W	LCD Module Standby Mode Control 0: Sets LCD to the module standby mode. 1: Cancels the module standby mode for LCD.	0

- Port Data Register 9 (PDR9) Address: H'FFDC

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
0	P90	1	R/W	P90 Data Register 0: P90 pin output is 0. 1: P90 pin output is 1.	0

4.3 RAM Usage

The RAM usage in this sample task is described in table 3.

Table 3 RAM Used

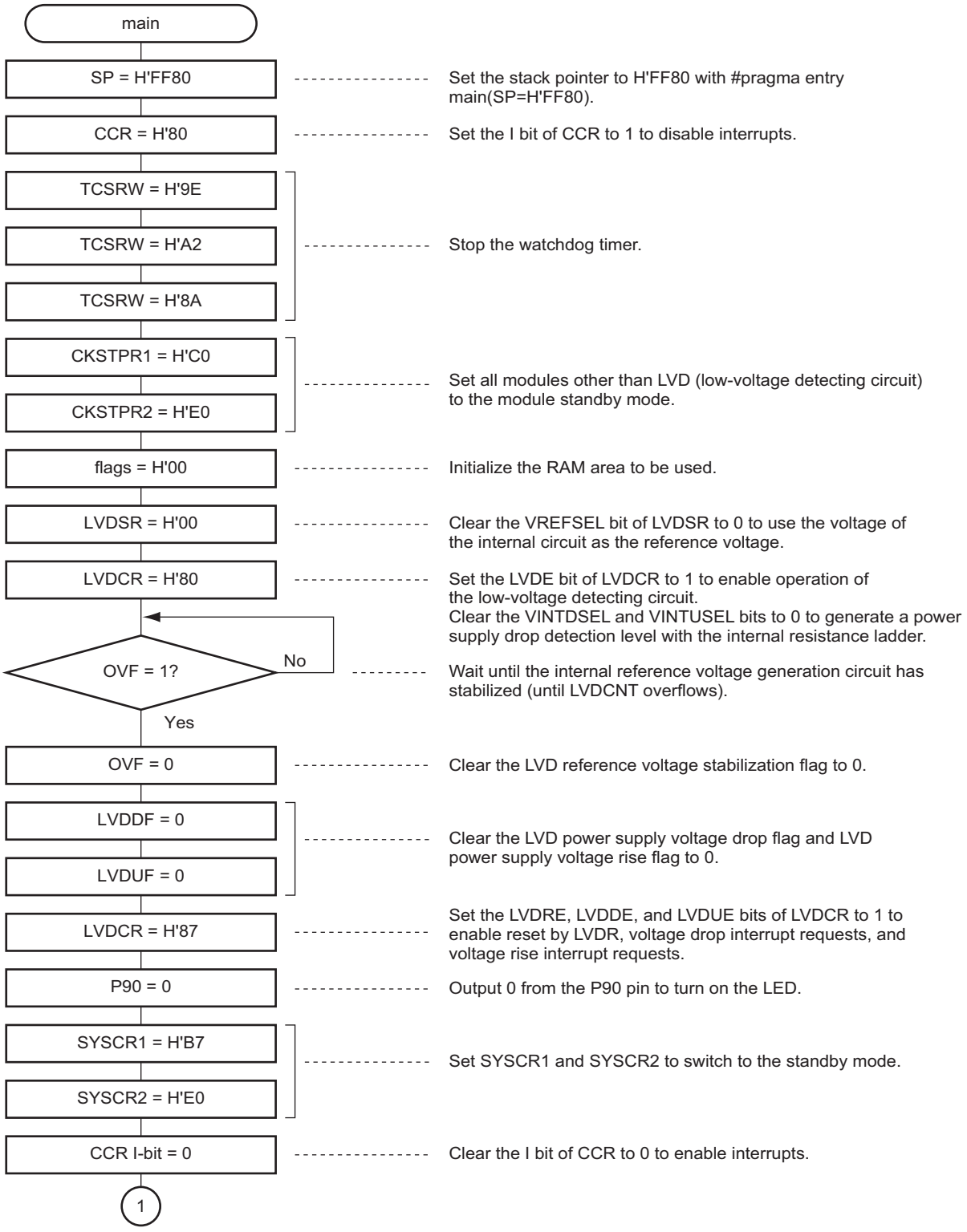
Variable Name	Description	Amount of Memory	Function Name
flags	Flag storage	1 byte	main, int_irq0

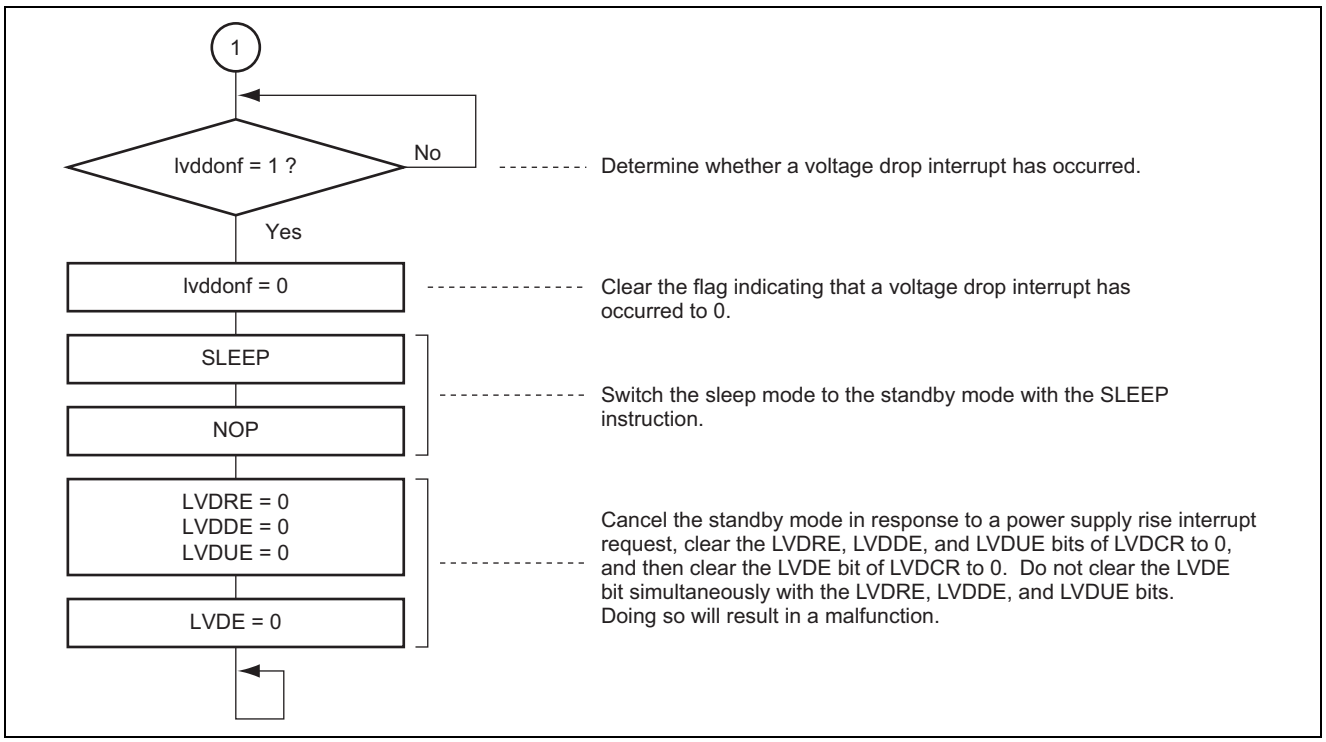
- Flags Address: H'FB80

Bit	Bit Name	Initial Value	Description
7	lvddonf	0	Flag indicating that a power-supply voltage drop interrupt occurred
6	—	0	Unused
5	—	0	
4	—	0	
3	—	0	
2	—	0	
1	—	0	
0	—	0	

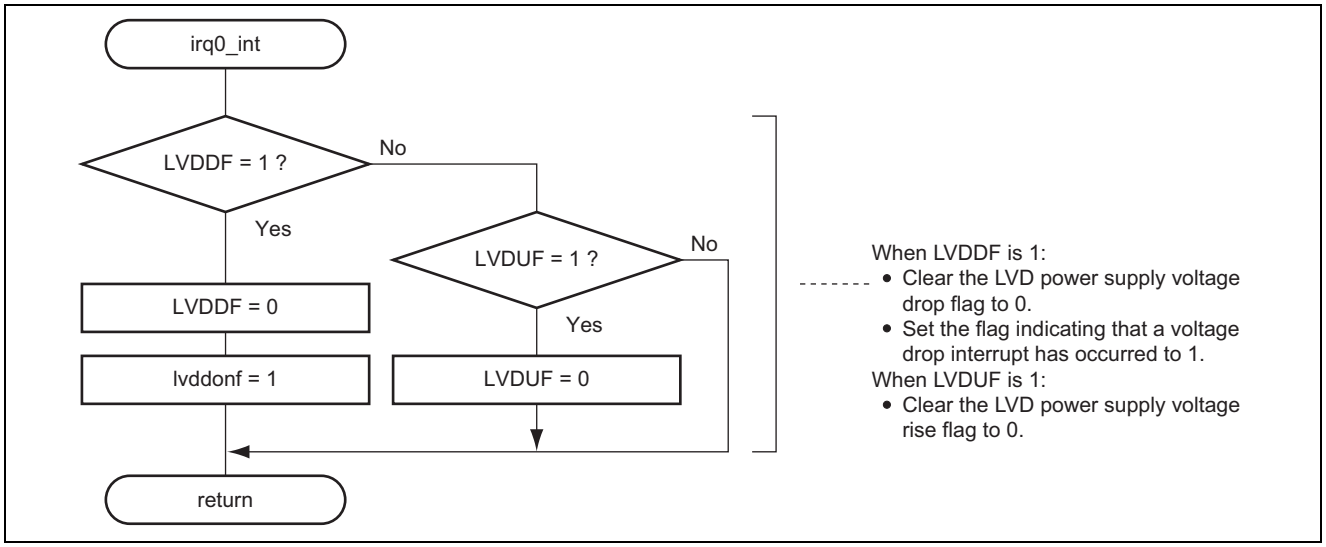
5. Flowcharts

5.1 main





5.2 int_irq0



5.3 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.13.05	—	First edition issued

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