# Layout Recommendations for FemtoClock 3 Devices

This application note provides board layout guidelines for FemtoClock 3 devices (RC32312, RC22312, RC32308, and RC22308).

## Contents


1. Introduction ........ 1
2. Power ........ 1
3. Thermal Considerations ........ 3
4. Crystal ........ 5
5. Clock Input and Output Routing ........ 6
6. Layer Stack-Up ........ 6
7. Revision History ........ 9


## 1. Introduction

To get the best performance from a FemtoClock 3 (FC3) device, the board layout must follow certain guidelines as described in this application note.

## 2. Power

Renesas recommends a dedicated power plane or power distribution network. Each FC3 device should have a dedicated LDO near the device on the same layer. Having dedicated power helps minimize voltage fluctuations and noise caused by other components sharing the same power supply network and keeps noise from switching power supplies from causing spurs on the outputs of the FC3. A short LDO output trace from a dedicated LDO will ensure a low IR drop between the LDO and the device since the trace has a lower inductance and a higher current carrying ability. In addition, the FC3 device should be kept away from noisy components such as switching regulators, high-current traces.

Please follow these general recommendations:

- Do not overlay power trace/plane from the two power layers.
- Do not run power lines parallel/adjacent for long stretches, even if they are of different layers.
- Cross power trace from different layers at 90 degrees if the crossing is necessary.
- Keep power trace as thick as possible (while keeping a generous spacing to adjacent power lines) for lower resistance and lower inductance.

Of the power pins on the device, $V_{DDA}$ is most sensitive to external noise while $V_{DD_DIG}$ is the noisiest. These two pins should be separated by a power supply pi-decoupling filter similar to the design in Figure 1. In the power supply-decoupling filter, place the 0.1μF bypass capacitors of as close as possible to the power supply pins of the FC3 device (see C49 in Figure 1). A second 10μF capacitor near the device is also recommended if there is room. These capacitors help filter out high-frequency noise and provide a stable power supply. For additional filtering, we recommend a 4.7μF or 10μF capacitor with a larger package before the ferrite bead (see C46 and C47 in Figure 1). If possible, avoid using vias and place the capacitors on the same layer as the device.


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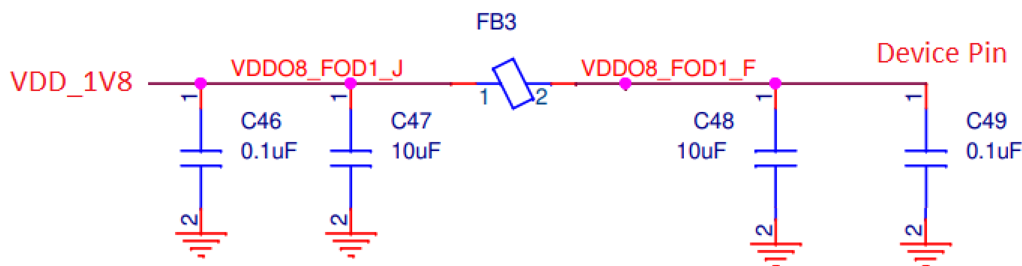



**Figure 1. Example Decoupling Schematic Structure**

The ground plane in the design should be a solid and low-impedance ground plane dedicated for clock devices. The ground pins of FC3 should be directly to this ground plane, minimizing ground loops and reducing ground noise.

Renesas recommends that the design avoids unnecessary power plane below the FC3 device, so that supply noise and other currents don't couple into the sensitive clock circuitry.

In Figure 2, the blue area indicates where the power plane under the entire timing device should be part of an isolated plane with a single connection to ground at the device. This will ensure shorter loops and better isolation.

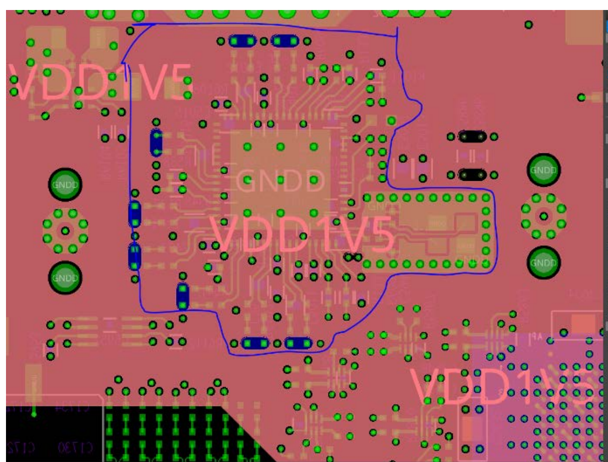


**Figure 2. Example Design Showing Power Planes Below Device with Different Layers Visible**

# 3. Thermal Considerations

Renesas recommends a layout pattern with vias similar to Figure 3 on the top layer. This provides sufficient heat transfer from the FC3 device to the substrate and a good ground for the device since this device does not have a ground pin. Figure 4 shows the ground layer under the device with yellow arrows indicating the heat dissipation paths. The heat will couple from the top layer to the ground layer using the vias. In addition, the bottom layer of the device is shown in Figure 5. The recommended decoupling capacitors from section 2 “Power” need a large number of vias, which need to be considered when looking at the heat flow from the device to the board.

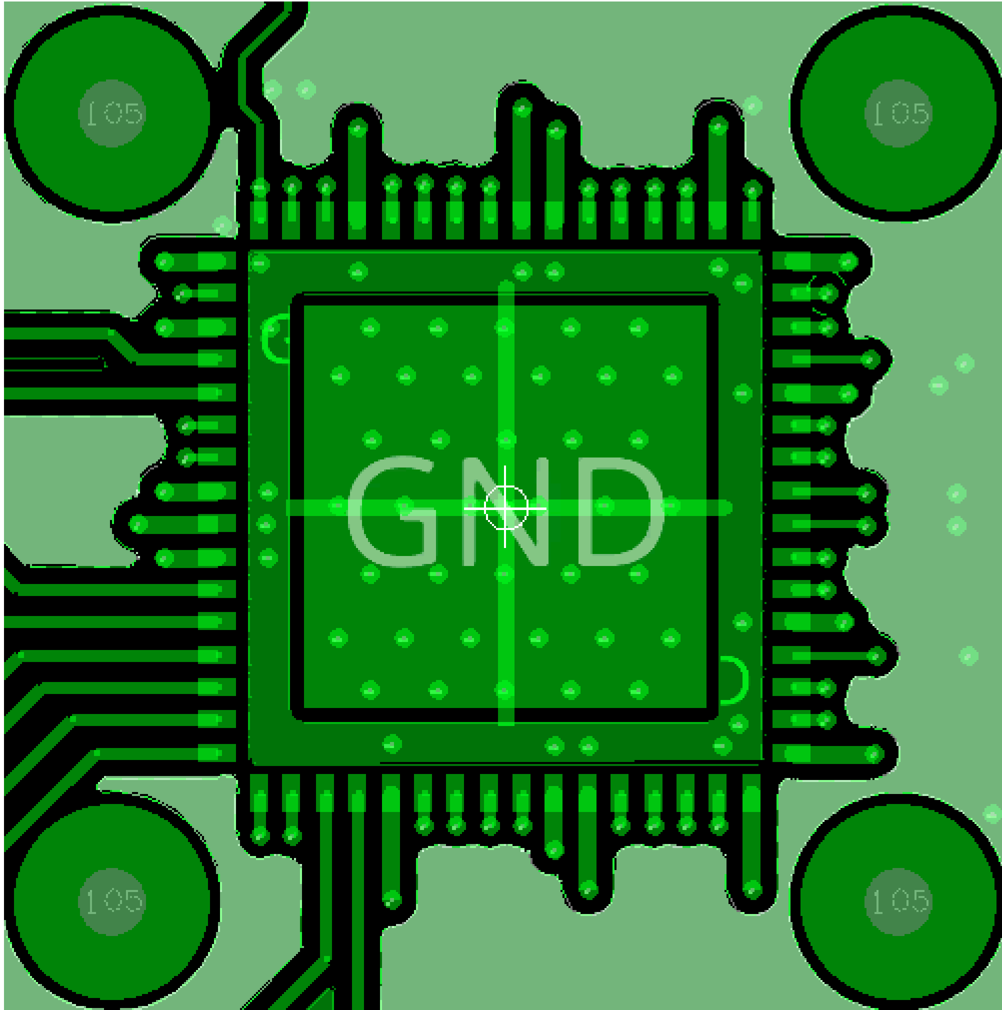



**Figure 3. EPAD Layout Example on Top Layer**

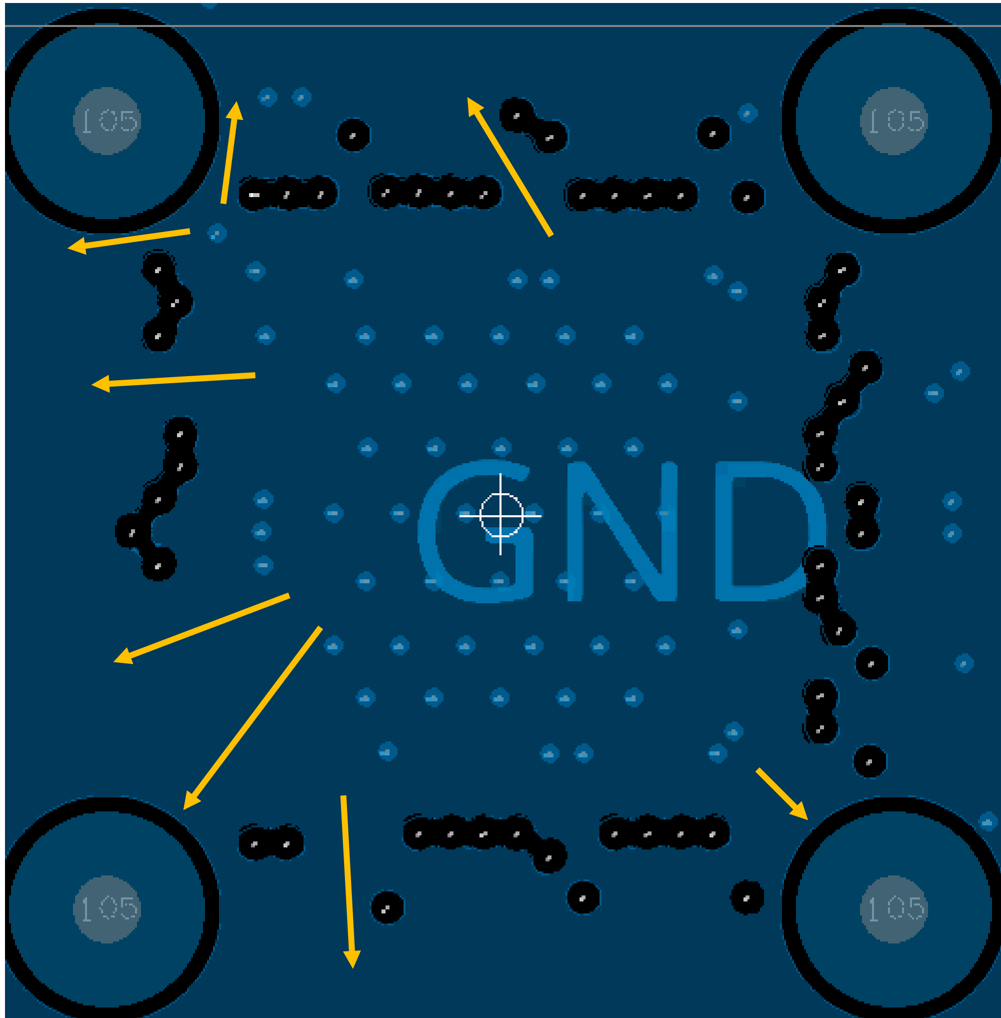



Figure 4. EPAD Layout Example on Layer 2 (ground)

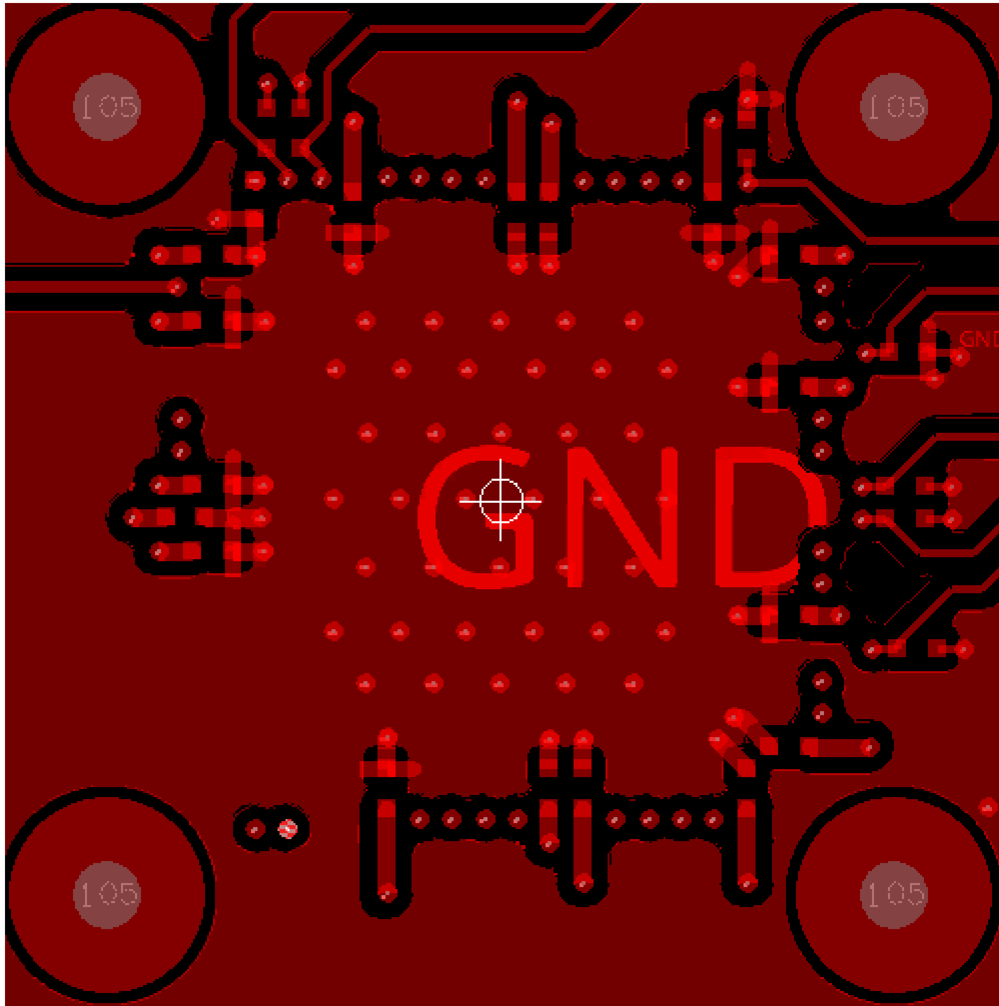



Figure 5. EPAD Layout Example on Bottom Layer

## 4. Crystal

As with all timing devices, careful attention is needed on the crystal circuit to ensure best device performance. For the traces connecting the crystal to the device, the XOUT is low-impedance and XIN is high-impedance. To minimize noise coupling, XIN and XOUT should be as short as possible.

Renesas recommends a GND plane channel (~3mil) around the crystal to isolate it from noise on the plane. The design needs to ensure that the load capacitors have a common ground plane.

Other signals should not cross the crystal 'keep-out' area to minimize noise from coupling into the crystal traces or grounds. A crystal layout example is shown in Figure 6.

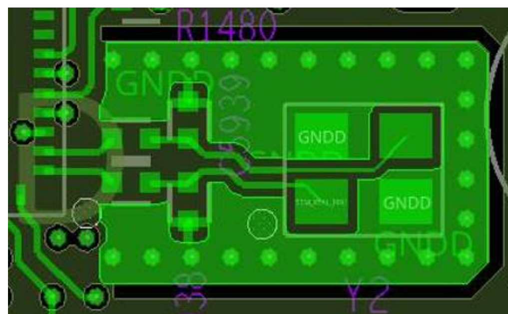



Figure 6. Crystal Layout Example

# 5. Clock Input and Output Routing

Clock signals need to be routed carefully due to their sensitivity to noise and reflections.

The differential clock traces should be routed as 100Ω signal pairs with impedance control per the PCB fabricator. The layout should minimize the use of vias. The signal should only switch layers at the driver and at the termination since the stubs from the vias will add reflections.

If needed due to space, clocks from the same domain (frequency and phase) can run parallel. Clocks from different domains should not run parallel, though an exception may be made if they are on different signal layers and separated by multiple ground layers.

If space is available around the output clocks, then ground stitching can be added around the differential pair to prevent board noise from coupling to the signal.

For inputs, the termination should be placed near the receiver to minimize reflections. The reference ground via should be placed as close as possible to the source or receiver of the differential clock pair and ensure that the reference ground via connects to a continuous ground plane.

# 6. Layer Stack-Up

A PCB consists of multiple layers of copper (foil) and isolation materials laminated together. PCB layer stack-up design refers to the layer arrangement of copper and dielectric material layers with the total number of layers and the thickness of each layer taking into considerations.

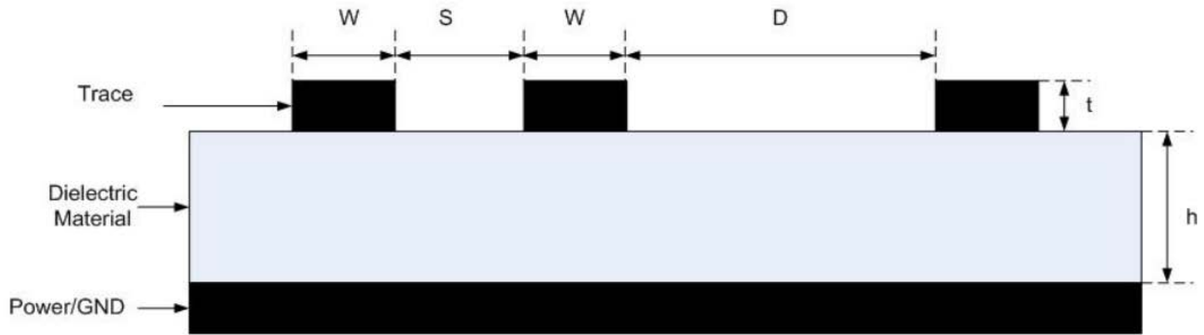
Planning optimal multi-layer stack-up is one of the most critical factors in determining electromagnetic compatibility performance of a PCB. A well-designed layer stack-up can both minimize the radiation and stay robust from external noise sources.

Figure 7 and Figure 8 illustrate the significance and relationships of signal impedance and EMC control with the PCB layer stack-up.

A signal trace that is suspended over a ground plane with a dielectric layer between them is called a microstrip. The impedance of the microstrip trace is determined by a number of factors in the PCB and its stack-up arrangement:

- Signal trace width
- Thickness of the trace (thickness of copper layer)
- Distance between the two traces if it is a differential pair
- Thickness of the dielectric layer between a microstrip and the ground plane under the dielectric layer
- Dielectric constant Er

The microstrip structure is shown in Figure 7 and the impedance is shown in Figure 8. For more information on microstrip standards, see ANSI IPC-D-317A.




**Microstrip Transmission Line Layout**

W = Width of trace
t = Thickness of trace
h = Height between trace and reference plane
S = Space between two traces of a differential pair
D = Space between two adjacent differential pairs

**Figure 7. Microstrip Signal Example**

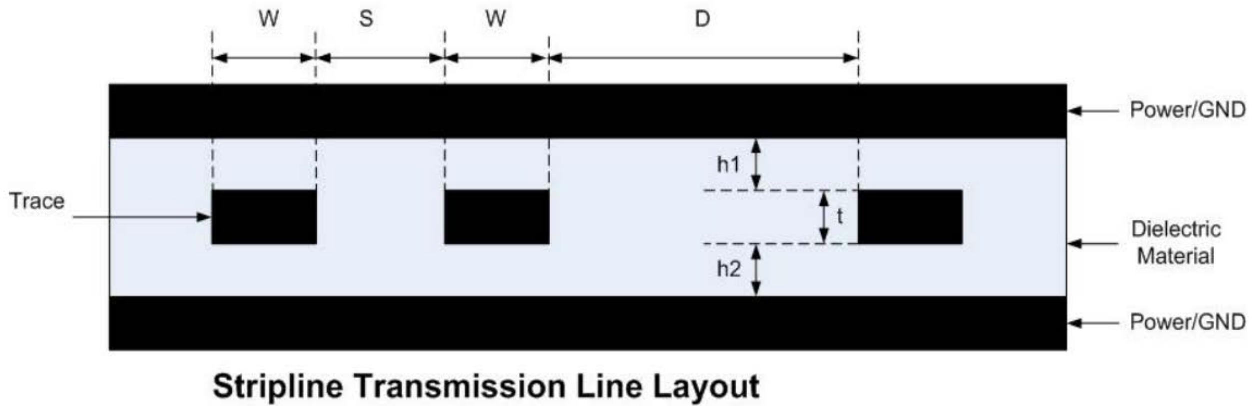
$$Z_o = \frac{60}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left[\frac{4h}{0.67(0.8w+t)}\right] ohms$$

$$Z_{diff} \cong 2Z_o\left(1 - 0.48e^{-0.96\frac{s}{h}}\right) ohms$$

**Figure 8. Microstrip Signal Impedance**

When a signal trace changes layers, the above factors affecting trace impedance change as well. Caution must be exercised in order to keep the signal impedance continuous to avoid signal integrity impairments.

Another signal type is called a stripline signal, which is one sandwiched between two dielectric material layers. The stripline structure is shown in Figure 9 and the impedance is shown in Figure 10.




W = Width of trace
t = Thickness of trace
S = Space between two traces of a differential pair
D = Space between two adjacent differential pairs

**Figure 9. Stripline Signal Example**

$$Zo = \frac{60}{\sqrt{\varepsilon_r}} \times \ln\left(\frac{1.9(2(h1 + h2) + t)}{0.67\pi(0.8w + t)}\right)$$

$$Zdiff = 2 \times Zo\left(1 - 0.374\, e^{-2.9\left[\frac{s}{h1 + h2}\right]}\right)$$

**Figure 10. Stripline Signal Impedance**

For a design with FC3, Renesas recommends that the clock signals are protected from ambient noise by using the stripline internal trace structure (sandwiching them between two ground planes).

The FC3 evaluation board (Rev C) stack-up is shown in Figure 11.

- This EVB uses an 8-layer board.
- There are five copper planes for power and ground – three layers are ground, and one layer is dedicated to power. The SIG_3 layer is between ground layers GND2 and GND4 and the SIG_7 layer is between ground layers GND6 and BOTTOM. This generous number of ground and power planes will help the board's EMC performance.

  *Note*: Depending on signal density, not every PCB board can dedicate such an abundant number of copper planes.
- The evaluation board uses Nanya NPLD-II material due to its low losses at the frequency supported by this device. Other Renesas boards that support similar maximum clock frequencies have used other FR4 materials for similar performance.

| STACKUP TABLE | | | | |
|---|---|---|---|---|
| Unit = Mils | | | | |
| # | NAME | TYPE | MATERIAL | THICKNESS |
| | | SURFACE | AIR | 0 |
| | SOLDERMASK_TOP | MASK | NANYA NPLD-II | 1 |
| 1 | TOP | CONDUCTOR | 1OZ_COPPER | 1.4 |
| | | DIELECTRIC | NANYA NPLD-II | 4.6 |
| 2 | GND2 | PLANE | 1OZ COPPER | 1.4 |
| | | DIELECTRIC | NANYA NPLD-II | 10 |
| 3 | SIG_3 | CONDUCTOR | 1OZ_COPPER | 1.4 |
| | | DIELECTRIC | NANYA NPLD-II | 4.6 |
| 4 | GND4 | PLANE | 1OZ_COPPER | 1.4 |
| | | DIELECTRIC | NANYA NPLD-II | 10 |
| 5 | PWR5 | PLANE | 1OZ COPPER | 1.4 |
| | | DIELECTRIC | NANYA NPLD-II | 4.6 |
| 6 | GND6 | PLANE | 1OZ COPPER | 1.4 |
| | | DIELECTRIC | NANYA NPLD-II | 10 |
| 7 | SIG_7 | CONDUCTOR | 1OZ_COPPER | 1.4 |
| | | DIELECTRIC | NANYA NPLD-II | 4.6 |
| 8 | BOTTOM | CONDUCTOR | 1OZ_COPPER | 1.4 |
| | SOLDERMASK BOTTOM | MASK | NANYA NPLD-II | 1 |
| | | SURFACE | AIR | 0 |
| | | | TOTAL THICKNESS | 61.6 |

**Figure 11. Stack-up Example for FC3**

# 7. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | Jun 16, 2023 | Initial release. |

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