RL78/G24

Interleaved CrM PFC and LLC Control with RL78/G24 (Hardware & Software Basics)

Abstract

This application note describes how to implement constant voltage control by combining an interleaved CrM PFC with an LLC using the features of the RL78/G24 microcontroller.

Target Device

RL78/G24

Board

RL78/G24 Interleaved PFC + LLC Board 400W Kit (RTK0EL0006D00000BJ)

Note: When applying the sample application to other microcontrollers, modify it according to the specifications of that microcontroller and evaluate it thoroughly.

Related Documents

- Interleaved CrM PFC and LLC Control Using RL78/G24(FAA Software) (RA01AN8176)
- Interleaved CrM PFC and LLC Control Using RL78/G24(CPU Software) (RA01AN8177)
- RL78/G24 User's Manual: Hardware (R01UH0961)

Contents

1. Introduction

This application note describes the fundamental hardware and software concepts of a PFC and LLC digital power system using the RL78/G24 microcontroller.

For more detailed information on software operation, please also refer to the following application notes:
“Interleaved CrM PFC and LLC Control Using RL78/G24(FAA Software)” (R01AN8176) and
“Interleaved CrM PFC and LLC Control Using RL78/G24(CPU Software)” (R01AN8177).

1.1 Features of Digital Power Using the RL78/G24

The RL78/G24-based digital power solution enables both high efficiency and low power consumption during light-load and standby operation by optimizing PWM control patterns and flexibly switching operating modes through software.

Control sequences and fine PWM tuning that are difficult to realize with conventional analog control can be easily implemented using digital control with the RL78/G24, which incorporates dedicated hardware.

This flexibility and improved power efficiency simplify compliance with energy regulations and reduce heat dissipation, allowing smaller cooling components such as heat sinks and contributing to overall power system cost reduction.

More specific features are described below.

- The RL78/G24 integrates advanced dedicated peripherals optimized for digital power applications. For instance, the PWM output capability of the 16-bit Timer KBn and the timer restart function using an external interrupt or comparator provide hardware-level support for CrM PFC control and LLC converter control, enabling basic converter operation.
  With feedback control performed by the CPU or FAA, this microcontroller can achieve high-efficiency and high power-factor PFC and LLC control.
- The RL78/G24 also provides functions for power supply protection. The forced output shutdown function of Timer KBn, operating in conjunction with a high-speed comparator or external interrupt, enables immediate and asynchronous shutdown upon detection of overcurrent or overvoltage in the PFC or LLC circuit, without intervention by the CPU or FAA, thereby protecting the device and surrounding components.
  Since this function is implemented in hardware, it guarantees fast and reliable shutdown with no software-induced latency. Furthermore, recovery from an emergency shutdown can be managed by software, allowing flexible design of restart sequences and protection release conditions to meet system requirements.
- The RL78/G24 incorporates a 32-bit independently operating coprocessor known as the Flexible Application Accelerator (FAA). Operating separately from the CPU, the FAA can rapidly execute power control feedback calculations, allowing real-time control loops to be processed without CPU involvement.
  This improves feedback response and reduces CPU load, enabling the CPU to dedicate resources to communication tasks and higher-level system control, thereby achieving high overall control performance and system stability.
- The RL78/G24 integrates peripheral functions supporting commonly used communication interfaces, including UART, SPI, PMBus/SMBus, and infrared (IR).
  For instance, remote control signal reception can be implemented using the pulse interval measurement function of the 16-bit Timer Array Unit, thereby reducing CPU load during data reception.

2. Hardware Description

This section describes the hardware used in this application note.

2.1 Specifications

2.1.1 Input/Output Specifications

The input/output specifications are listed in Table 2.1.

Table 2.1 Input/Output Specifications

Item			Content	Remarks
Input		Voltage	$90V_{AC}$ – $264V_{AC}$	This represents the assumed operating range of the hardware. The operating voltage ranges addressed by the program in this application note are 90-110 V, 220-240 V.
		Frequency	50/60Hz	
		Maximum Power	400W	
Output	PFC	Rated Voltage	$386V_{DC}$	LLC Input Voltage
		Maximum Current	1.044A	
	LLC1 (Output 1)	Rated Voltage	$13V_{DC}$ ±5%	
		Maximum Current	6.0A	
		Maximum Power	78W	
	LLC2 (Output 2)	Rated Voltage	$50V_{DC}$ ±5%	
		Maximum Current	6.5A	
		Maximum Power	325W	
	Others	Power Factor	0.96 or higher	
		Overall Efficiency	95% or higher	
		Standby Power	0.3W or lower	Standby Mode, Output 1 = 0.15W when loaded

2.1.2 Protection Functions

This board provides both hardware protection functions, implemented by the comparators and timers integrated in the microcontroller, and software protection functions realized through program operation. This section describes the hardware-based protection functions. For details on the software protection functions, refer to Section 3.3.1.

In addition, these hardware protection functions enable rapid abnormality detection and operation shutdown without software intervention. For specific stop times, refer to Section 22.4.6 of the *RL78/G24 User's Manual: Hardware*.

2.1.2.1 PFC OCP

The source current of the PFC MOSFET is converted into a voltage and applied to the comparator of the RL78/G24. When the input voltage exceeds the reference voltage set by the RL78/G24's D/A converter, the 16-bit timer function forces the PFC output to stop. This function is defined as PFC OCP (Over Current Protection).

In this sample program, the OCP detection threshold is set to the equivalent of 12 A for both the master and slave terminals.

2.1.2.2 LLC OCP

The resonant current of the LLC is converted into a voltage and applied to the comparator of the RL78/G24. When the input voltage exceeds the reference voltage set by the RL78/G24's D/A converter, the function forces the output of the corresponding LLC to stop. This function is defined as LLC OCP (Over Current Protection).

In this sample program, the OCP detection threshold is set based on the measured peak voltage of the CS signal under rated load conditions, with an additional 20% margin.

The OCP detection threshold for LLC1 is set to 4.2V (measured peak voltage of 3.5V under rated load), and the OCP detection threshold for LLC2 is set to 3.6V (measured peak voltage of 3.0V under rated load).

2.1.3 Other

Other hardware specifications are listed in Table 2.2.

Table 2.2 Other Specifications

Item	Specifications
Withstand Voltage Design Specifications	Input-FG, Input-Output 300V_{AC} for 1 minute
Insulation Resistance Design Specifications	Input-FG, Input-Output 30MΩ or more / 500V_{DC}
ESD Resistance Design Specifications	9KV
Size	305mm * 315mm
Ambient Temperature	0–40℃
Ambient Humidity	20–85%RH

2.2 Board Appearance

2.2.1 Main Board

The appearance of the main board is shown below.

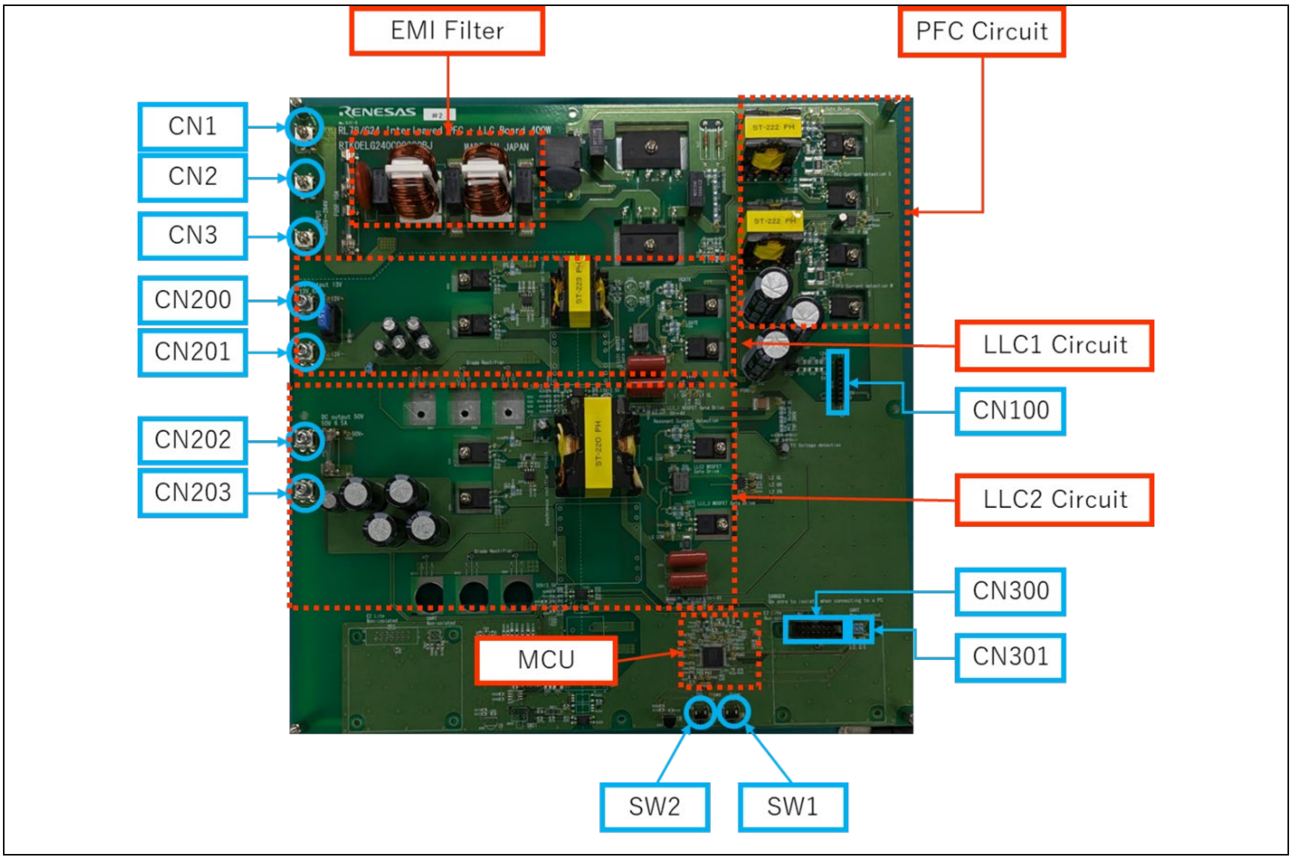


Figure 2.1 Main Board Appearance Photo

The main board's input/output pins are listed in Table 2.3.

Table 2.3 Main Board Input/Output Pin List

Terminal	I/O	Function	Remarks
CN1	I	FG	90–264V_{AC}
CN2	I	AC (L) Input	
CN3	-	AC (N)	
CN200	O	Output 1 (+)	6.0A Max
CN201	O	Output 1 (-)	
CN202	O	Output 2 (+)	6.5A Max
CN203	O	Output 2 (-)	
CN100	I/O	IPD Board	
CN300	I/O	Debug Board	
CN301	I/O	Debug Board	

2.2.2 IPD Circuit Board

The appearance of the IPD board is shown below.

Figure 2.2 IPD Board Appearance Photo

The IPD board's input/output pins are listed in Table 2.4.

Table 2.4 IPD Board Input/Output Pin List

Terminal	I/O	Function	Remarks
1	I	Vin	
2	-	N/A	
3	-	N/A	
4	-	N/A	
5	-	N/A	
6	-	N/A	
7	O	12V out	
8	O	5V out	
9	I	GND	

2.2.3 Debug Board

The appearance of the debug board is shown below.

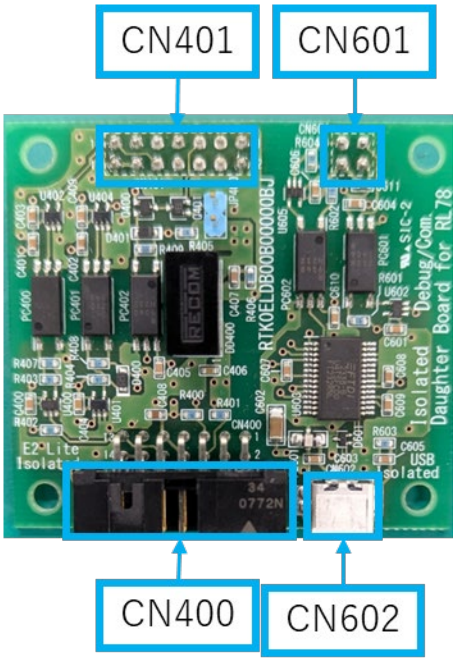


Figure 2.3 Debug Board Appearance Photo

The debug board's input/output pins are listed in Table 2.5.

Table 2.5 Debug Board Input/Output Pin List

Terminal	I/O	Function	Remarks
CN400	I/O	E2 lite connection pin	
CN401	I/O	Connected to main board CN300	
CN601	I/O	Connected to main board CN301	
CN602	I/O	USB pin	

2.3 Hardware Configuration

The hardware consists of multiple components, as shown in Figure 2.4. Each component is described below.

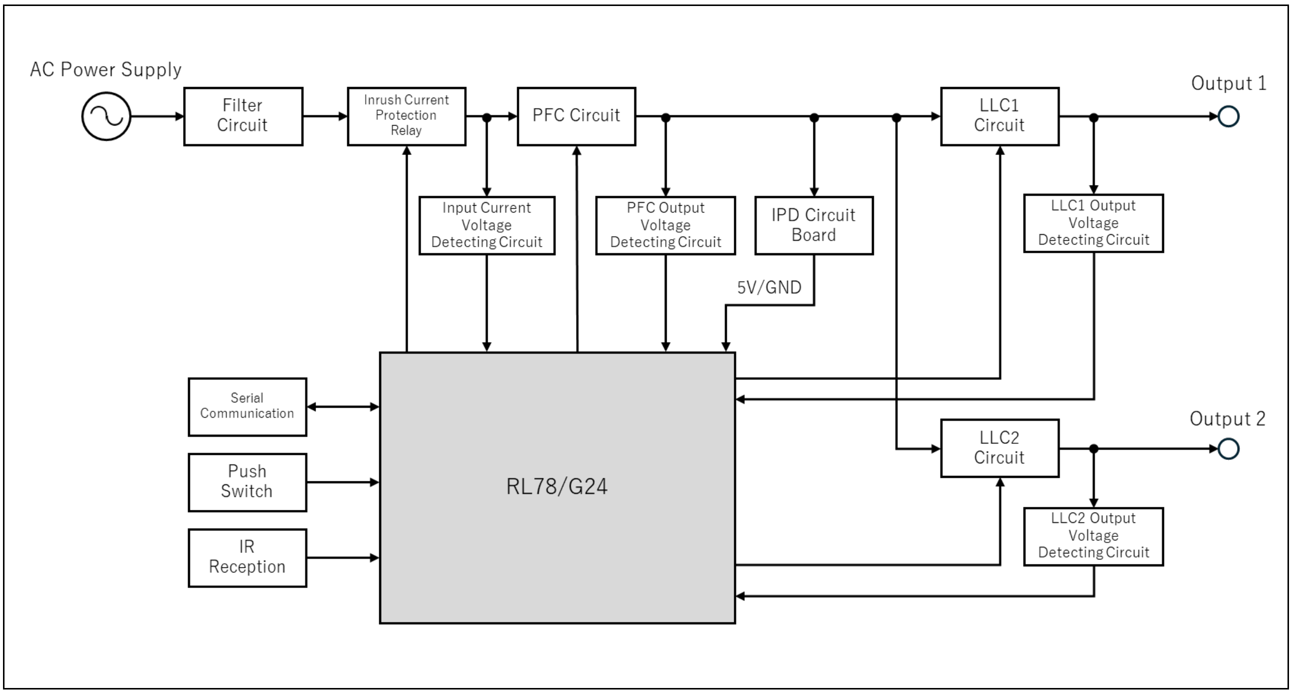


Figure 2.4 Hardware Block Diagram

2.3.1 Inrush Current Protection Relay

When switching power supplies are turned on, a large current flows into the smoothing condenser. This is called “Inrush Current”. Unless countermeasures are taken against inrush current, it can damage electronic components and affect the lifespan of the smoothing condenser. The target board uses an NTC thermistor (RT1) that can simply and effectively limit inrush current. Although the internal resistance of the NTC thermistor constantly generates power loss, reducing efficiency, the relay is switched ON/OFF according to the operating mode to control the path of the input current I_{in}, thereby improving efficiency.

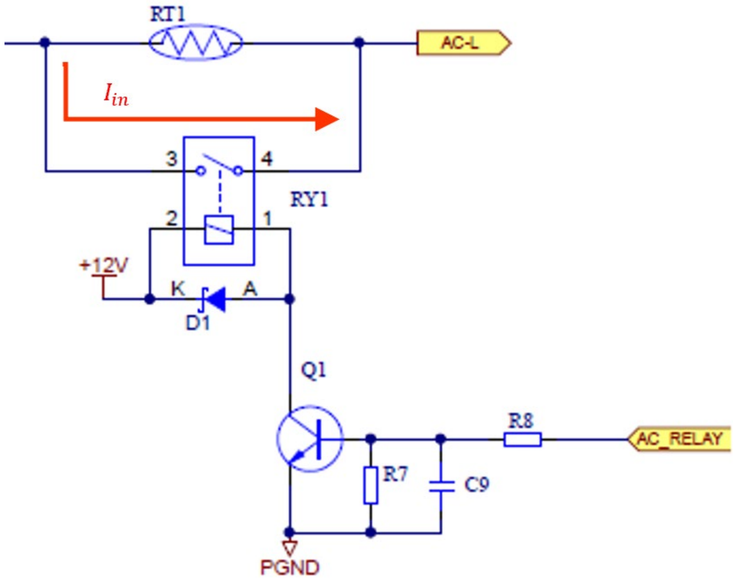


Figure 2.5 Inrush Current Protection Relay Circuit

2.3.2 AC Voltage Sense Circuit (AC_V)

This circuit detects the rectified voltage of the AC input as an analog input. To enable detection as an analog input for the RL78/G24, the voltage is divided via a resistor, and the resulting voltage is designated as AC_V.

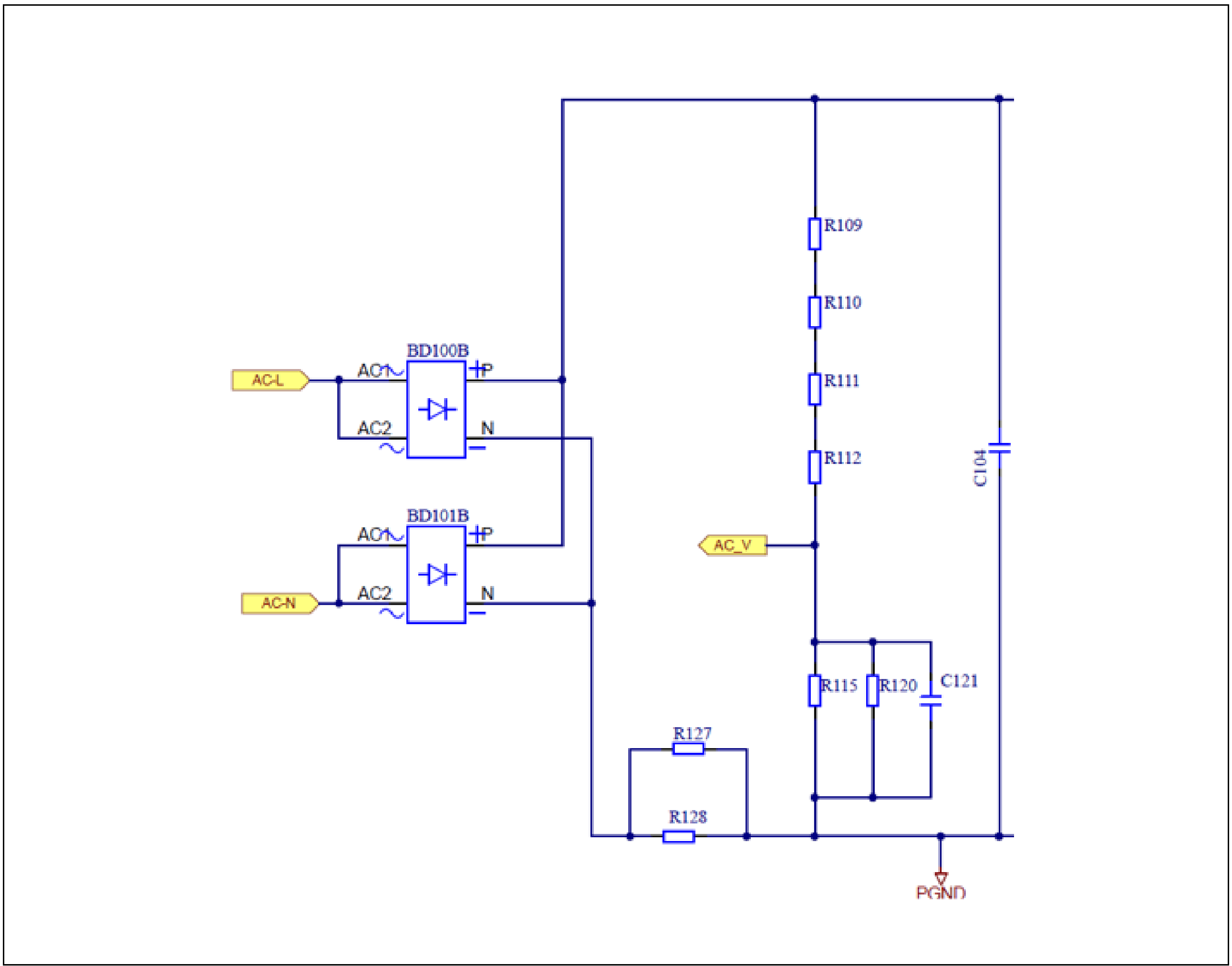


Figure 2.6 AC Input Voltage Detection Circuit

The AC_V voltage is calculated using the following equation. Here, $V_{AC\_IN\_PEAK}$ denotes the peak value of the AC consumption current.

$$AC\_V = V_{AC\_IN\_PEAK} \times \frac{(R115+R120)}{(R109+R110+R111+R112)+(R115+R120)}$$

2.3.3 AC Current Sense Circuit (AC_CS)

A simplified circuit for detecting AC power consumption current is shown in Figure 2.7. By multiplying the current I_{FB_PEAK} flowing through the current detection resistors R127 and R128, the magnitude of the current can be detected. To reduce power loss and increase the detection voltage, low-inductance resistors and an amplifier are employed. The detection accuracy can be further enhanced by using a metering microcontroller such as the RL78/I1B or RL78/I1C, or by employing an RMS converter.

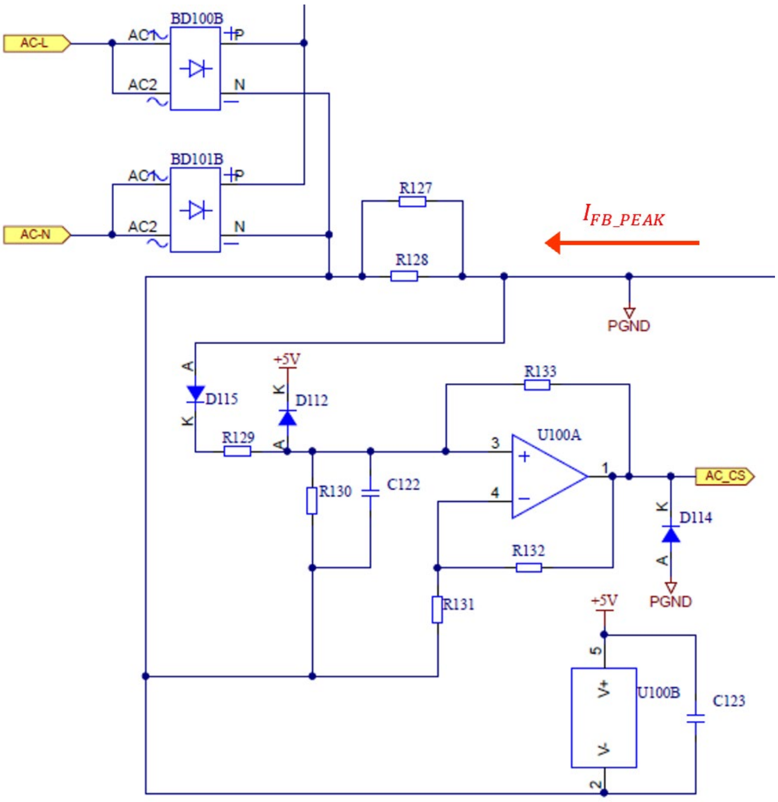


Figure 2.7 AC Current Sense Circuit

The voltage of AC_CS is obtained using the following equation.

$$\text{AC\_CS} = I_{\text{FB PEAK}} \times \left(\frac{R127 \times R128}{R127 + R128}\right) \times \text{Gain}$$

$$\text{Note: Gain} = 1 + \frac{\text{R132}}{\text{R131}}$$

2.3.4 PFC Circuit

2.3.4.1 Overview of Circuit Control

The PFC circuit consists of two boost converters operating in critical conduction mode. The input/output relationship between the PFC circuit and the microcontroller is shown in Figure 2.8.

By periodically monitoring the load, the RL78/G24 appropriately switches between single output and interleaved output depending on the load level, thereby achieving high efficiency across a wide load range. During interleaved output operation, a 180° phase shift is required. However, with the interleaved PFC function of the RL78/G24's Timer KB, the phase is automatically adjusted, suppressing ripple. This design reduces output ripple current and enables downsizing and cost reduction of the input/output filters.

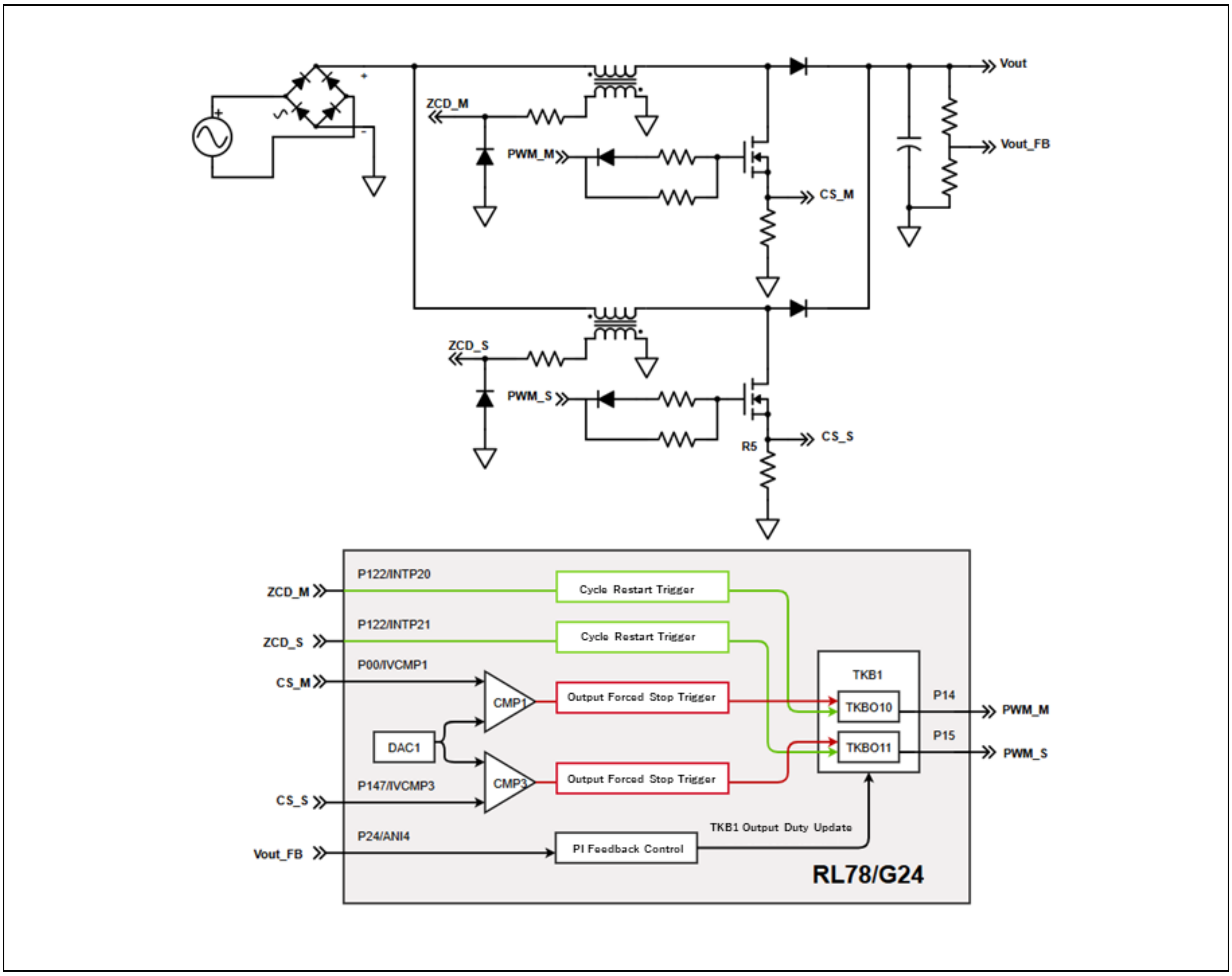


Figure 2.8 PFC Circuit

Figure 2.9 shows the waveform during PFC control. When PWM control is ON, the current is expressed as: $I_{ON}=(V_{IN}/L)\times t_{ON}$. By keeping the output time t_{ON} constant, I_{ON} becomes proportional to V_{IN}. Therefore, the peak current I_{PEAK} is in phase with the V_{IN} waveform and takes a sinusoidal shape. Since the current waveform is triangular, the average current is given by: $I_{AVERAGE}=I_{PEAK}/2$. This average current is also proportional to V_{IN}. Consequently, the average current waveform is in phase with the input voltage waveform and sinusoidal, thereby achieving a waveform with a power factor close to unity.

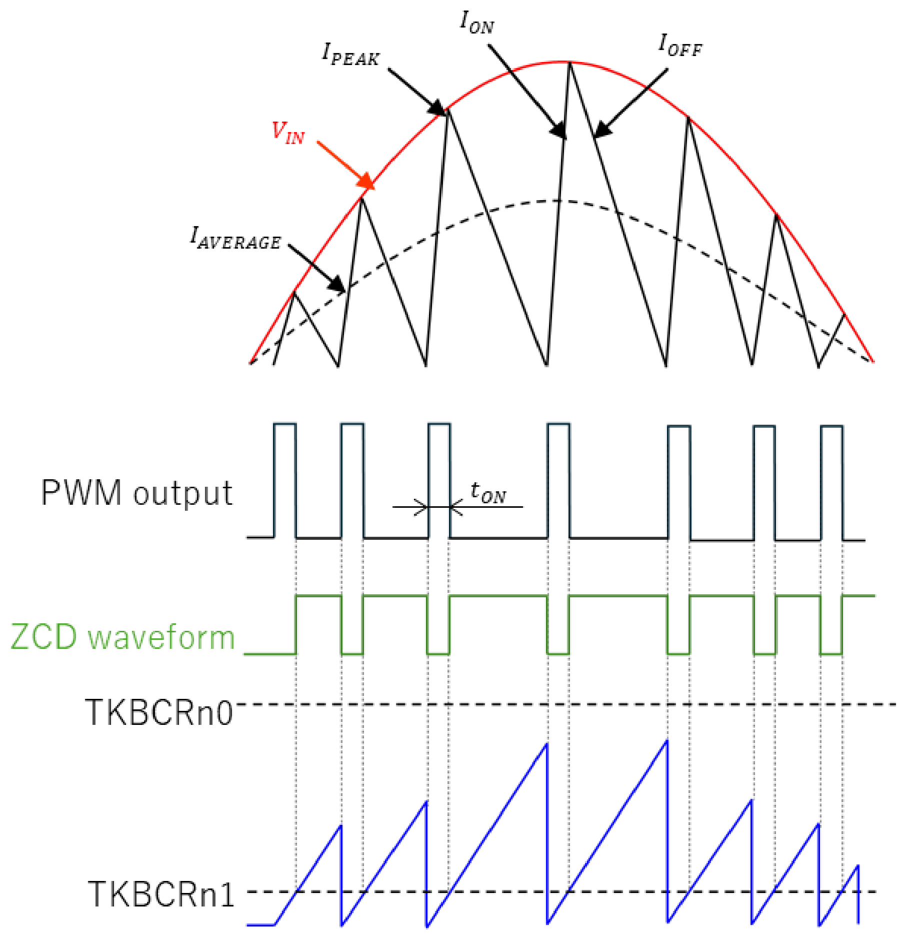


Figure 2.9 PFC Output Waveform

The blue line indicates the counter register value of the 16-bit Timer KB in the RL78/G24.
PWM output level control is performed by comparing the counter register value with each compare register, TKBCRn0 and TKBCRn1.
The counter register counts up from 0 to 65,535. The interval up to TKBCRn0 represents the ON width of the PWM output, while the interval up to TKBCRn1 represents the PWM output period. However, in normal operation under critical conduction mode, the PWM output is restarted by ZCD detection before this period expires. Therefore, the period (frequency) set in TKBCRn1 corresponds to the minimum frequency of the PFC. In normal operation, PWM output is generated at a frequency higher than this minimum.

(1) Inductor Selection

The selection of the boost inductor must be considered based on the maximum input peak current requirement. The inductor value can be determined using the following equation.

$$L = \frac{\eta \times V_{IN\_MIN}{}^{2}\left(V_{OUT} - \sqrt{2}V_{IN\_MIN}\right)}{f_{MIN} \times V_{OUT} \times P_{OUT}}$$

η : Efficiency
V_{IN_MIN} : Minimum applicable V_{in}
V_{OUT} : Output voltage
f_{MIN} : Minimum frequency
P_{OUT} : Maximum output power

The peak current of the inductor, I_{PEAK}, can be expressed by the following equation. To prevent the choke from saturating, it is necessary to select an appropriate core material.

$$I_{PEAK} = \frac{\sqrt{2}\, P_{OUT}}{V_{IN\_MIN} \times \eta}$$

For circuit control, a fixed ON time (t_{on}) and zero-current detection (ZCD) are required. Therefore, the auxiliary winding of the choke is used to detect when the inductor current reaches zero.
The winding ratio can be determined using the following equation.

$$\frac{N_P}{N_S} = \frac{V_{OUT} - \sqrt{2}\, V_{IN\_MAX}}{V_{ZCD}}$$

2.3.4.2 Output Overcurrent Detection Circuit (PFC_CS_M/S)

To prevent device failure due to abnormal inrush current or overload conditions, a shunt resistor is connected in series with the MOSFET source to enable current sensing. This signal is fed into the comparator of the RL78/G24, and when it exceeds the threshold value set by the internal DAC (configured via software), the forced output stop function of timer KBn is triggered. In this way, overcurrent detection and PWM shutdown are achieved.

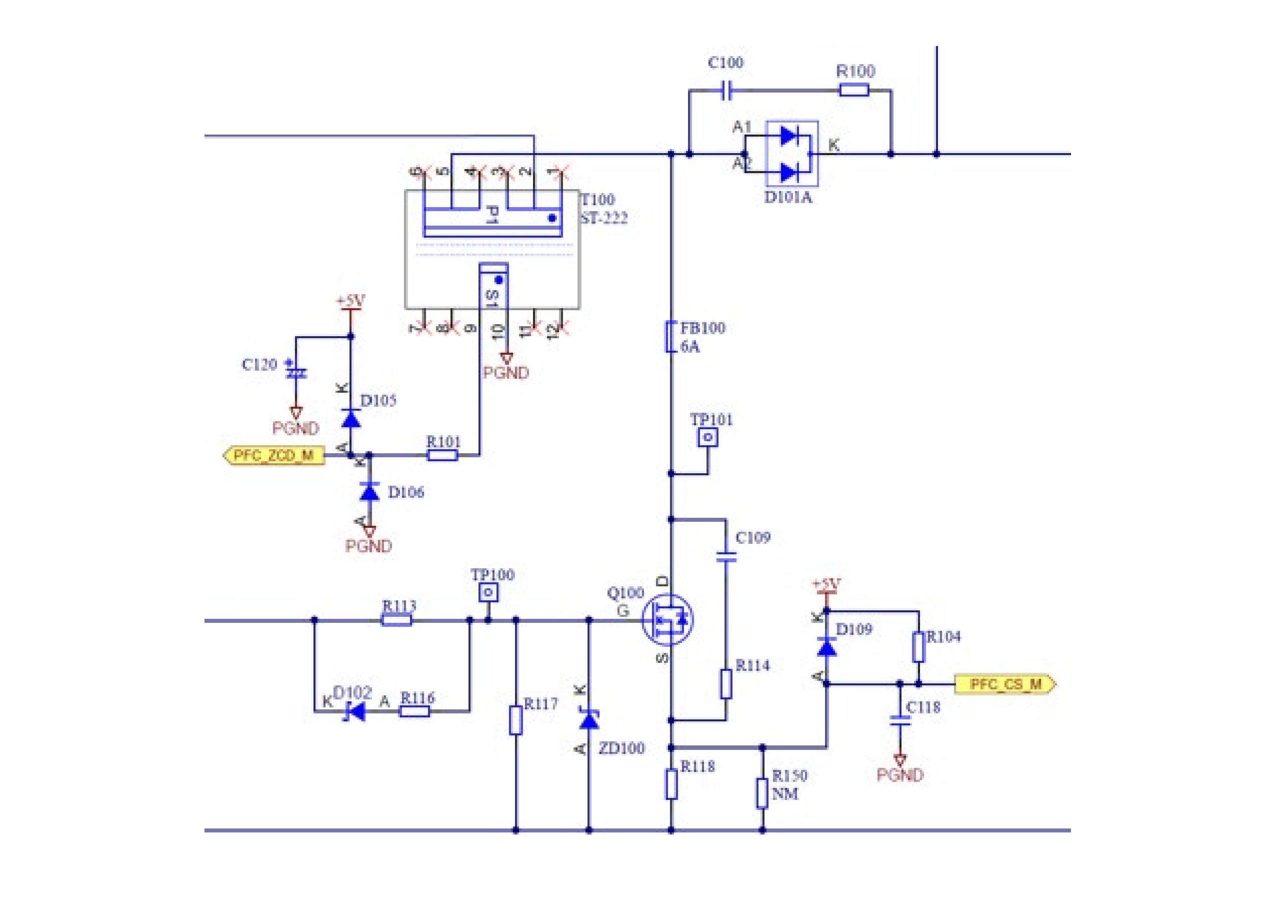


Figure 2.10 PFC Output Overcurrent Detection Circuit

The current information **PFC_CS** is obtained using the following equation:

$$\text{PFC\_CS} = I_{PEAK} \times R118$$

2.3.4.3 Output Voltage Detection Circuit (PFC_V_FB)

By dividing the PFC output voltage and connecting it to the analog input pin of the RL78/G24, the PFC output voltage can be monitored. To enhance the stability of the output voltage, both signal accuracy and noise immunity are required; therefore, this signal is connected to ground using short wiring.

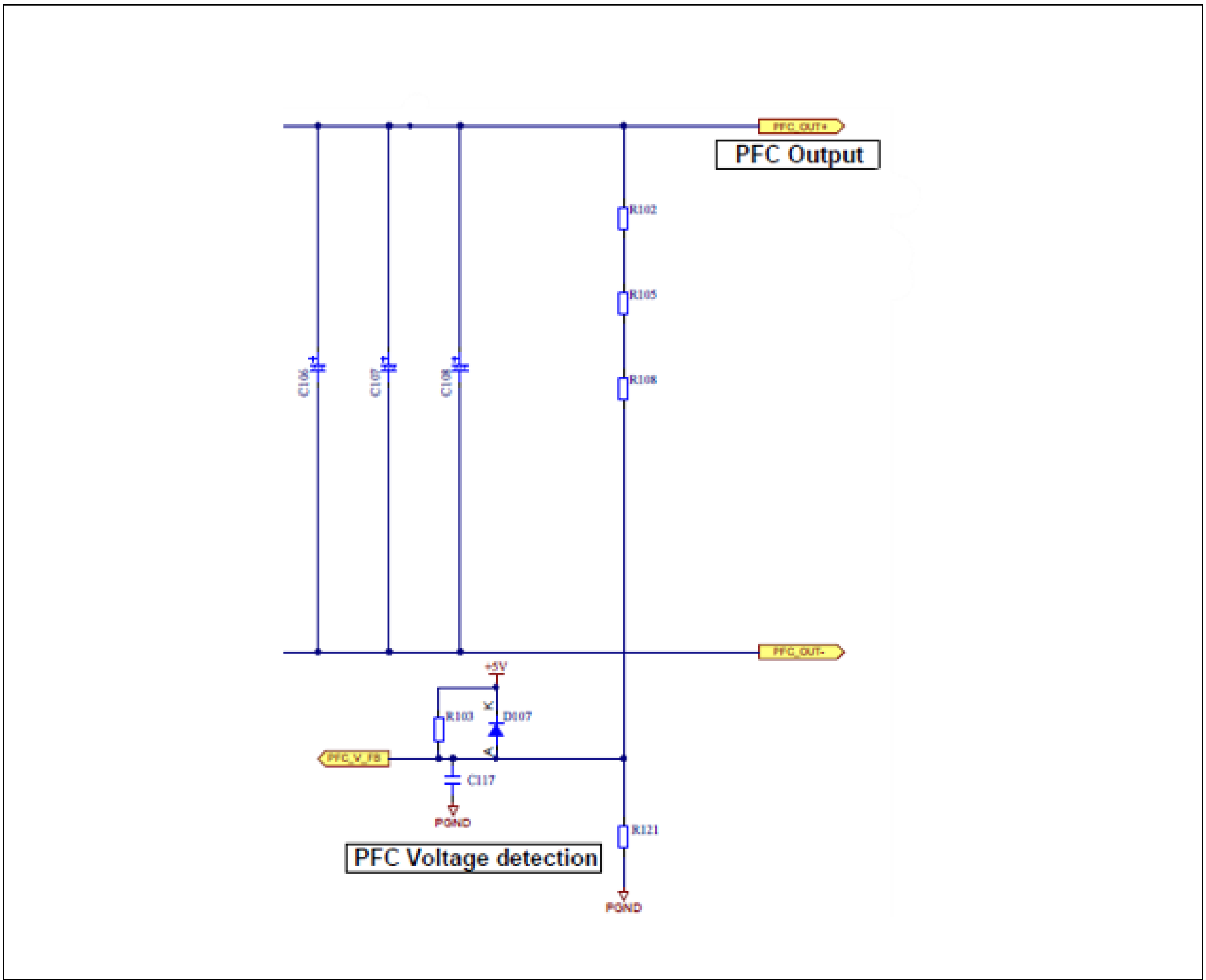


Figure 2.11 PFC Output Voltage Detection Circuit

The PFC output voltage is obtained using the following equation:

$$\mathrm{PFC\_OUT} = \frac{\mathrm{PFC\_V\_FB} \times (\mathrm{R102}+\mathrm{R105}+\mathrm{R108}+\mathrm{R121})}{\mathrm{R121}}$$

2.3.5 LLC Circuit

2.3.5.1 Circuit Analysis

Figure 2.12 shows the basic LLC model used for deriving the equations that represent the system behavior. The description of each stage of the circuit is provided below.

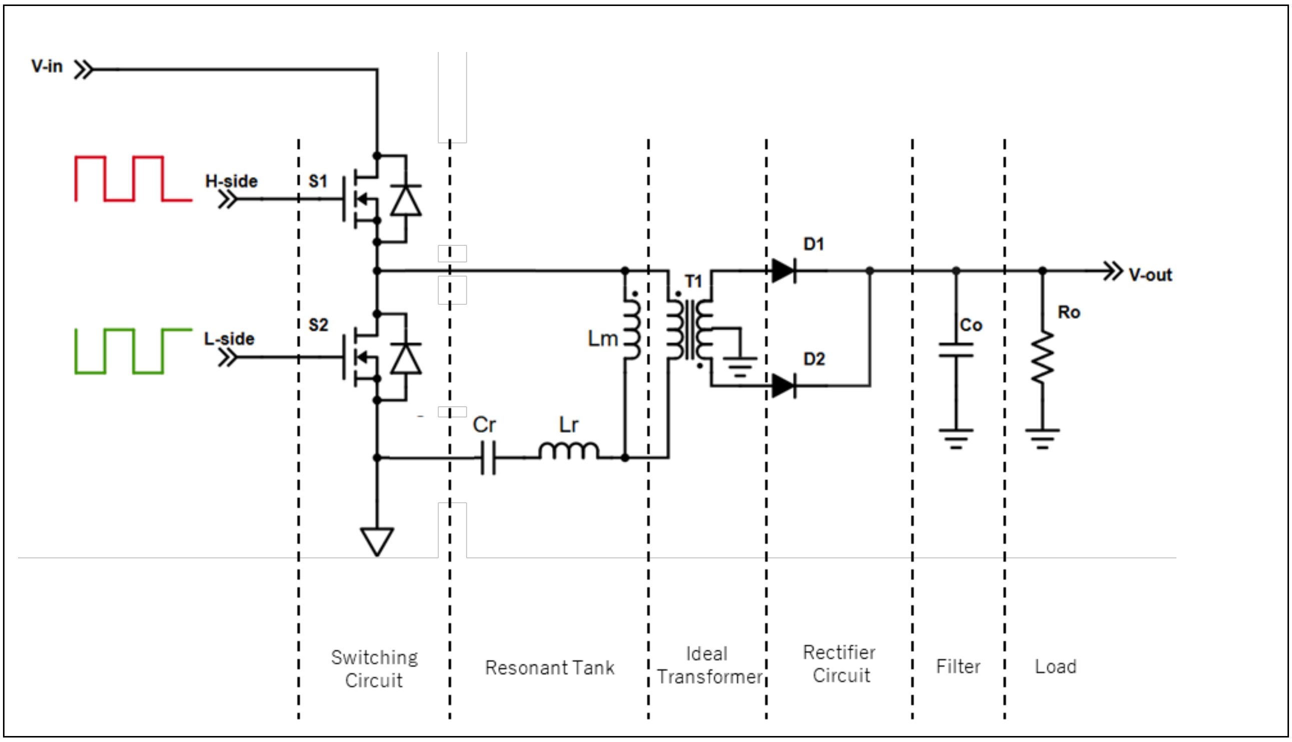


Figure 2.12 LLC Circuit

- Switching Circuit

The switching circuit is configured as a half-bridge using a high-side MOSFET and a low-side MOSFET. The body diode and parasitic output capacitance of the MOSFETs affect the circuit operation and performance.

- Resonant Tank

The circuit consists of the resonant capacitor Cr, resonant inductance Lr, and magnetizing inductance Lm. Two resonant frequencies are generated within the circuit. Details are explained later in the equivalent circuit section.

- Ideal Transformer

For the purpose of simplifying the circuit, the transformer is replaced with an ideal model. Strictly speaking, the leakage inductances of the primary and secondary sides should also be considered; however, at the stage of determining the overall system behavior, analysis using the ideal model is sufficient.

- Rectifier Circuit

Since the details of the rectifier circuit are not critical for the circuit analysis, the current waveform calculation is based on full-wave rectification.

- Filter

The filter is represented by the capacitor Co.

- Load

The output power is represented by the resistor Ro.

(1) Fourier series expansion of the input voltage

Because the circuit operation is highly complex, the design employs an equivalent circuit model. In normal-mode operation, the MOSFET switching frequency is designed to match the tank resonant frequency, and the tank components are selected accordingly. When a switching waveform compatible with the tank circuit is applied, only the sinusoidal component is transferred to the output.

The two MOSFETs operate complementarily with a fixed dead time and a 50% duty cycle. Consequently, the output of the switching stage is a rectangular waveform. To describe this rectangular waveform analytically, we expand it using a Fourier series.

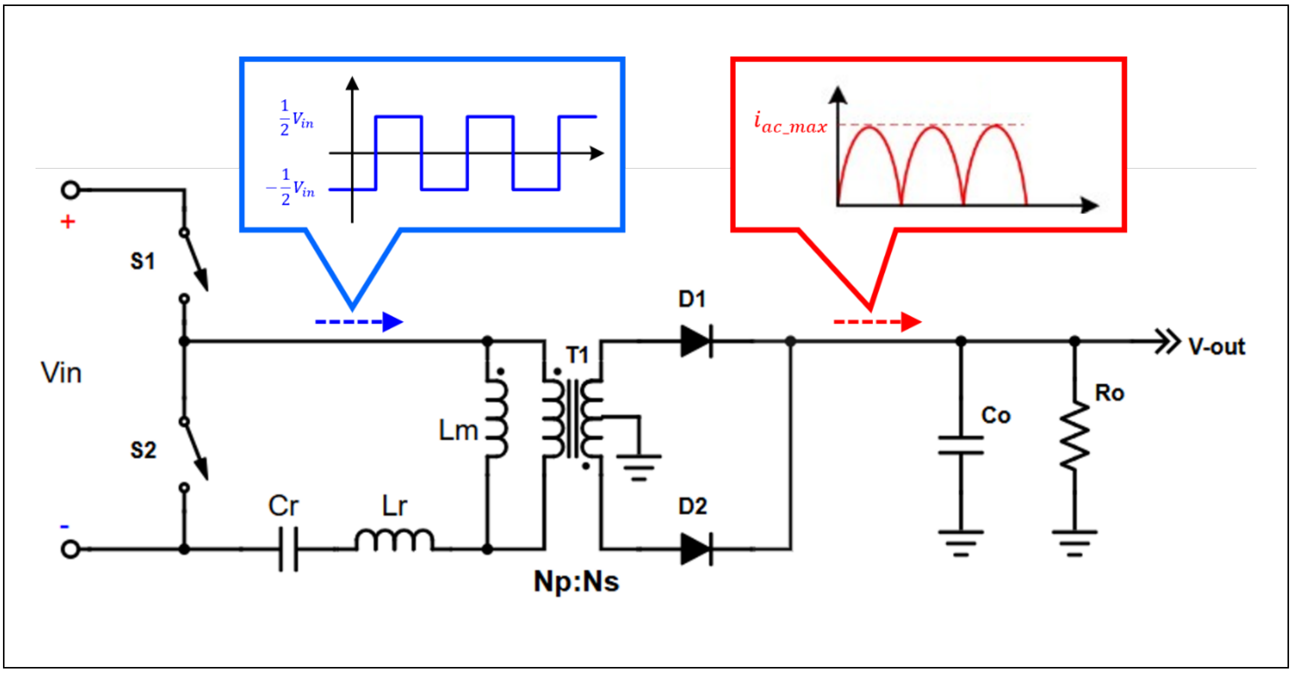


Figure 2.13 Input Voltage and Load Current of the LLC Circuit

Figure 2.14 shows the rectangular input waveform to be expanded using a Fourier series. For analytical simplification, the amplitude is set to 1.

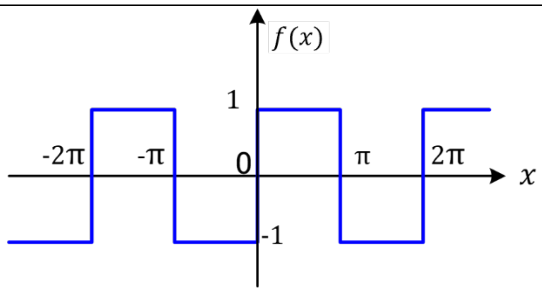


Figure 2.14 Input rectangular waveform simplification

The rectangular waveform function f(x) over one period --π≦x≦π can be written as follows:

$$f(x) = \begin{cases} -1 \ (-\pi \leq x \leq 0) \\ 1 \ (0 \leq x \leq \pi) \end{cases}$$

Since the function f(x) is an odd function, its Fourier series are respectively as follows.

$$a_0 = 0$$

$$a_n = 0$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\sin nx\,dx$$

$$= \frac{2}{\pi}\int_{0}^{\pi} \sin nx\,dx$$

$$= \begin{cases} 0 \ (\text{n is even}) \\ \dfrac{4}{\pi n} \ (\text{n is odd}) \end{cases}$$

The function f(x) is expanded into a Fourier series, and the following result is obtained.

$$\mathrm{f(x)} = a_0 + \sum_{n=1}^{\infty}(a_n \cos nx + b_n \sin nx)$$

$$= \sum_{n=1}^{\infty}(b_n \sin nx)$$

$$= \frac{4}{\pi}\left(\sin x + \frac{1}{3}\sin 3x + \frac{1}{5}\sin 5x + \ldots\right)$$

$$= \frac{4}{\pi}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin(2n+1)x$$

(2) Calculation of Rectified Current

The current waveform after the rectifier circuit on the secondary side, as well as the waveform converted to DC, are shown in Figure 2.15. Derive the relationship between the maximum value of the AC current before DC conversion, i_{ac_max}, and the load current after conversion, I_o.

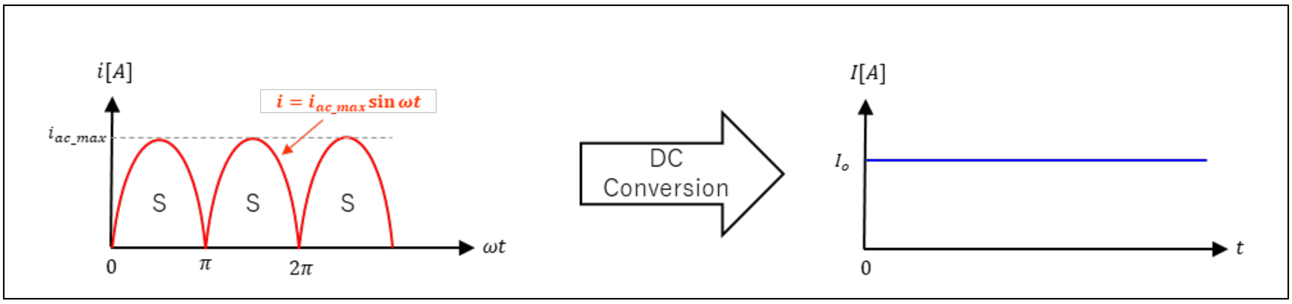


Figure 2.15 Current waveform before and after DC conversion

First, the equation for the AC current before smoothing is defined as follows.

$$i = f(t) = i_{ac\_max} \sin \omega t$$

When the total current of the AC half-wave is denoted by S, S is obtained by the following equation.

$$S = \int_0^{\pi} f(t)dt = 2i_{ac\_max}$$

The load current I_o can be calculated by dividing by the period π.

$$I_o = \frac{S}{\pi} = \frac{2}{\pi} \cdot i_{ac\_max}$$

By rearranging the equation, the relationship between i_{ac_max} and I_o is obtained.

$$i_{ac\_max} = \frac{\pi}{2} I_o$$

(3) Analysis of the Equivalent Circuit

In the equivalent circuit, the transformer on the primary side of the LLC is represented by the magnetizing inductance L_m and the leakage inductance L_r. On the other hand, the leakage inductance on the secondary side is not significant and is therefore omitted. By replacing the output circuit on the secondary side with an equivalent resistance R_{ac}, the circuit shown in Figure 2.12 can be expressed by the equivalent circuit below.

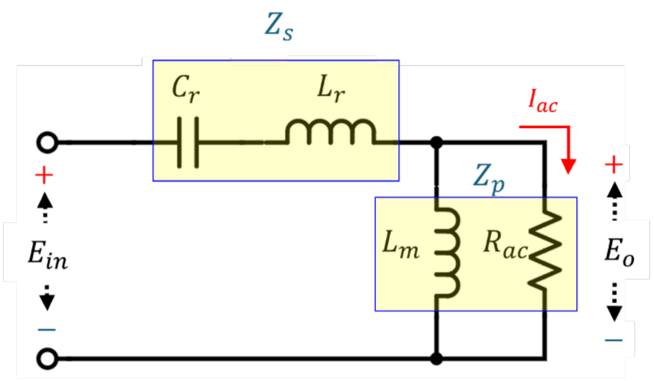


Figure 2.16 LLC Equivalent Circuit

Each parameter of the equivalent circuit can be obtained by the following equations.

$$\mathrm{E_{in}} = \frac{1}{2}\mathrm{V_{in}} \times \frac{4}{\pi} = \frac{2}{\pi}\mathrm{V_{in}}$$

$$\mathrm{E_o} = \mathrm{nV_o} \times \frac{4}{\pi} = \frac{4}{\pi}\mathrm{nV_o}$$

$$I_{ac} = \frac{\pi}{2} I_o \times \frac{1}{\mathrm{n}} = \frac{\pi}{2\mathrm{n}} I_o$$

$$\mathrm{G_{ac}} = \frac{\mathrm{E_o}}{\mathrm{E_{in}}} = \frac{2\mathrm{nV_o}}{\mathrm{V_{in}}}$$

$$R_{ac} = \frac{\mathrm{E_o}}{I_{ac}} = \frac{\frac{4}{\pi}\mathrm{nV_o}}{\frac{\pi}{2\mathrm{n}} I_o} = \frac{8}{\pi^2}\mathrm{n}^2 R_o$$

$$\text{Note: } \mathrm{n} = \frac{\mathrm{N_P}}{\mathrm{N_S}}$$

By aggregating the series impedance Z_s (comprising C_r and L_r) and the parallel impedance Zp (comprising Lm, the transformer, and the output load), the transfer function of the circuit can be easily calculated. By applying the Laplace transform to the impedances Z_s and Z_p, the voltage transfer ratio is obtained.

$$Z_s = j\left(\omega L_r - \frac{1}{\omega C_r}\right)$$

$$\mathcal{L}(Z_s) = L_r s + \frac{1}{C_r s}$$

$$Z_p = \frac{1}{\frac{1}{R_{ac}} + \frac{1}{j\omega L_m}}$$

$$\mathcal{L}(Z_p) = \frac{R_{ac} L_m s}{R_{ac} + L_m s}$$

The gain G can be obtained by the following equation.

$$\mathcal{L}(G) = \frac{E_o}{E_{in}} = \frac{\mathcal{L}(Z_p)}{\mathcal{L}(Z_s) + \mathcal{L}(Z_p)} = \frac{\frac{R_{ac} L_m s}{R_{ac} + L_m s}}{L_r s + \frac{1}{C_r s} + \frac{R_{ac} L_m s}{R_{ac} + L_m s}}$$

$$= \frac{1}{1 + \frac{L_r}{L_m} + \frac{L_r}{R_{ac}} \cdot s + \frac{1}{R_{ac} C_r} \cdot \frac{1}{s} + \frac{1}{L_m C_r} \cdot \frac{1}{s^2}}$$

$$|G| = \mathcal{L}^{-1}(\mathcal{L}(G)) = \frac{1}{\sqrt{\left(1 + \frac{1}{K} - \frac{1}{K\omega_n^{\,2}}\right)^2 + Q^2\left(\omega_n - \frac{1}{\omega_n}\right)^2}}$$

Each parameter at this point can be expressed as follows.

$$K = \frac{L_m}{L_r}$$

$$\omega_n = \frac{\omega}{\omega_r}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}$$

$$Q = \frac{Z_0}{R_{ac}} = \frac{\sqrt{L_r / C_r}}{R_{ac}} = \frac{\omega_r L_r}{R_{ac}} = \frac{1}{R_{ac}\omega_r C_r}$$

From the above equation, the transfer ratio G can be expressed as a function of the switching frequency and the tank parameters K and Q.

Although the gain function of the circuit cannot be derived without calculating all parameters, it is possible to plot the gain curve by individually assigning values to the parameters K and Q. Figure 2.17 shows an example of gain curves obtained by fixing the parameter K and varying the quality factor Q across multiple patterns.

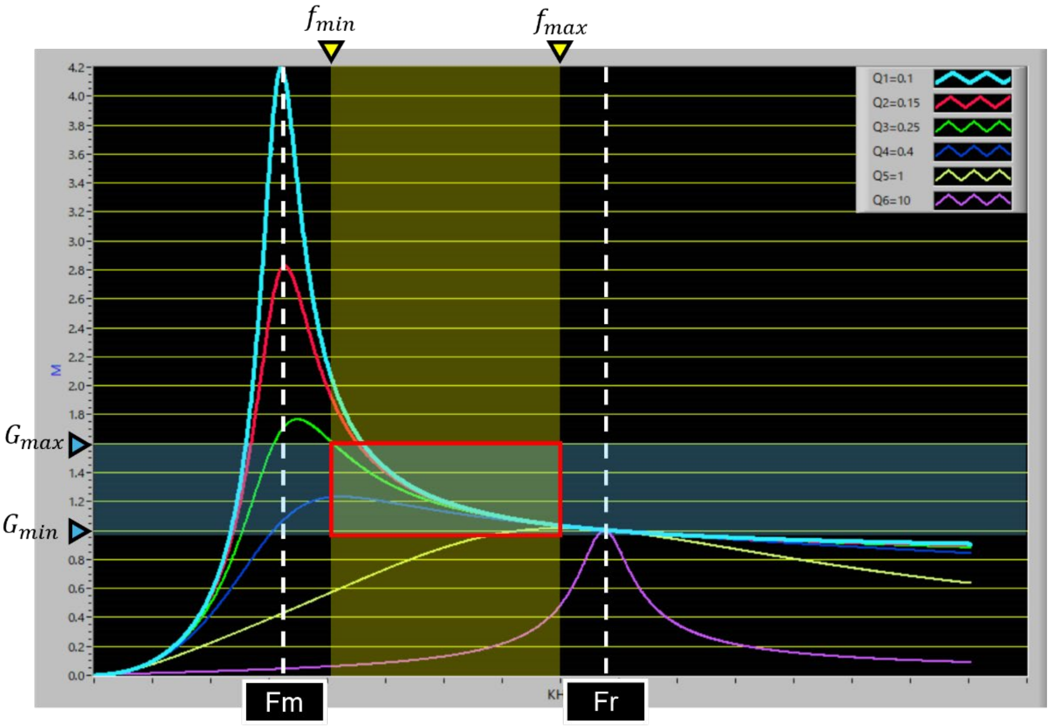


Figure 2.17 Gain Curve (Fixed K)

This figure shows the resonant frequencies F_r and F_m. The frequency F_m affects the higher peak on the left side. The operating range of the switching frequency is set between F_m and F_r. In the figure above, as an example, the operating range of the switching frequency is indicated from f_{min} to f_{max}.

The design of the quality factor Q must take into account the condition of minimum input voltage and heavy load. As the value of Q increases, there is a risk of insufficient gain at low input voltage and entering the ZCS (Zero Current Switching) region. Within the typical range of the parameter K (approximately 3 to 8), it is recommended to set the maximum quality factor that satisfies both ZVS (Zero Voltage Switching) operation and the required gain.

The required gain range (G_{min}, G_{max}) can be obtained using the input voltage range (V_{in-min}, V_{in-max}), the output voltage range (V_{o-min}, V_{o-max}), and the transformer turns ratio n, as given by the following equations.

$$G_{min} = \frac{2n \times V_{o-min}}{V_{in-max}}$$

$$G_{max} = \frac{2n \times V_{o-max}}{V_{in-min}}$$

In Figure 2.17, it is recommended to design within the range of the quality factor Q for which the gain curve lies inside the region bounded by the required gain range (G_{min}, G_{max}) and the switching frequency range (f_{min}, f_{max}).

Next, Figure 2.18 shows an example of gain curves plotted for several values of the value of K, while keeping the quality factor Q fixed. All of the curves intersect at a single point corresponding to F_r (i.e., the resonant frequency), where the voltage conversion ratio becomes 1.

When a curve with a steep gain peak is selected, the gain varies significantly with frequency deviations, making the system difficult to control; therefore, such designs should be avoided. Conversely, when a curve with a gentle gain peak is selected, the gain becomes less sensitive to frequency deviations, which may result in insufficient output. For this reason, the value of K must be chosen so that the gain remains appropriate over the intended switching frequency range.

The operating range of the switching frequency is examined below. The switching frequency reaches its maximum under the condition of the highest input voltage combined with a light load. Conversely, it becomes minimum when the lowest input voltage is combined with the maximum load. In general, the value of K is designed to fall within the range of approximately 3 to 8.

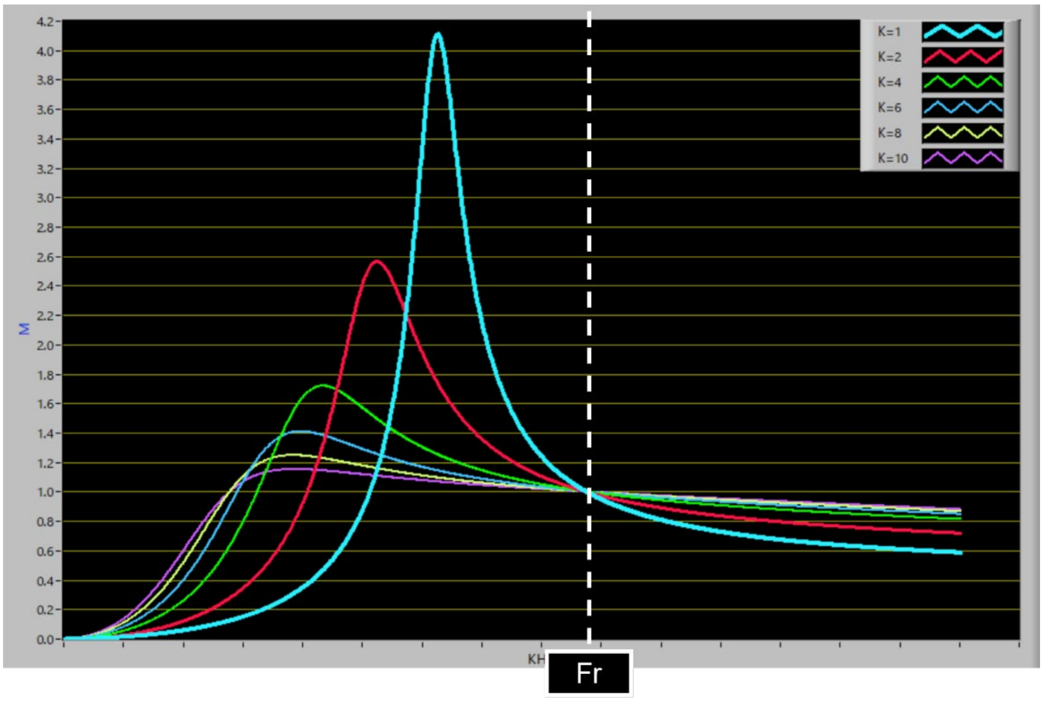


Figure 2.18 Gain Curve (Fixed Q)

2.3.5.2 Output Voltage Sensing Circuit (LLC_x_V_FB)

The secondary-side output voltage is configured using an optocoupler, a TL431, and resistors, as shown in Figure 2.19. The output voltage is determined by the resistance values of R1 and R2. The microcontroller receives the feedback signal from the primary side of the optocoupler and performs MOSFET switching control according to the load conditions.

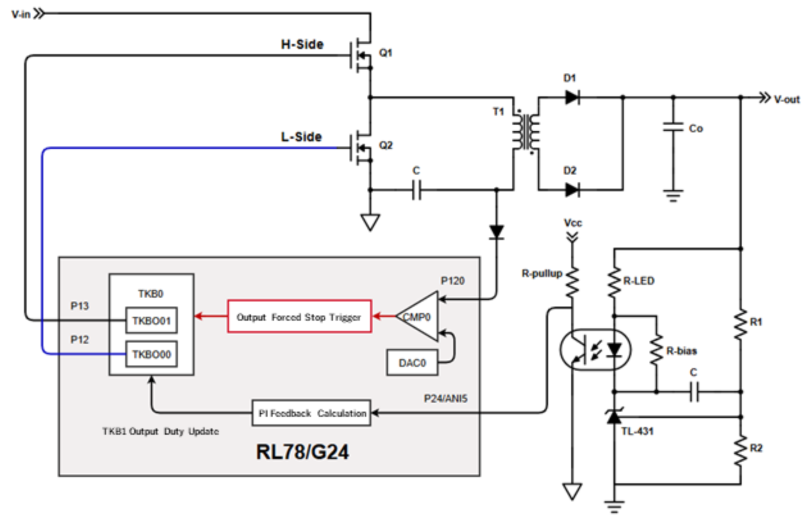


Figure 2.19 LLC1 Output Voltage Sensing Circuit

The output is obtained using the following equation.

$$V_{out}=\left(1+\frac{\mathrm{R1}}{\mathrm{R2}}\right)\times \mathrm{V_{REF}}$$

The TL431 requires a reference input current I_{ref} of approximately 2 μA to 4 μA (depending on the device), so an appropriate resistance value must be selected for R1. The cathode pin must also be supplied with more than 1 mA of current. Assuming a forward voltage drop VF of 1 V for the optocoupler, the minimum cathode current I_{min} flows accordingly. Once the reference voltage V_{REF} is established, stable operation can be achieved.

For the optocoupler, its CTR must be derated to account for temperature, long-term degradation (50%), and design margin (50%). Based on the calculated $R_{LED\text{-}max}$ value obtained from the equation below, a resistance value approximately four times larger can be used.

$$R_{bias}\times I_{min}\leq \mathrm{V_F}$$

$$\therefore R_{bias}\leq \frac{1\mathrm{V}}{1\mathrm{mA}}$$

$$\mathrm{R_{LED\text{-}max}}\leq \frac{\mathrm{V_{RLED}}}{\mathrm{I_{KA}}}=\frac{\mathrm{V_{out}}-\mathrm{V_F}-\mathrm{V_{KA\text{-}min}}}{\mathrm{I_F}+\mathrm{I_{bias}}}$$

2.3.5.3 Overcurrent Protection (LLC_CS)

When an overload occurs and components continue operating beyond their specifications, hazards such as overheating or ignition may arise. To quickly shut down the circuit in the event of an overload, an overcurrent protection circuit is implemented. Figure 2.20 shows the LLC overcurrent protection circuit. This circuit detects overcurrent by rectifying the AC component flowing through the transformer and converting it into a DC signal.

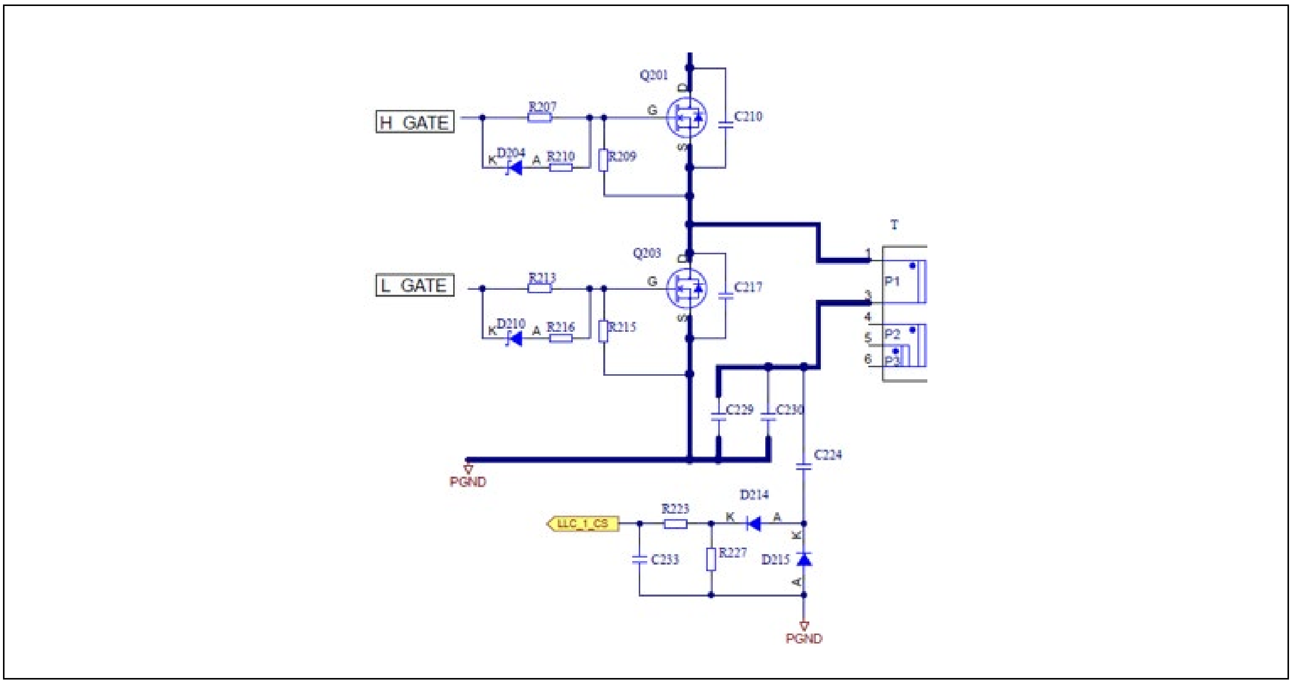


Figure 2.20 LLC Overcurrent Protection Circuit

A voltage waveform as shown in Figure 2.21 is applied to the LLC_1_CS terminal. When this waveform exceeds the threshold voltage set by software, the microcontroller stops the LLC output without software intervention as an overcurrent detection. (LLC_2_CS operates similarly.)

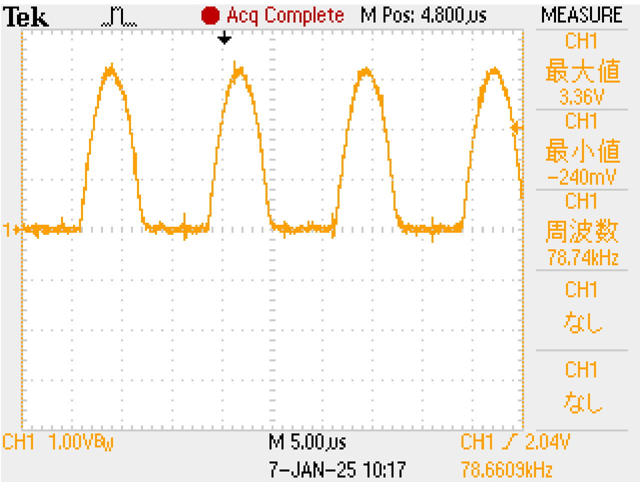


Figure 2.21 LLC_CS Voltage Waveform

The peak voltage of LLC_CS can be calculated using the following equation:

$$\mathrm{LLC\_CS}=\mathrm{R227}\times I_{ac}\times\left(\frac{C224}{C224+C229+C230}\right)$$

where I_{ac} is the current obtained from the equivalent circuit in Section 2.3.5.1(3).

2.3.6 Other I/O

2.3.6.1 Serial Communication

Serial communication with a PC or another microcontroller is possible via the CN301 connector.

By embedding UART communication as user code, communication with a PC can be performed via the debug board.

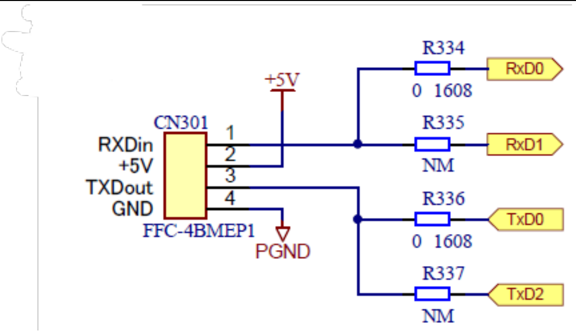


Figure 2.22 Serial Communication

2.3.6.2 Push Switches

Two push switches are implemented for user use. The sample program uses them to switch operating modes.

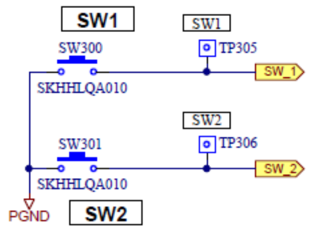


Figure 2.23 Push Switches

2.3.6.3 IR Receiver

This is a circuit for receiving infrared signals. By embedding an infrared receiver program as user code, you can receive signals from a remote control.

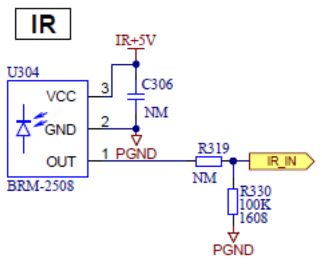


Figure 2.24 IR Receiver

3. Software Description

This section describes the software used in this document.

The software covered in this document is provided in multiple projects with different configurations. Refer to separate application notes for project-specific designs.

Interleaved CrM PFC and LLC Control with RL78/G24 (FAA Software) (R01AN8176)

Interleaved CrM PFC and LLC Control with RL78/G24 (CPU Software) (R01AN8177)

3.1 List of Used Pins

This section lists the pins used by the microcontroller.

Table 3.1 List of Used Pins

Function	Pin Name	I/O	Description
PFC	P15/TKBO11	O	PFC Slave-Side Output
	P14/TKBO10	O	PFC Master-Side Output
	P122/INTP20	I	PFC Master-Side ZCD Detection
	P121/INTP21	I	PFC Slave-Side ZCD Detection
	P24/ANI4	I	PFC Output Voltage Analog Input
	P00/IVCMP1	I	PFC Master Current Input (for OCP Detection)
	P147/IVCMP3	I	PFC Slave Current Input (for OCP Detection)
LLC1	P12/TKBO00	O	LLC1 High-Side Gate Output
	P13/TKBO01	O	LLC1 Low-Side Gate Output
	P25/ANI5	I	LLC1 Optocoupler Output Voltage Analog Input
	P120/IVCMP0	I	LLC1 Current Input (for OCP Detection)
LLC2	P16/TKBO20	O	LLC2 High-Side Gate Output
	P17/TKBO21	O	LLC2 Low-Side Gate Output
	P26/ANI6	I	LLC2 Optocoupler Output Voltage Analog Input
	P01/IVCMP2	I	LLC2 Current Input (for OCP Detection)
	P30	O	LLC2 MOSFET Output Enable ON/OFF Control
Miscellaneous	P27/ANI7	I	AC Input Voltage Analog Input
	P22/ANI2	I	AC Input Current Analog Input
	P70	O	Inrush Relay ON/OFF Control
	P62	O	Test Pin
	P71	I	SW1 Input
	P72	I	SW2 Input
	P51/TxD0	O	UART Transmit to Debug Board (PC)
	P50/RxD0	I	UART Receive from Debug Board (PC)
	P10/TxD2	O	UART Transmit to Sub-MCU *Optional
	P73/RxD1	I	UART Receive from Sub-MCU *Optional
	P31/TI03	I	IR Signal Input
	P21/AVREFM	I	A/D Reference Voltage (-)
	P20/AVREFP	I	A/D Reference Voltage (+)

3.2 Operating Modes

The software operates by transitioning through three major operating modes. The operating modes are as follows:

- Power-on Mode
  A temporary mode used to prepare for transition to Standby Mode after the microcontroller power is turned ON.
  This mode is executed only once at power-up.

- Standby Mode
  A low-power consumption mode. In this mode, only LLC1 output is active, capable of driving a light load as defined in Table 2.1.

- Normal Mode
  A mode in which PFC and LLC independently perform constant-voltage feedback control.

The operating mode transition diagram is shown in Figure 3.1.
If an abnormal condition occurs in any mode, both PFC and LLC outputs are stopped, and the system waits in a low-power consumption mode (STOP).

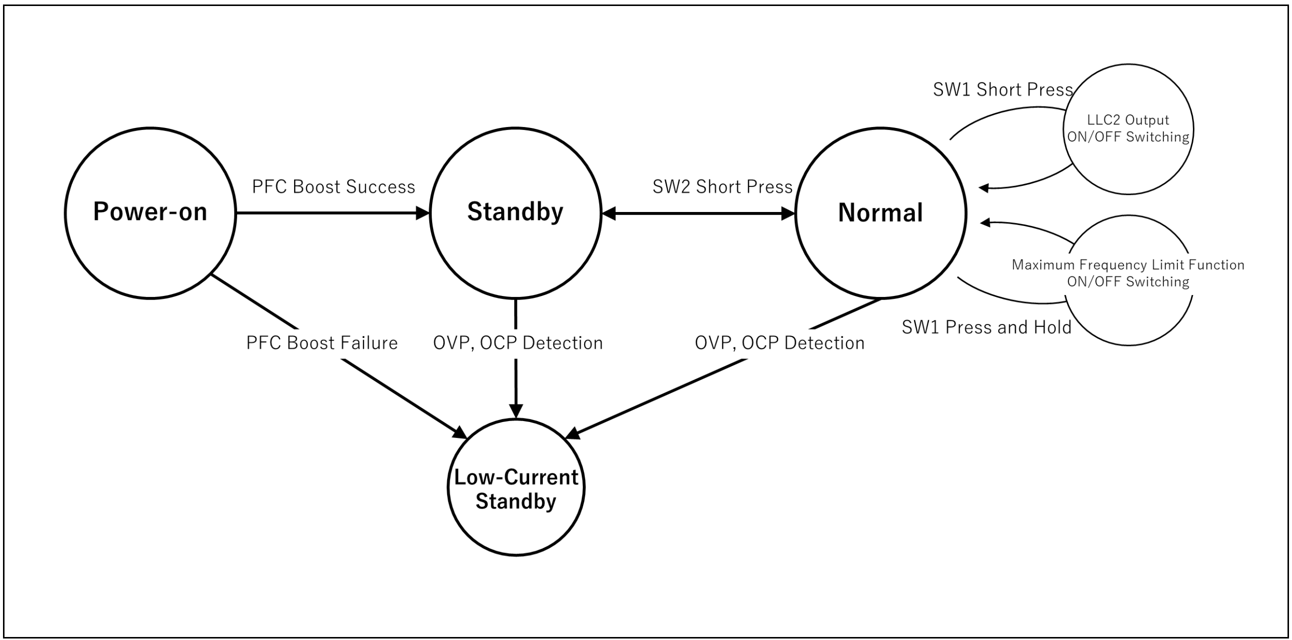


Figure 3.1 Operating Mode Transition Diagram

3.2.1 Power-on Mode

It is a temporary mode that performs the preparation for transitioning to Standby Mode after the microcontroller is powered on.

When the boosting of the PFC output voltage succeeds, it transitions to Standby Mode.

3.2.1.1 Operating Clock

The RL78/G24 microcontroller starts up using the High-Speed On-Chip Oscillator (hereafter HOCO). This software is configured to operate at HOCO 8 MHz immediately after startup. After startup, once the input-voltage stabilization wait described later is completed, the system switches to the Middle-Speed On-Chip Oscillator (hereafter MOCO) at 4 MHz and continues operation.

3.2.1.2 List of Peripheral Functions Used

This section lists the peripheral functions used in Power-on mode.

Table 3.2 Peripheral Functions Used in Power-on Mode

Peripheral Function		Purpose
16-bit Timer	KB31	PFC output
32-bit Interval Timer	ITL000&ITL001	Input-voltage stabilization timer (500 ms)
A/D Converter	-	Acquisition of A/D values for each ANI
D/A Converter	DAC1	PFC_CS overcurrent threshold
Comparator	CMP1	PFC_CS_M overcurrent detection
	CMP3	PFC_CS_S overcurrent detection
Interrupt Function	INTTMKBSTR10	PFC master-side OCP detection
	INTTMKBSTR11	PFC slave-side OCP detection

3.2.1.3 Flowchart

The flowchart for the Power-on mode is shown below.

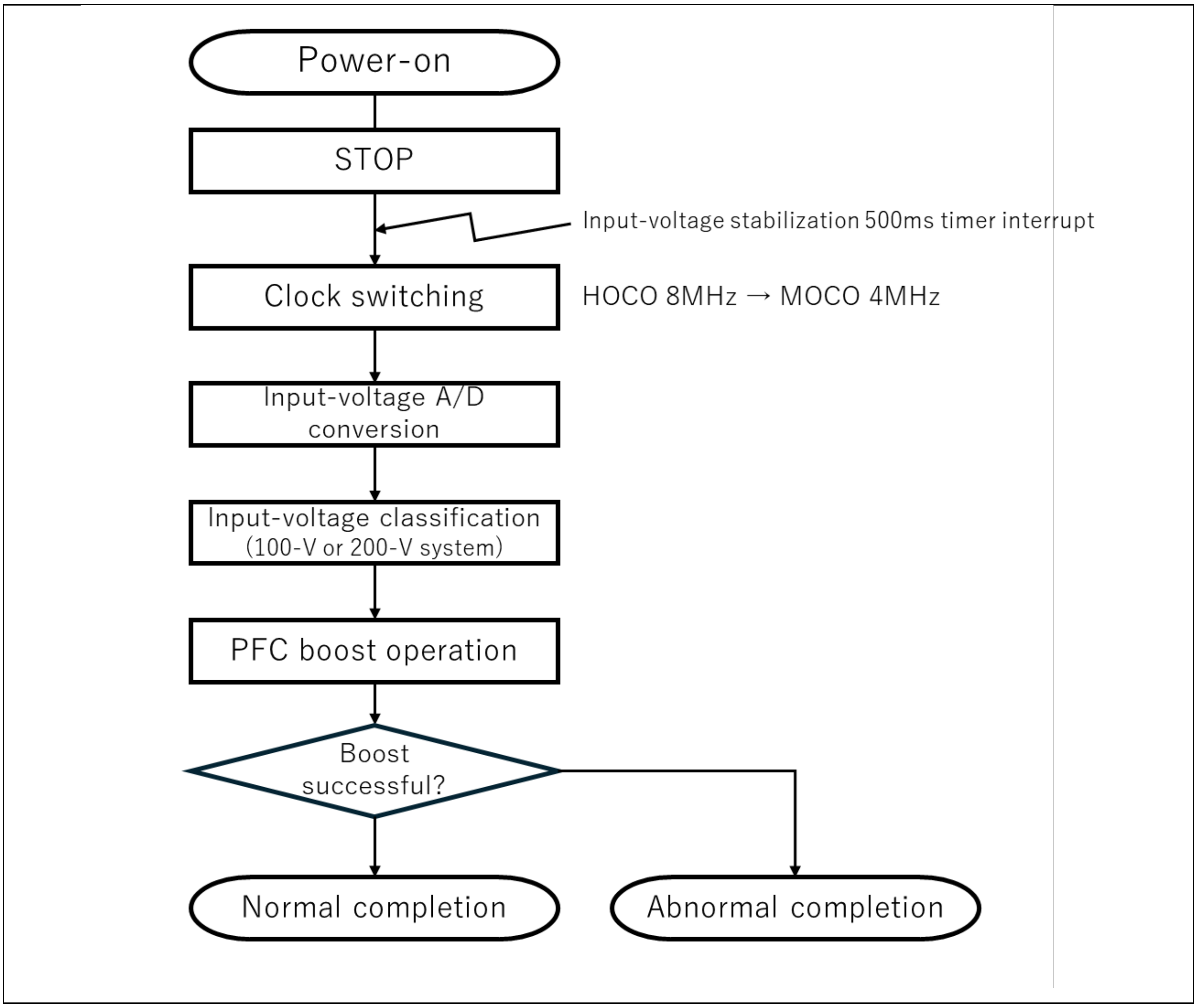


Figure 3.2 Power-on Mode Flowchart

(1) Input-Voltage Stabilization Wait

During the 500 ms stabilization period for the input voltage (AC_V pin), the microcontroller enters standby mode using the STOP instruction and remains in a low-power state. After the 500 ms period has elapsed, the system clock is switched from HOCO 8 MHz to MOCO 4 MHz.

(2) Input-Voltage Determination

The A/D value of the input voltage (AC_V terminal) is sampled four times, and if the average value exceeds the threshold (equivalent to 150 V), the input voltage is judged to be the 200-V system. If the average value is below the threshold, it is judged to be the 100-V system.

(3) PFC Boost

Using soft-start (gradually increasing the PWM on-time), the PFC output voltage is boosted up to the boost-completion voltage of 366 V. Specifically, as the soft-start operation, at the minimum frequency of 50 kHz, the on-time is linearly increased from 250 ns to 40 μs over 800 ms. During soft-start, the output is stopped at 2 ms intervals, and if the A/D value of the PFC output voltage (PFC_V_FB) has not reached the boost-completion voltage, the on-time is updated and the output is resumed.

If the A/D value of the PFC output voltage (PFC_V_FB) reaches the boost-completion voltage during the boost period, it is regarded as "boost successful," and the Power-on mode ends normally. If the boost-completion voltage is not reached even after the boost period has elapsed, it is regarded as "boost failed," and the Power-on mode ends abnormally.

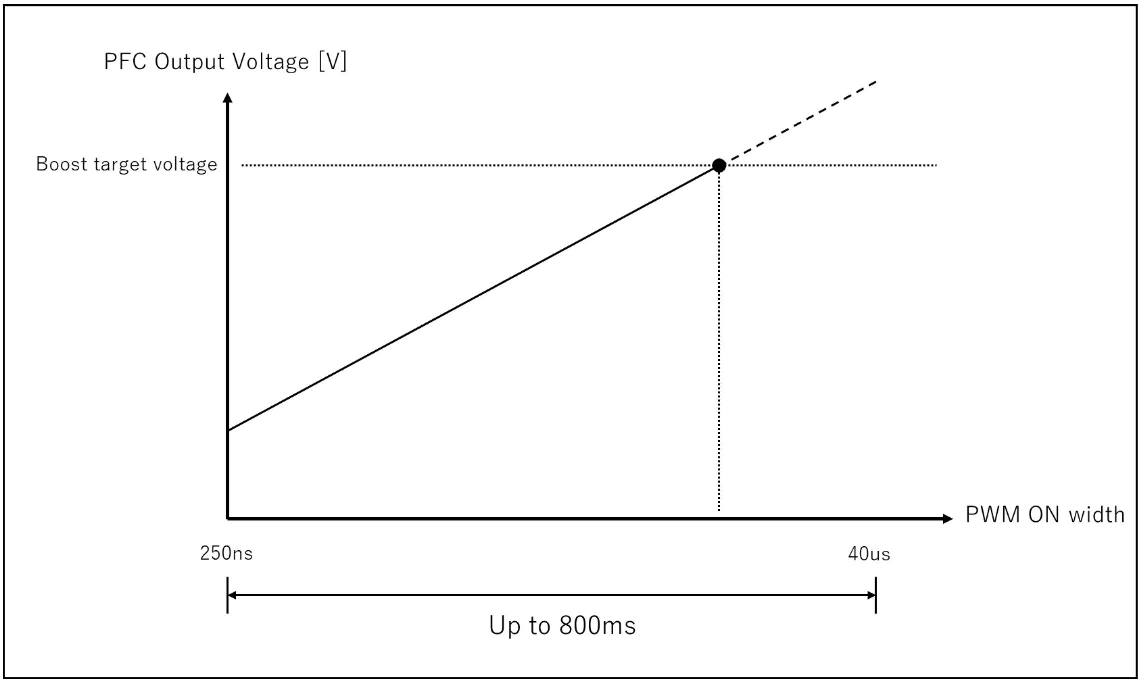


Figure 3.3 PFC Boost Converter Diagram

3.2.2 Standby Mode

This mode is designed to achieve low power consumption. In Standby mode, the PFC and LLC1 each regulate their output independently to maintain a constant voltage, while LLC2 remains inactive.

The PFC maintains a constant voltage by generating pulses when the output voltage falls below the lower limit of the target range and stops the pulses when it exceeds the upper limit.

LLC1 maintains a constant voltage by outputting pulses at fixed intervals.

A short press of SW2 transitions the system to Normal mode.

3.2.2.1 Operating Clock

Standby mode operates using the MOCO at 4MHz.

3.2.2.2 List of Peripheral Functions Used

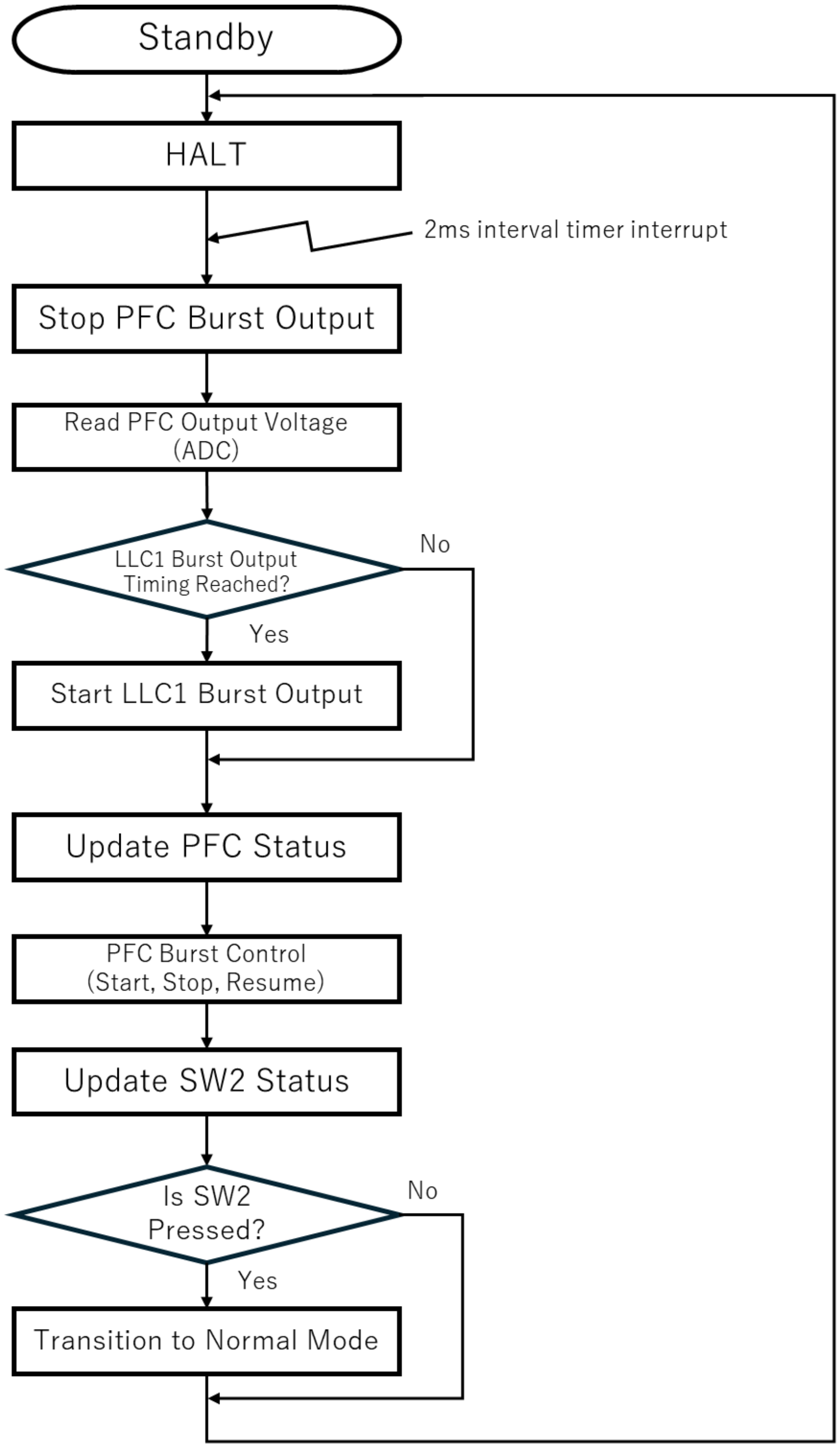
This section lists the peripheral functions used in Standby mode.

Table 3.3 Peripheral Functions Used in Standby Mode

Peripheral Function		Purpose
16-bit Timer	KB30	LLC1 output
	KB31	PFC output
32-bit Interval Timer	ITL000&ITL001	Interval timer during Standby (2 ms)
A/D Converter	-	Acquisition of A/D values from each ANI
D/A Converter	DAC0	LLC1_CS overcurrent threshold
	DAC1	PFC_CS overcurrent threshold
Comparator	CMP0	LLC1_CS overcurrent detection
	CMP1	PFC_CS_M overcurrent detection
	CMP3	PFC_CS_S overcurrent detection
Interrupt Functions	INTTMKBSTR00	LLC1 high-side OCP detection
	INTTMKBSTR01	LLC1 low-side OCP detection
	INTTMKBSTR10	PFC master-side OCP detection
	INTTMKBSTR11	PFC slave-side OCP detection

3.2.2.3 Flowchart

The flowchart for the Standby mode is shown below.



(1) PFC Burst

PFC burst is an intermittent operation in which the PFC outputs only when necessary, so that the PFC output voltage (PFC_V_FB) stays between the lower limit of 366 V and the upper limit of 386 V.

The PFC output voltage (PFC_V_FB) is obtained as an A/D value every 2 ms, and when it falls below the lower limit of 366 V, the output is started, and when it exceeds the upper limit of 386 V, the output is stopped. At this time, the PFC ON-width used for output is fixed to the ON-width at the timing when boost completion was detected in Power-on Mode. Refer to 3.2.1.3(3) for details.

During A/D acquisition, the PFC PWM is temporarily stopped to avoid the influence of switching noise.

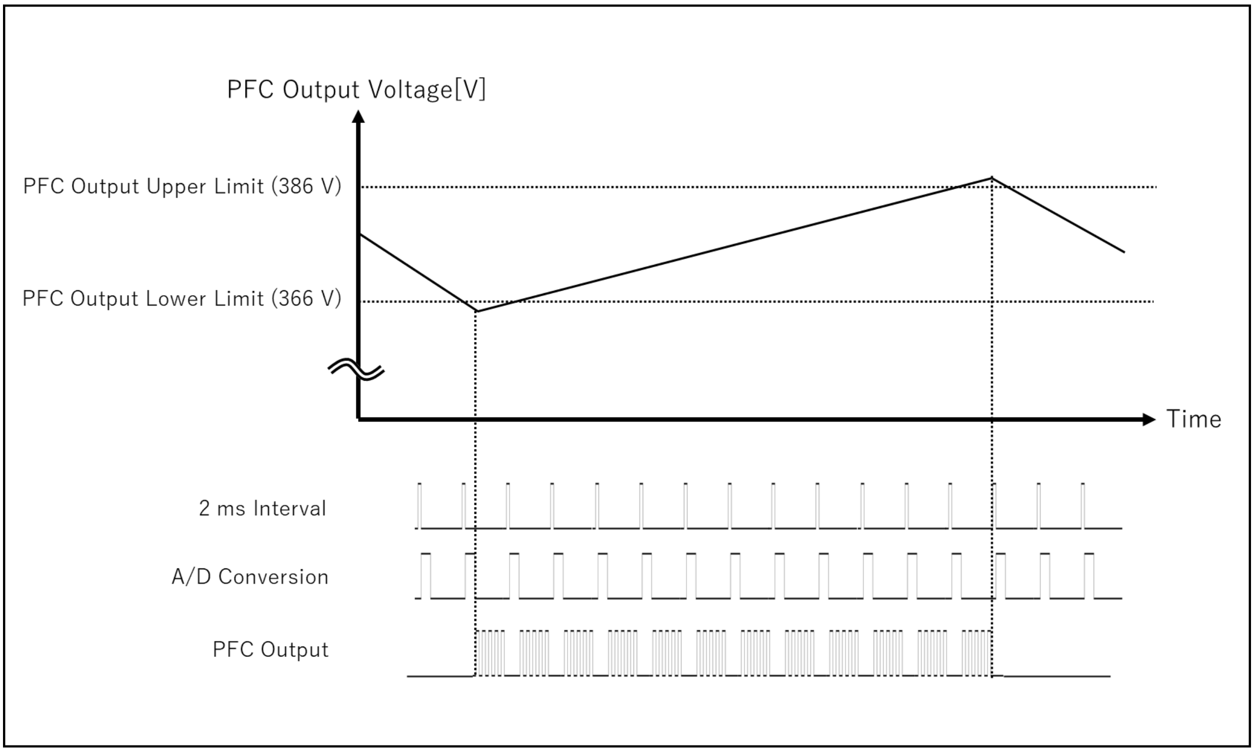


Figure 3.4 PFC Burst

(2) LLC1 Burst

LLC1 burst is an intermittent output operation that makes the LLC1 output voltage become 10 V under a specific load condition (0.15 W). In the LLC burst operation, the output voltage is not monitored, and the voltage control is performed by the output interval and the configuration of the output pulses.

In the sample program, the target voltage is achieved by outputting one 80-kHz pulse at 28-ms intervals.

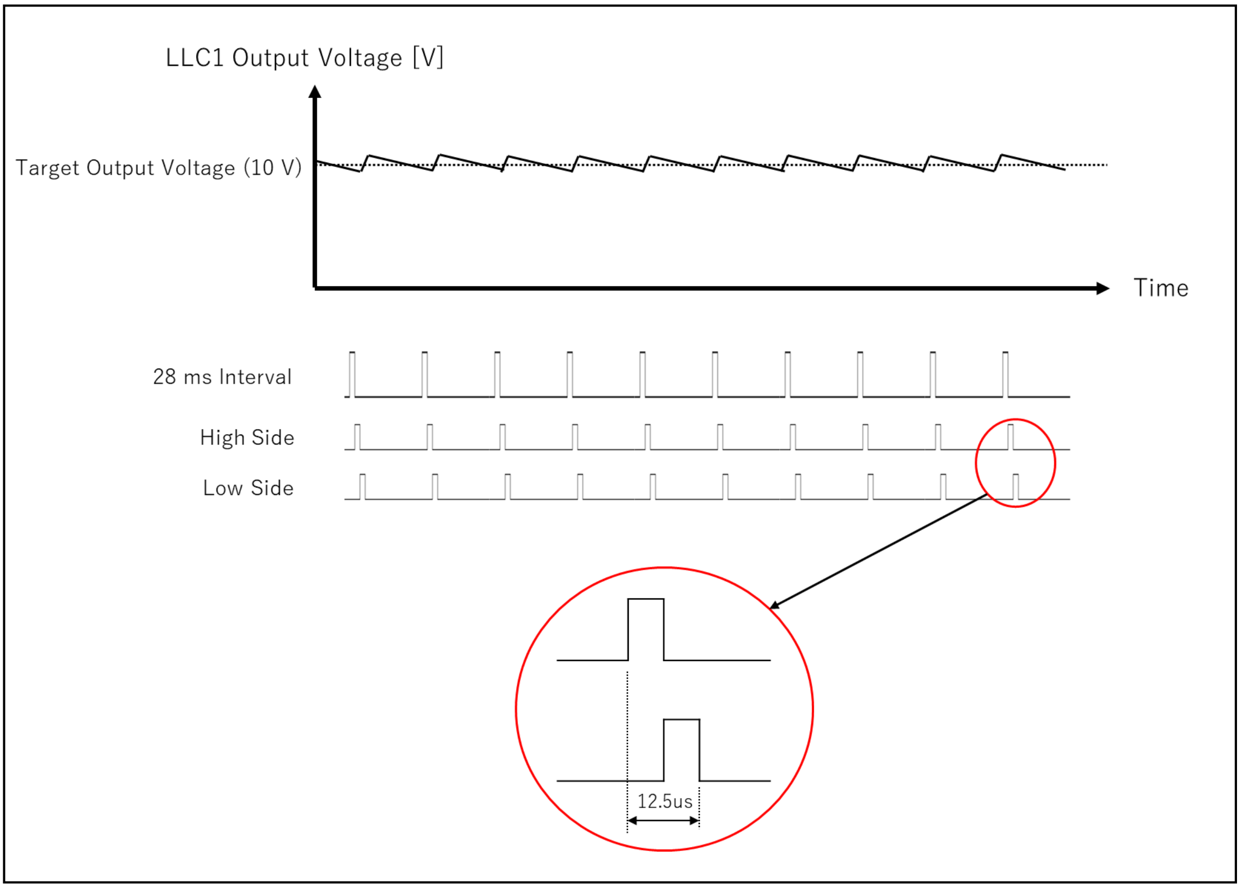


Figure 3.5 LLC1 Burst

3.2.3 Normal Mode

Normal Mode is a mode in which the PFC and LLC each perform independent constant-voltage feedback control.

3.2.3.1 Operating Clock

In Normal Mode, the PLL circuit oscillates at 96 MHz, using HOCO 8 MHz as its input. The 16-bit Timer KBn operates at 96 MHz, and the main clock f_{CLK} operates at 48 MHz, which is obtained by dividing the 96-MHz clock by 1/2.

3.2.3.2 List of Peripheral Functions Used

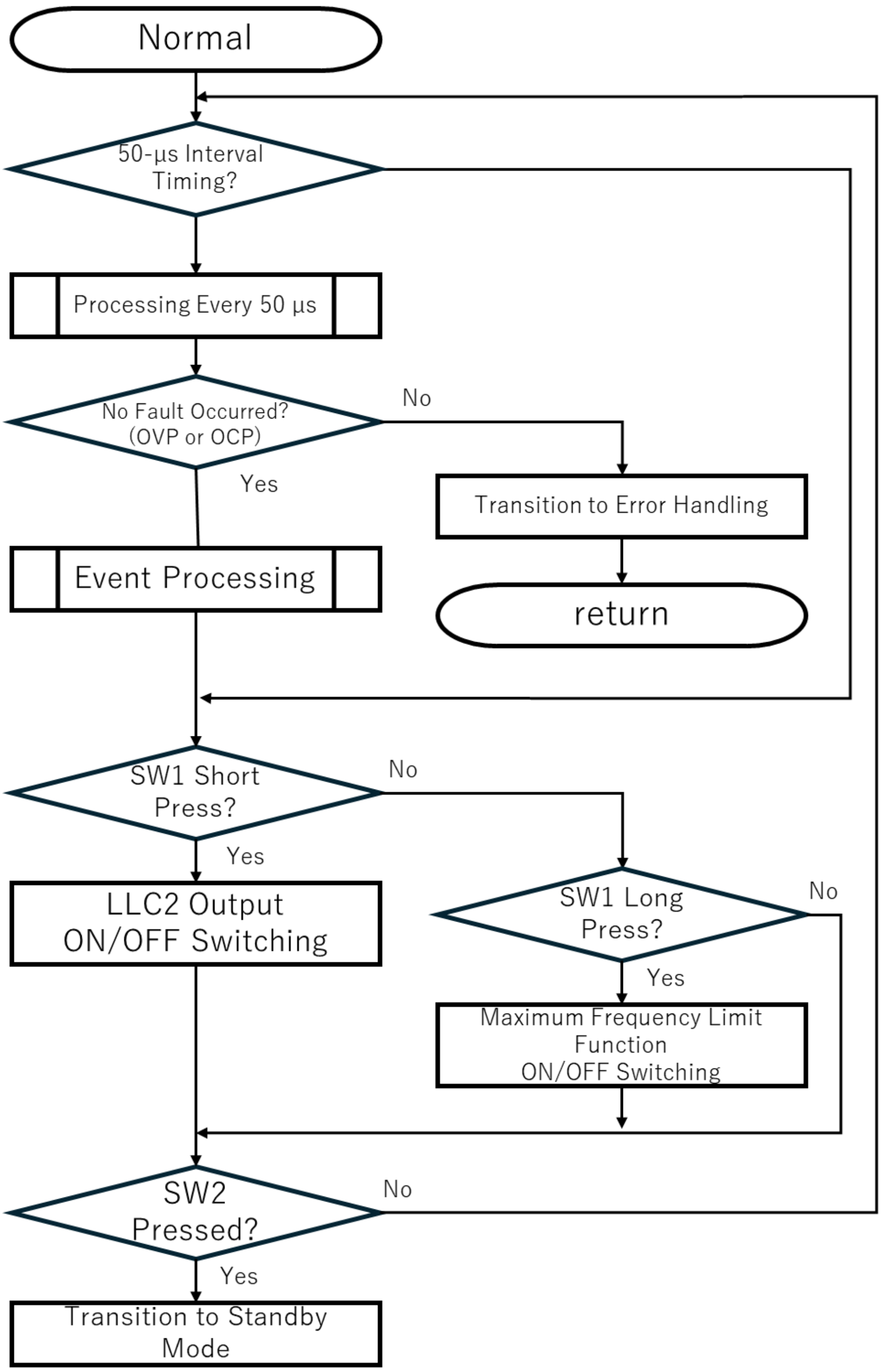
This section lists the peripheral functions used in Normal mode.

Table 3.4 List of Peripheral Functions Used in Normal Mode

Peripheral Function		Purpose
Timer Array Unit	ch0	Interval timer for Normal Mode (50 µs)
	ch1	A/D conversion start trigger (12.5 µs)
16-bit Timer	KB30	LLC1 output
	KB31	PFC output
	KB32	LLC2 output
A/D Converter	-	Acquisition of A/D values from each ANI
D/A Converter	DAC0	LLC1_CS overcurrent threshold
	DAC1	PFC_CS overcurrent threshold
	DAC2	LLC2_CS overcurrent threshold
Comparator	CMP0	LLC1_CS overcurrent detection
	CMP1	PFC_CS_M overcurrent detection
	CMP2	LLC2_CS overcurrent detection
	CMP3	PFC_CS_S overcurrent detection
Interrupt Functions	INTAD3	A/D conversion complete
	INTTMKBSTR00	LLC1 high-side OCP detection
	INTTMKBSTR01	LLC1 low-side OCP detection
	INTTMKBSTR10	PFC master-side OCP detection
	INTTMKBSTR11	PFC slave-side OCP detection
	INTTMKBSTR20	LLC2 high-side OCP detection
	INTTMKBSTR21	LLC2 low-side OCP detection
	INTTM00	Interval timer for Normal Mode (50 µs)

3.2.3.3 Flowchart

The flowchart for the Normal mode is shown below.



(1) PFC Feedback Control

This is an operating mode in which the PFC output voltage is monitored and feedback-controlled so that it becomes a constant voltage.

In the PFC feedback control, at every 400 µs feedback period, the average A/D-converted value of the PFC output voltage (PFC_V_FB) is used as the input, and the PWM output ON width is controlled so that the error from the target voltage A/D value becomes zero.

Since the A/D conversion sampling period is 12.5 µs, the average of 32 A/D conversion results becomes the input value for each feedback period.

In addition, a separate load-estimation function monitors the magnitude of the load applied to the secondary side. In the sample program, when AC 100 V is applied and the load becomes 85 W or more, the output mode switches from single to interleaved. When operating in interleaved output, if the load becomes less than 50 W, the output mode switches from interleaved back to single.

Note: When the master ON width is less than or equal to the slave ON width, the ZCD signal may fail to enter within the specified period depending on circuit configuration, peripheral components, and I/O load conditions, potentially causing Timer KB interleaving condition No. 8 (pulse skipping).

To avoid this, the program sets different ON widths for the master and slave so that the slave-side ZCD signal is detected slightly earlier.

(2) LLC1 Feedback Control

This is an operating mode in which the LLC1 output voltage is monitored and feedback-controlled so that it becomes a constant voltage.

In the LLC1 feedback control, at every 200 µs feedback period, the evaluation result based on the A/D-converted value of the LLC1 output voltage (LLC1_V_FB) is used as the input, and the output frequency is PFM-controlled so that the error from the target evaluation result becomes zero.

The LLC1 output-voltage evaluation is performed as a two-value evaluation in which the A/D value through the photocoupler is judged as either higher or lower than the target voltage. As the evaluation, a value of 1 indicates that it is higher than the target voltage, and a value of 0 indicates that it is lower.

Since the A/D conversion sampling period is 12.5 µs, the sum of 16 evaluation results becomes the input value for each feedback period. The target evaluation result is “the number of evaluations higher than the target voltage and the number of evaluations lower than the target voltage are equal,” so for 16 evaluation results, the total becomes 8.

(3) LLC2 Feedback Control

This is an operating mode in which the LLC2 output voltage is monitored and feedback-controlled so that it becomes a constant voltage.

In the LLC2 feedback control, at every 200 µs feedback period, the evaluation result based on the A/D-converted value of the LLC2 output voltage (LLC2_V_FB) is used as the input, and the output frequency is controlled (PFM) so that the error from the target evaluation result becomes zero.

The LLC2 output-voltage evaluation is performed as a two-value evaluation in which the A/D value through the optocoupler is judged as either higher or lower than the target voltage. As the evaluation, a value of 1 indicates that it is higher than the target voltage, and a value of 0 indicates that it is lower.

Since the A/D conversion sampling period is 12.5 µs, the sum of 16 evaluation results becomes the input value for each feedback period.
The target evaluation result is “the number of evaluations higher than the target voltage and the number of evaluations lower than the target voltage are equal,” so for 16 evaluation results, the total becomes 8.

At the transition to Normal mode, the LLC2 output is OFF (stopped) by default. The output ON/OFF can be switched by short-pressing SW1.

3.3 Functions Provided

This section describes the functions implemented by the software.

3.3.1 Protection Functions

This section describes the protection functions implemented by the software.

3.3.1.1 PFC Dynamic OVP

For the PFC output voltage, the software has a function that temporarily stops the output when the voltage exceeds a certain threshold, and keeps it stopped until the voltage falls below that threshold. This function is defined as the PFC Dynamic OVP (Over Voltage Protection).
In this sample program, the detection voltage threshold for Dynamic OVP is set to 400 V.

3.3.1.2 PFC OVP

For the PFC output voltage, the software has a function that forcibly stops the PFC output when the voltage exceeds a certain threshold, and this function is defined as the PFC OVP. The detection voltage threshold for OVP is set higher than the detection voltage threshold for Dynamic OVP.

In this sample program, the detection voltage threshold for OVP is set to 430 V.

3.3.1.3 LLC Dynamic OVP

During the PI control of the LLC, the software has a function that forcibly stops the LLC output when the calculated result of the output frequency, which is the control target, exceeds a certain threshold, and this function is defined as the LLC Dynamic OVP.

In this sample program, the OVP detection frequency threshold is set to 300 kHz, commonly for both LLC1 and LLC2.

3.3.2 Load Estimation Function

This section describes the load estimation function implemented in the software.

This function estimates the load connected to the output terminals of this board based on internal software parameters. Using the load estimated by this function, the software performs decisions such as switching the PFC output mode and determining the optimal frequency when the maximum-frequency-limit function is enabled.

3.3.2.1 Load Estimation Using the PFC ON Width

This function estimates the load based on the ON-width setting value of the PFC master terminal.

For three patterns—AC 100 V single-phase, AC 100 V two-phase, and AC 230 V single-phase—the PFC ON-width setting values under load conditions in 10-W increments are plotted, and a linear approximation equation representing the relationship between the load and the ON width is derived.

The accuracy of the approximation equation shown in the table below is approximately ±10 W based on actual measurements.

Table 3.5 Load-Estimation Linear Approximation Equations Using the PFC ON Width (by Condition)

Input Voltage	PFC Output Mode	Linear Approximation Equation
AC100 V	Single-phase	$watt = 0.2601 \times onWidth - 22.543$
	Two-phase	$watt = 0.4878 \times onWidth - 39.0244$
AC230V	Single-phase	$watt = 1.282 \times onWidth - 3.846$

Note that *onWidth* is the PFC ON-width setting value, and *watt* is the load power (unit: W), with watt ≥ 0.

3.3.3 Efficiency-Improvement Function

This section describes the efficiency-improvement function implemented in the software.

3.3.3.1 PFC Maximum-Frequency-Limit ON/OFF Function

The 16-bit Timer KB of the RL78/G24 includes a maximum-frequency-limit function. The purpose of this function is to suppress switching at excessively high frequencies in critical-conduction-mode PFC control. When a ZCD detection trigger occurs earlier than the configured maximum frequency, the restart can be held until the configured maximum frequency is reached. While the restart is being held, the operation enters a discontinuous-current mode; however, because this reduces MOSFET switching losses, efficiency can be improved.

This function is OFF by default (no limitation), and the ON/OFF switching can be performed by pressing and holding SW1 for 2 seconds or longer.

For two input-voltage patterns—AC 100 V and AC 230 V—the optimal (high-efficiency) maximum frequency under multiple load conditions is investigated, and a table of load versus optimal maximum frequency is created.

The load and optimal maximum-frequency settings configured in the software are shown below.

However, when applying a load of 300 W or more at AC 230 V, do not turn this function ON.

Operation may become unstable.

Table 3.6 Optimal Maximum-Frequency Settings by Load (AC 100 V)

Load Range	Maximum Frequency
0W ≦ watt ＜ 45W	120kHz
45W ≦ watt ＜ 90W	200kHz
90W ≦ watt ＜ 125W	120kHz
125W ≦ watt ＜ 275W	200kHz
275W ≦ watt ＜ 325W	120kHz
325W ≦ watt ＜ 375W	200kHz
375W ≦ watt	120kHz

Table 3.7 Optimal Maximum-Frequency Settings by Load (AC 230 V)

Load Range	Maximum Frequency
0W ≦ watt ＜ 45W	240kHz
45W ≦ watt ＜ 175W	120kHz
175W ≦ watt ＜ 275W	240kHz
275W ≦ watt ＜ 325W	260kHz
325W ≦ watt＜375	180kHz
375W≦ watt	260kHz

3.3.4 Transient-Response Improvement Functions

This section describes the transient-response improvement functions implemented in the software.

3.3.4.1 PFC Output-Mode Switching at AC Zero-Cross Timing (Optional)

The PFC output mode switches depending on the load level. In the default switching function, the output mode switches regardless of the timing within the AC input-voltage waveform. For this reason, when switching from single to interleaved mode, a soft-start process is applied, and when switching from interleaved to single mode, a soft-end process is applied. Soft-start and soft-end are used to reduce ripple during mode transitions; however, because these processes require transition time, the transient response becomes longer by the amount of time required for these processes.

This function is enabled only when switching from interleaved to single mode, and it switches the output mode at the AC input-voltage zero-cross timing without using the soft-end process. By doing so, the transient characteristics can be improved.

3.3.4.2 PFC Gain Dynamic Compensation (Optional)

This function provides the capability to dynamically change the PFC gain for the purpose of improving the response to input-voltage variations and sudden load changes. This function allows you to configure the correction factor applied to the proportional gain Kp, as well as the zero-point frequency (f_Z) derived from the pole frequency of the control circuit. By using this option, dynamic compensation functionality can be implemented.

3.3.4.3 PFC Energy Compensation Function

Due to the circuit configuration of the PFC, the output energy obtained with the same ON width differs between single output and interleaved output.

Therefore, if the output mode is switched from single to interleaved, or from interleaved to single, without adjusting the ON-width setting, the output energy changes, resulting in ripple appearing in the PFC output voltage.

To compensate for this, a equation is implemented that converts the ON width that produces a given energy in single-output operation into the ON width that produces the same energy in interleaved-output operation.

This function is enabled by default, and it can also be disabled through optional settings.

3.3.5 Debug Functions

This section describes the debug functions implemented in the software.

3.3.5.1 PFC ON-Width Output Function (Optional)

This function outputs the PFC master-side ON width (the TKBCR11 register setting value) via UART.

By enabling this option and connecting a PC through the debug board, the ON width can be monitored using terminal software.

The output is an 8-digit hexadecimal value, and the latest ON width is output at 2-ms intervals.

The value can be converted to time units [μs] using the following equation:

PFC master-side ON time [us] = output value / 96×10^6

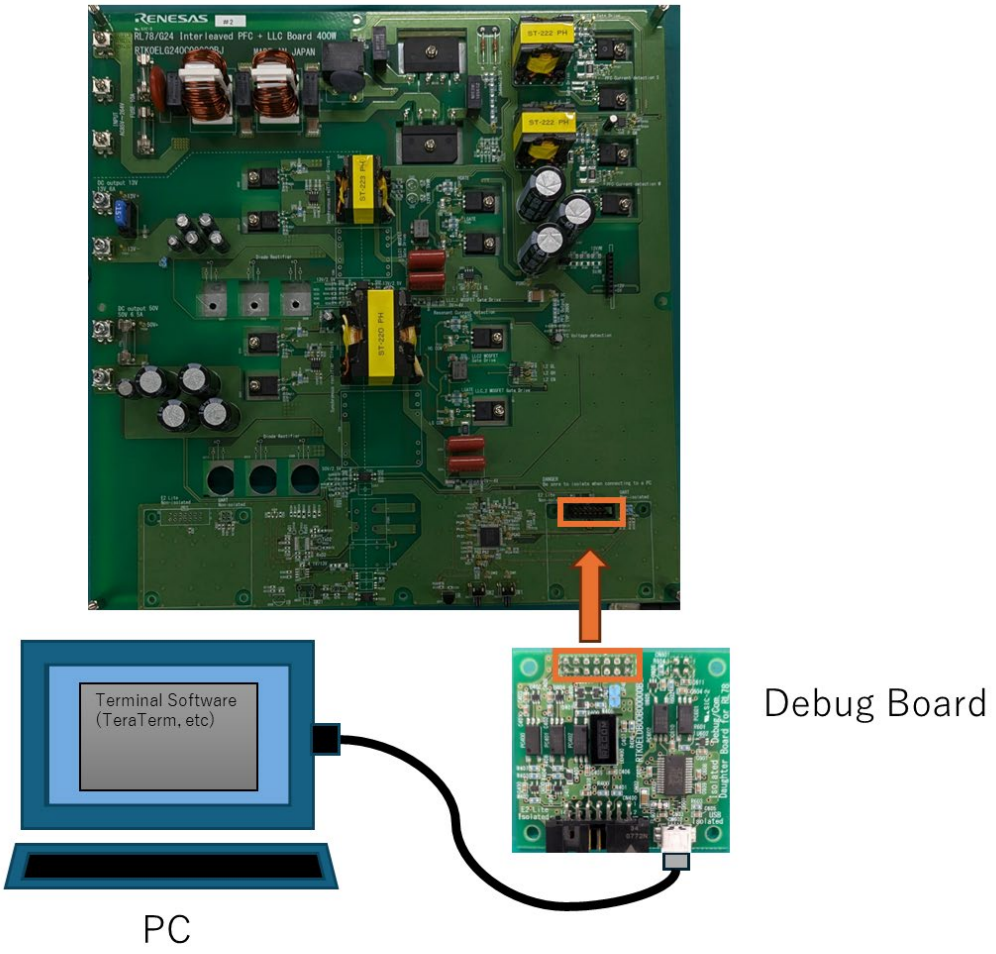


Figure 3.6 Debug Function Connection

Table 3.8 Communication Settings

Item	Setting
Baud Rate	11520bps
Data Bits	8bit
Stop Bits	None
Flow Control	None

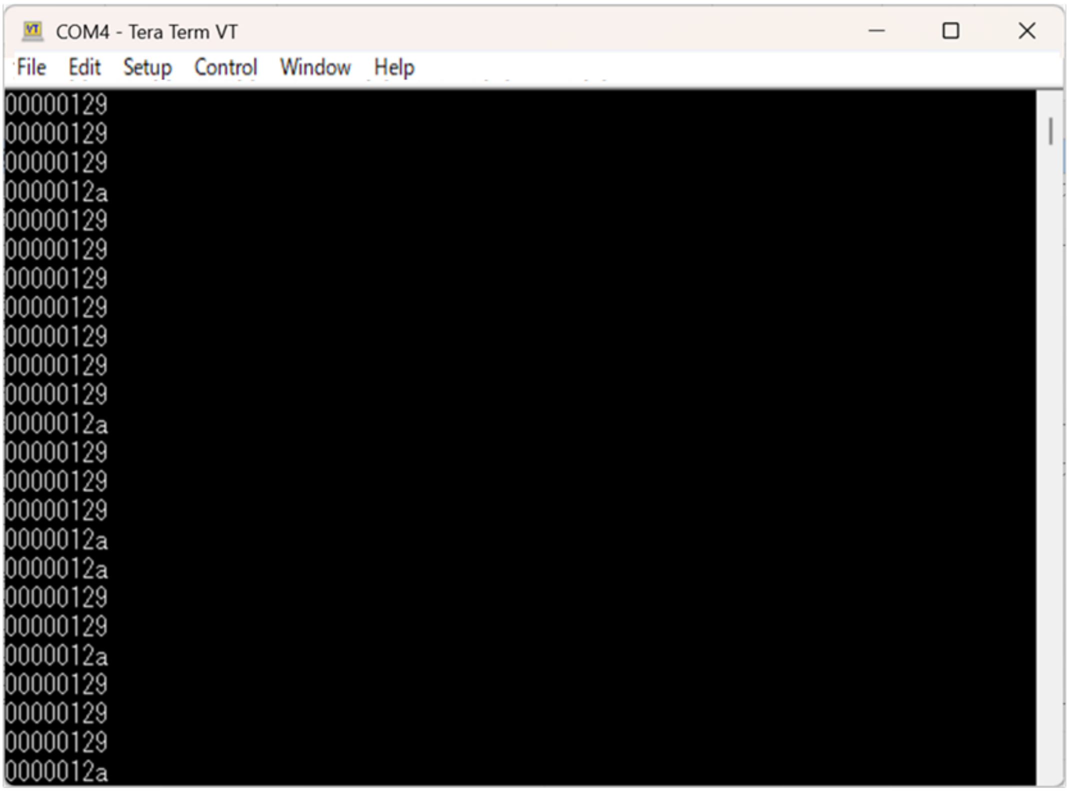


Figure 3.7 Example of Terminal Software Output

Note: This function is not available when generated with QE for Lighting & Power.

3.4 Calculation of PI-Control Coefficients

The constant-voltage control of the PFC and LLC output voltages can be achieved by using PI-control-based feedback processing. The following sections describe the PI control equations for each block and the calculation of their coefficients.

3.4.1 PFC

3.4.1.1 PI Control Equation

The PFC PI-feedback equation is shown below.

$$D(n) = D(n-1) + A_1 \times E(n) + A_2 \times E(n-1)$$

$D(n)$: Latest PWM output ON width

$D(n-1)$: Previous PWM output ON width

$E(n)$: Latest error value = (A/D conversion target value) – (latest A/D conversion measurement)

$E(n-1)$: Previous error value = (A/D conversion target value) – (previous A/D conversion measurement)

A_1, A_2: Coefficients

The feedback coefficients A_1 and A_2 are obtained from the following equations:

$$A_1 = (\pi \times f_Z \times T + 1) \times K_p$$
$$A_2 = (\pi \times f_Z \times T - 1) \times K_p$$

π: Pi (circular constant)

f_Z: Zero-point frequency

T: Feedback period

K_p: Proportional gain

Thus, the coefficients A_1 and A_2 can be calculated by determining the three parameters f_Z, T, and K_p.

3.4.1.2 Calculation of Zero-Point Frequency (f_Z) from the Pole Frequency of the Control Circuit

This control circuit contains an LC-circuit pole. This pole frequency can be regarded as equal to the cutoff frequency. Let the cutoff frequency be f_c. For L=175 μH and C=300 μF, the following value is obtained:

$$f_c = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \fallingdotseq 2.18KHz$$

A zero-point frequency f_z lower than this cutoff frequency f_c is selected.

$$f_z = 2Hz$$

3.4.1.3 Calculation of Feedback Period (T) from the Zero-Point Frequency (f_Z)

ccording to the sampling theorem, the sampling frequency—which is equal to the inverse of the feedback period T —must be at least twice the zero-point frequency f_Z.

Therefore, the relationship between the feedback period T and the zero-point frequency f_Z must satisfy the following condition:

$$T < \frac{1}{2f_Z}$$

Thus, when f_Z = 2Hz, the feedback period T must be less than 250 ms.
In this sample program, the feedback period T is configured as follows:

$$T = 400\mu s$$

3.4.1.4 Calculation of the Proportional Gain K_p from the Microcontroller Gain (ADC Input / PWM Output)

The microcontroller gain (A/D converter input / PWM output) can be calculated by focusing on how the output voltage changes with respect to the A/D conversion resolution and the PWM resolution.

First, it is necessary to determine the change in output voltage corresponding to the inherent A/D conversion resolution. When the output voltage is V_{out}, the A/D conversion result of the feedback voltage is X, the A/D conversion resolution is M bits, and the ADC reference voltage is V_{REF}, the following equation holds:

$$V_{out} = \frac{V_{REF} \times X}{2^M}$$

Here, if we denote the change in output voltage corresponding to an A/D conversion value equal to 1 (X = 1) as v_{AD}, the following result is obtained:

$$v_{AD} = \frac{V_{REF}}{2^M}$$

Next, it is necessary to determine the change in output voltage corresponding to the inherent PWM resolution. When the output voltage is V_{out}, the input voltage is V_{in}, the value of (PWM ON-width register + 1) is Y, and the PWM output resolution is N bits, the following equation holds:

$$V_{out} = \frac{V_{in} \times Y}{2^N}$$

Here, if we denote the change in output voltage corresponding to a PWM ON-width value equal to 1 (Y=1) as v_{PWM}, the following result is obtained:

$$v_{PWM} = \frac{V_{in}}{2^N}$$

Therefore, the gain $v_{PWM}/\ v_{AD}$ can be estimated from the above equations as follows:

$$\frac{v_{PWM}}{v_{AD}} = \frac{V_{in}}{V_{REF}} \times 2^{(M-N)}$$

Considering that the A/D conversion resolution M is 12 bits, the PWM output resolution is 16 bits, the input voltage V_{in} is 264 V (under AC 230 V input), and the A/D converter reference voltage V_{REF} is 5 V, the following gain result is obtained:

$$\frac{v_{PWM}}{v_{AD}} = \frac{264}{5} \times 2^{(12-16)} = 3.3125$$

The proportional gain must be set to a value smaller than the inverse of this gain:

$$K_p < \frac{1}{\left(\frac{v_{PWM}}{v_{AD}}\right)} \cong 0.302$$

Here, K_p is selected as follows:

$$K_p = 0.25$$

From the above results, the PI-control coefficients A_1 and A_2 can be calculated:

$$A_1 = 0.25031$$
$$A_2 = -0.24969$$

In this sample program, both coefficients are handled as integer variables, just like the PWM ON width and the error value. To simplify computation, they are multiplied by 2^{16}(=65536):

$$A_1 = 16425$$
$$A_2 = -16343$$

3.4.2 LLC1

3.4.2.1 PI Control Equation

The PI control equation for LLC1 feedback is shown below:

$$P(n) = P(n-1) + A_1 \times E(n) + A_2 \times E(n-1)$$

$P(n)$: Latest PFM output period

$P(n-1)$: Previous PFM output period

$E(n)$: Latest error value = (A/D conversion target value) − (latest A/D conversion measurement)

$E(n-1)$: Previous error value = (A/D conversion target value) − (previous A/D conversion measurement)

A_1, A_2: Coefficients

The feedback coefficients A_1 and A_2 are obtained from the following equations:

$$A_1 = (\pi \times f_Z \times T + 1) \times K_p$$
$$A_2 = (\pi \times f_Z \times T - 1) \times K_p$$

π: Pi (circular constant)

f_Z: Zero-point frequency

T: Feedback period

K_p: Proportional gain

Thus, the coefficients A_1 and A_2 can be calculated by determining the three parameters f_Z, T, and K_p.

3.4.2.2 Calculation of the Zero-Point Frequency (f_Z) from the Pole Frequency of the Control Circuit

This control circuit contains an LC-circuit pole. This pole frequency can be regarded as equal to the cutoff frequency. Let the cutoff frequency be f_c. For L=600 μH and C=44 nF, the following value is obtained:

$$f_c = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} = 30.975KHz$$

A zero-point frequency f_z lower than this cutoff frequency f is selected.

$$f_z = 1.5KHz$$

3.4.2.3 Calculation of the Feedback Period (T) from the Zero-Point Frequency (f_Z)

According to the sampling theorem, the sampling frequency—which is equal to the inverse of the feedback period T —must be at least twice the zero-point frequency f_Z.

Therefore, the relationship between the feedback period T and the zero-point frequency f_Z must satisfy the following condition:

$$T < \frac{1}{2f_Z}$$

Thus, when f_Z=1.5KHz, the feedback period T must be less than 333.3 μs.

In this sample program, the feedback period T is configured as follows

$$T = 200\mu s$$

3.4.2.4 Calculation of the Proportional Gain K_p from the Microcontroller Gain (ADC Input / PFM Output)

The microcontroller gain (A/D converter input / PFM output) can be obtained by examining how the output voltage changes with respect to the A/D conversion resolution and the PFM resolution.

First, it is necessary to determine the change in output voltage corresponding to the inherent A/D conversion resolution. When the output voltage is V_{out}, the A/D conversion result of the feedback voltage is X, the A/D conversion resolution is M bits, and the ADC reference voltage is V_{REF}, the following equation holds:

$$V_{out} = \frac{V_{REF} \times X}{2^M}$$

Here, if we denote the change in output voltage corresponding to an A/D conversion value equal to 1 (X=1) as v_{AD}, the following result is obtained:

$$v_{AD} = \frac{V_{REF}}{2^M}$$

Next, it is necessary to determine the change in output voltage corresponding to the inherent PFM resolution. When the output voltage is V_{out}, the input voltage is V_{in}, the value of (PFM period register + 1) is Y, and the PFM output resolution is N bits, the following equation holds:

$$V_{out} = \frac{V_{in} \times Y}{2^N}$$

Here, if we denote the change in output voltage corresponding to a PFM period value equal to 1 (Y=1) as v_{PWM}, the following result is obtained:

$$v_{PWM} = \frac{V_{in}}{2^N}$$

Therefore, the gain $v_{PWM}/\ v_{AD}$ can be estimated from the above equations as follows:

$$\frac{v_{PWM}}{v_{AD}} = \frac{V_{in}}{V_{REF}} \times 2^{(M-N)}$$

Considering that the A/D conversion resolution M is 12 bits, the PFM output resolution is 16 bits, the input voltage V_{in} is 386 V, and the A/D converter reference voltage V_{REF} is 5 V, the following gain result is obtained:

$$\frac{v_{PWM}}{v_{AD}} = \frac{386}{5} \times 2^{(12-6)} = 4.825$$

The proportional gain must be set to a value smaller than the inverse of this gain:

$$K_p < \frac{1}{\left(\frac{v_{PWM}}{v_{AD}}\right)} = 0.207$$

Here, K_p is selected as follows:

$$K_p = 0.015625$$

From the above results, the PI-control coefficients A_1 and A_2 can be calculated:

$$A_1 = 0.030361$$
$$A_2 = -0.000899$$

In this sample program, both coefficients are handled as integer variables, just like the PFM period and the error value. To simplify computation, they are multiplied by 2^{16}(=65536):

$$A_1 = 1989$$
$$A_2 = -59$$

3.4.3 LLC2

3.4.3.1 PI Control Equation

The PI control equation for LLC2 feedback is shown below:

$$P(n) = P(n-1) + A_1 \times E(n) + A_2 \times E(n-1)$$

$P(n)$: Latest PFM output period

$P(n-1)$: Previous PFM output period

$E(n)$: Latest error value = (A/D conversion target value) − (latest A/D conversion measurement)

$E(n-1)$: Previous error value = (A/D conversion target value) − (previous A/D conversion measurement)

A_1, A_2: Coefficients

The feedback coefficients A_1 and A_2 are obtained from the following equations:

$$A_1 = (\pi \times f_Z \times T + 1) \times K_p$$
$$A_2 = (\pi \times f_Z \times T - 1) \times K_p$$

π: Pi (circular constant)

f_Z: Zero-point frequency

T: Feedback period

K_p: Proportional gain

Thus, the coefficients A_1 and A_2 can be calculated by determining the three parameters f_Z, T, and K_p.

3.4.3.2 Calculation of the Zero-Point Frequency (f_Z) from the Pole Frequency of the Control Circuit

This control circuit contains an LC-circuit pole. This pole frequency can be regarded as equal to the cutoff frequency. Let the cutoff frequency be f_c. For L=500 μH and C=44 nF, the following value is obtained:

$$f_c = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} = 33.931KHz$$

A zero-point frequency f_z lower than this cutoff frequency f_c is selected.

$$f_z = 1.25KHz$$

3.4.3.3 Calculation of the Feedback Period (T) from the Zero-Point Frequency (f_Z)

According to the sampling theorem, the sampling frequency—which is equal to the inverse of the feedback period T—must be at least twice the zero-point frequency f_Z.

Therefore, the relationship between the feedback period T and the zero-point frequency f_Z must satisfy the following condition:

$$T < \frac{1}{2f_Z}$$

Thus, when f_Z = 1.25KHz, the feedback period T must be less than 400 µs.
In this sample program, the feedback period T is configured as follows:

$$T = 200\mu s$$

3.4.3.4 Calculation of the Proportional Gain K_p from the Microcontroller Gain (ADC Input / PFM Output)

The microcontroller gain (A/D converter input / PFM output) can be obtained by examining how the output voltage changes with respect to the A/D conversion resolution and the PFM resolution.

First, it is necessary to determine the change in output voltage corresponding to the inherent A/D conversion resolution. When the output voltage is V_{out}, the A/D conversion result of the feedback voltage is X, the A/D conversion resolution is M bits, and the ADC reference voltage is V_{REF}, the following equation holds:

$$V_{out} = \frac{V_{REF} \times X}{2^M}$$

Here, if we denote the change in output voltage corresponding to an A/D conversion value equal to 1 (X=1) as v_{AD}, the following result is obtained:

$$v_{AD} = \frac{V_{REF}}{2^M}$$

Next, it is necessary to determine the change in output voltage corresponding to the inherent PFM resolution. When the output voltage is V_{out}, the input voltage is V_{in}, the value of (PFM period register + 1) is Y, and the PFM output resolution is N bits, the following equation holds:

$$V_{out} = \frac{V_{in} \times Y}{2^N}$$

Here, if we denote the change in output voltage corresponding to a PFM period value equal to 1 (Y=1) as v_{PWM}, the following result is obtained:

$$v_{PWM} = \frac{V_{in}}{2^N}$$

Therefore, the gain $v_{PWM}/\ v_{AD}$ can be estimated from the above equations as follows:

$$\frac{v_{PWM}}{v_{AD}} = \frac{V_{in}}{V_{REF}} \times 2^{(M-N)}$$

Considering that the A/D conversion resolution M is 12 bits, the PFM output resolution is 16 bits, the input voltage V_{in} is 386 V, and the A/D converter reference voltage V_{REF} is 5 V, the following gain result is obtained:

$$\frac{v_{PWM}}{v_{AD}} = \frac{386}{5} \times 2^{(12-6)} = 4.825$$

The proportional gain must be set to a value smaller than the inverse of this gain:

$$K_p < \frac{1}{\left(\frac{v_{PWM}}{v_{AD}}\right)} = 0.207$$

Here, K_p is selected as follows:

$$K_p = 0.059375$$

From the above results, the PI-control coefficients A_1 and A_2 can be calculated:

$$A_1 = 0.106008$$
$$A_2 = -0.012742$$

In this sample program, both coefficients are handled as integer variables, just like the PFM period and the error value. To simplify computation, they are multiplied by 2^{16}(=65536):

$$A_1 = 6947$$
$$A_2 = -835$$

4. Test Results

Tests were conducted using the hardware and software covered in this document. The results of these tests are described below.

4.1 Test Conditions

Operation was verified under the connection conditions and input/output conditions described below.

4.1.1 Connection Environment

The hardware connection environment is shown in Figure 4.1.

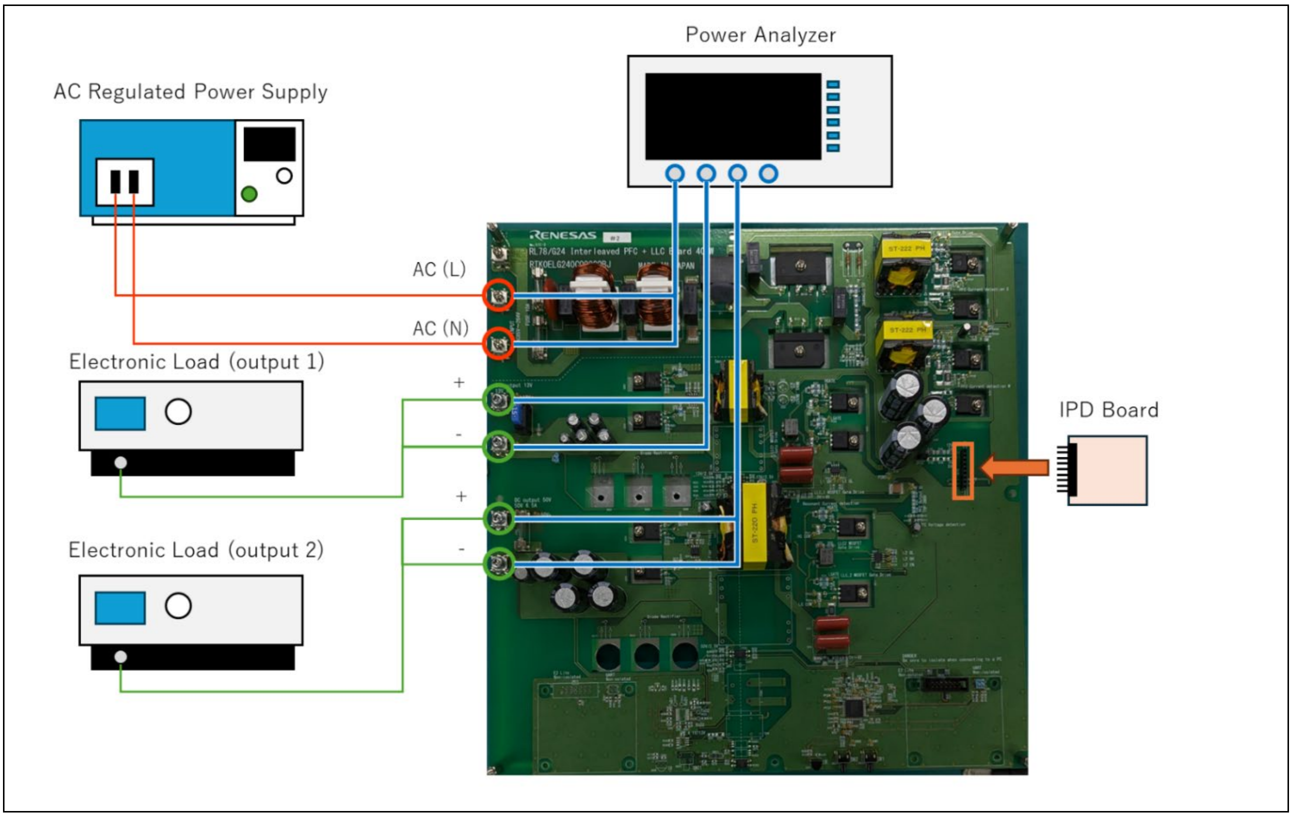


Figure 4.1 Test Connection Environment

In addition, the model numbers of the equipment used for the test connections are listed in Table 4.1.

Table 4.1 List of Test Equipment Model Numbers

Item	Model Number
AC Regulated Power Supply	Kikusui Electronics Corp. PCR500MA
Electronic Load (Output 1)	Measurement Technology Laboratory, Inc. ELC-1005
Electronic Load (Output 2)	Kikusui Electronics Corp. PLZ1003WH / ELC-1005
Power Analyzer	Yokogawa Test & Measurement Corporation WT500

4.1.2 Input Conditions

The input conditions during the test are shown below.

Table 4.2 Test Input Conditions

Item	Value
Input Voltage	AC 100V, AC 230V
Frequency	60 Hz
Current Limit	6 A

4.1.3 Load Conditions

The load conditions during the test are shown below.

Table 4.3 Test Load Conditions

Item	Condition	Value
Electronic Load Current (Output 1)	Standby	0.015 A
	Normal	0.015 A–6 A
Electronic Load Current (Output 2)	Standby	0.1 A
	Normal	0.1 A–6.5 A

4.2 Standby Power

The measured standby power in Standby mode is shown below.

Table 4.4 Standby Power

Input Voltage	Load Power (Output 1)	Standby Power
AC 100 V	0.15 W	279.422 mW
AC 230 V	0.15 W	275.439 mW

4.3 Efficiency and Power Factor

The efficiency and power factor for each load condition in Normal mode are presented below.

Results are provided for both cases: with the maximum-frequency-limit function enabled and disabled.

4.3.1 At AC 100 V Input

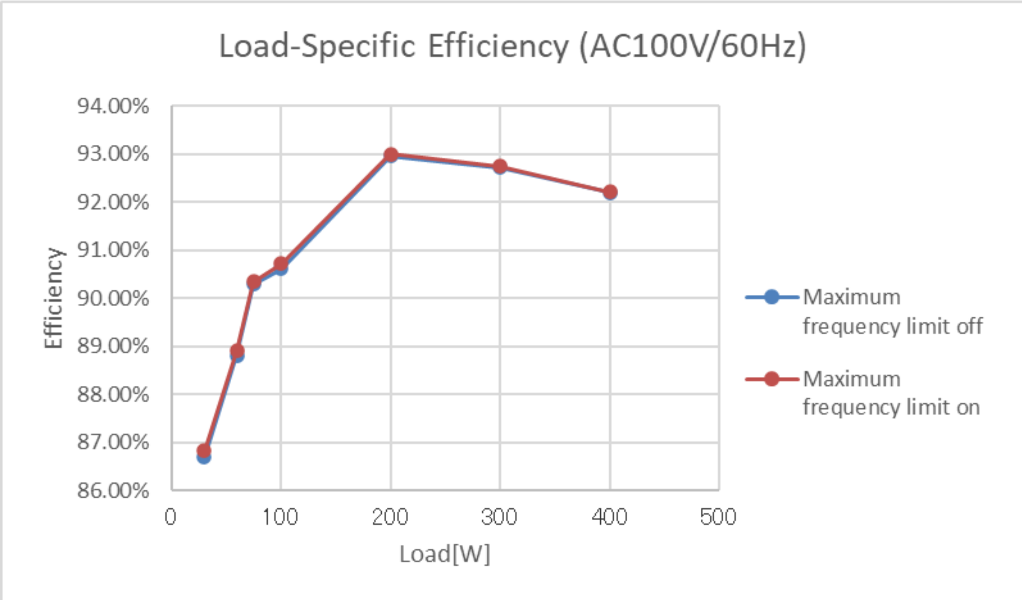


Figure 4.2 Load vs. Efficiency at AC 100 V Input

Table 4.5 Efficiency and Power Factor at AC 100 V Input (Maximum-Frequency-Limit OFF)

V_{in}[V]	I_{in}[A]	P_{in}[W]	V_{out1}[V]	I_{out1}[A]	P_{out1}[W]	V_{out2}[V]	I_{out2}[A]	P_{out2}[W]	Efficiency	Power Factor
100.08	0.3793	36.10	12.932	2.4161	31.25	0.000	0.000	0.000	86.69%	95.08%
100.05	0.7139	69.86	12.930	2.4161	31.24	49.114	0.626	30.766	88.81%	97.79%
100.40	0.8642	84.98	12.929	2.4161	31.24	49.111	0.926	45.474	90.29%	98.30%
100.00	1.1434	111.81	12.929	2.4161	31.24	49.116	1.427	70.070	90.61%	97.74%
99.95	2.1937	217.10	12.930	2.4162	31.24	49.086	3.474	170.560	92.96%	99.03%
99.86	3.2750	325.20	12.927	2.416	31.24	49.062	5.509	270.330	92.72%	99.45%
99.76	4.4085	438.20	12.893	6.117	78.87	49.047	6.629	325.160	92.19%	99.65%

Table 4.6 Efficiency and Power Factor at AC 100 V Input (Maximum-Frequency-Limit ON)

V_{in}[V]	I_{in}[A]	P_{in}[W]	V_{out1}[V]	I_{out1}[A]	P_{out1}[W]	V_{out2}[V]	I_{out2}[A]	P_{out2}[W]	Efficiency	Power Factor
100.08	0.3791	36.16	12.932	2.416	34.25	0.000	0.000	0.000	86.83%	95.28%
100.50	0.7133	69.79	12.929	2.416	31.24	49.114	0.626	30.762	88.90%	97.80%
100.40	0.8638	84.38	12.929	2.4161	31.24	49.110	0.926	45.474	90.35%	98.30%
100.01	1.1396	112.27	12.927	2.4161	31.24	49.101	1.438	70.620	90.72%	98.51%
99.94	2.1932	217.10	12.929	2.4163	31.25	49.085	3.474	170.550	93.01%	99.03%
99.85	3.2756	325.20	12.927	2.416	31.24	49.062	5.509	270.330	92.75%	99.45%
99.76	4.4081	438.20	12.892	6.117	78.87	49.047	6.629	325.160	92.21%	99.65%

4.3.2 At AC 230 V Input

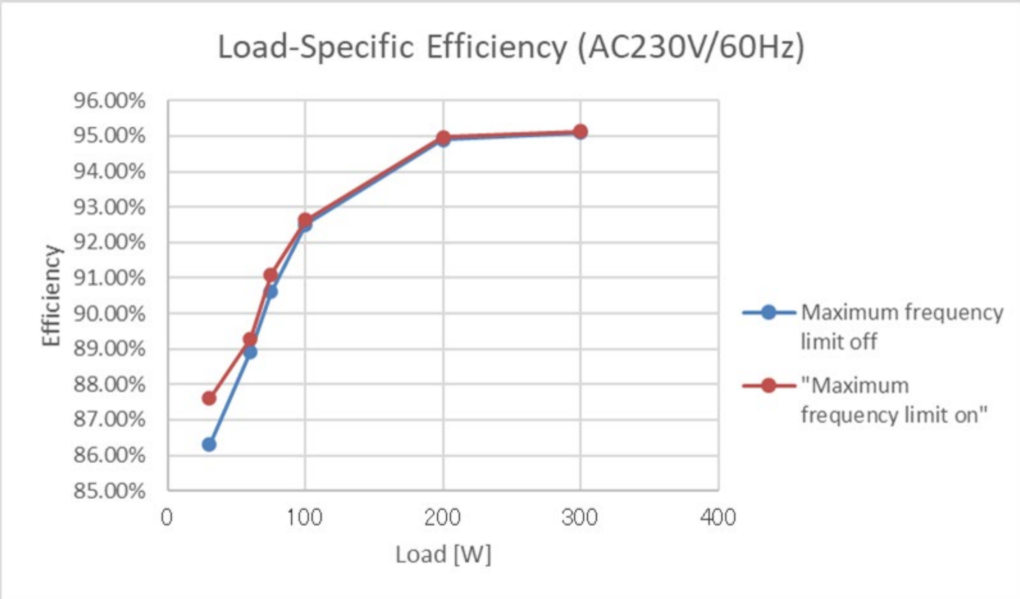


Figure 4.3 Load vs. Efficiency at AC 230 V Input

Table 4.7 Efficiency and Power Factor at AC 230 V Input (Maximum-Frequency-Limit OFF)

V_{in}[V]	I_{in}[A]	P_{in}[W]	V_{out1}[V]	I_{out1}[A]	P_{out1}[W]	V_{out2}[V]	I_{out2}[A]	P_{out2}[W]	Efficiency	Power Factor
230.01	0.2534	35.54	12.932	2.416	31.25	0.000	0.000	0.000	86.30%	61.30%
230.21	0.3473	69.22	12.930	2.4162	31.25	49.116	0.617	30.285	88.92%	86.45%
230.20	0.4123	85.22	12.930	2.4162	31.25	49.111	0.936	45.983	90.61%	89.78%
230.18	0.5131	109.63	12.930	2.4162	31.25	49.105	1.429	70.170	92.51%	92.80%
230.16	0.9517	212.28	12.930	2.4162	31.25	49.088	3.464	170.070	94.90%	97.06%
230.14	1.4031	317.74	12.930	2.4162	31.25	49.068	5.519	270.840	95.10%	98.39%
230.09	1.8703	425.74	12.896	6.116	78.89	49.055	6.628	325.190	95.00%	98.85%

Table 4.8 Efficiency and Power Factor at AC 230 V Input (Maximum-Frequency-Limit ON)

V_{in}[V]	I_{in}[A]	P_{in}[W]	V_{out1}[V]	I_{out1}[A]	P_{out1}[W]	V_{out2}[V]	I_{out2}[A]	P_{out2}[W]	Efficiency	Power Factor
229.86	0.2440	36.65	12.930	2.4154	31.24	0.000	0.000	0.000	87.61%	73.04%
230.22	0.3542	68.95	12.930	2.416	31.25	49.115	0.617	30.282	89.28%	84.57%
230.21	0.4213	84.81	12.930	2.4161	31.24	49.111	0.936	45.980	91.09%	87.43%
230.20	0.5330	109.48	12.930	2.4162	31.24	49.105	1.429	70.160	92.63%	89.25%
230.16	0.9484	212.19	12.930	2.4162	31.25	49.087	3.464	170.070	94.97%	97.22%
230.13	1.4131	317.69	12.930	2.416	31.24	49.068	5.519	270.840	95.14%	98.39%

5. Notes

-
- This sample application is configured and operates for Interleaved CrM PFC and LLC control using the RL78/G24.
- The sample program operations provided in this document are just examples. The application layer must be modified and evaluated according to the intended use.

6. Reference Documents

RL78/G24 User's Manual: Hardware (R01UH0961)

RL78 Family User's Manual: Software (R01US0015)

Obtain the latest version of the manual from the website of Renesas Electronics.

Technical Update/Technical News

Obtain the latest information from the website of Renesas Electronics.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2026.03.19	—	First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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