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SH7080 Group

Input Capture Function Using MTU2 in Cascade Connection (32-bit Counter)

Introduction

This application note describes the input capture operation of the multi-function timer pulse unit 2 (MTU2) with its channels in cascade connection (32-bit counter). The input capture operation is driven by an external signal.
Please use this application note as a guide in designing user programs.

Although the programs given in this application note have been verified for correct operation, we strongly recommend that the user confirm correct operation before applying the programs in the actual application.

Target Device

SH7085

Contents

1. Specifications

In this sample application, the channels 1 and 2 (CH1 and CH2) of the MTU2 are cascaded to operate as a 32-bit counter, and counter values are captured with the timing provided by an external input signal. Figure 1 shows the basic specifications of this sample task.

- Channels 1 and 2 of the MTU2 are connected in cascade. In the cascade connection, the timer counter TCNT_1 in channel 1 and TCNT_2 in channel 2 count the upper and lower 16 bits, respectively. This results in 32-bit counter operation.
- TGRA_2 and TGRA_1 registers store the captured values of the timer counters TCNT_2 and TCNT_1 respectively. The counter values are captured on the rising edge of the externally input pulse.
- The TIOC2A pin of channel 2 in the MTU2 functions as the external pulse input pin.

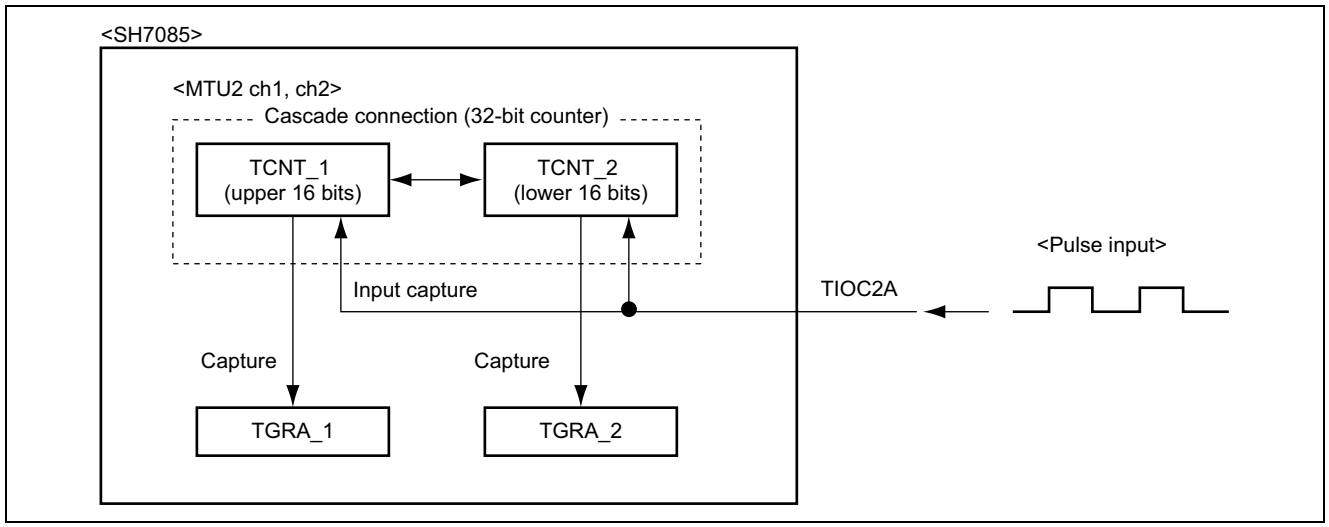


Figure 1 Overview

2. Conditions for Application

Operating frequency:	Internal clock:	80 MHz
	Bus clock:	40 MHz
	Peripheral clock:	40 MHz
	MTU2 clock:	40 MHz
	MTU2S clock:	80 MHz
C compiler:	Version 7.1.04 from Renesas Technology Corp.	

3. MCU Functions Used

In this sample task, input capture operation is performed using the cascaded channel 1 and channel 2 of the MTU2. Figure 2 outlines the operation.

The timer counters TCNT_1 and TCNT_2 are cascaded to operate as a 32-bit counter. Timer counter TCNT_2 is driven by the internal MTU2 clock (MPϕ) and operates as a lower 16-bit counter. Timer counter TCNT_1 operates as an upper 16-bit counter, and is incremented on overflow/underflow of TCNT_2.

On channel 2, input capture occurs on the rising edge of the external pulse that is input from the TIOC2A pin. At the same time, an input capture interrupt (TGIA_2 interrupt) is generated to the CPU. Input capture on channel 1 is driven by the input capture of channel 2, which is specified by the setting of the timer input capture control register (TICCR). The input captures on channel 1 and channel 2 occur simultaneously.

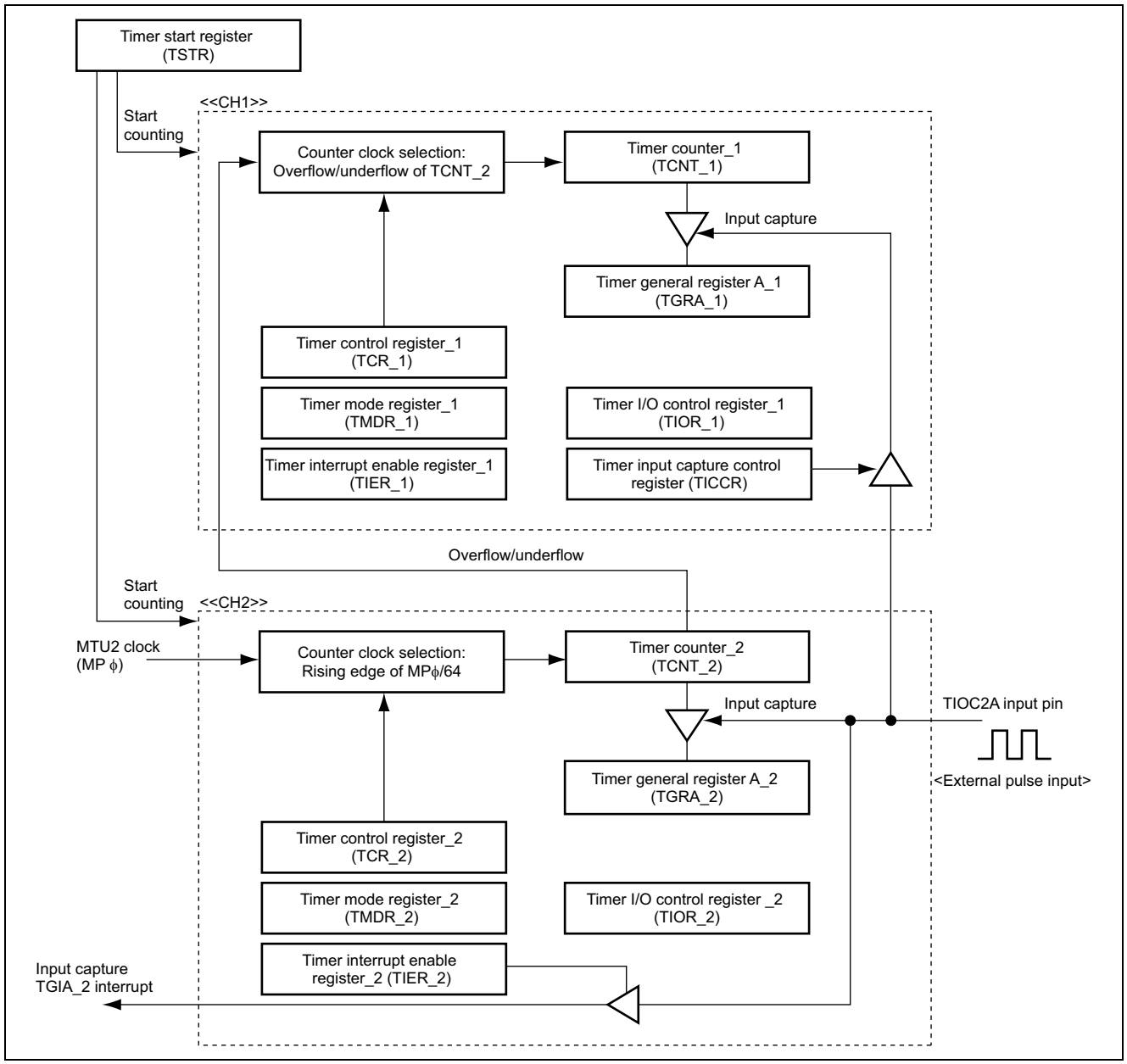


Figure 2 Operational Block Diagram of MTU2 (Channel 1 and Channel 2)

- Timer counter_1 (TCNT_1) is a 16-bit readable/writable counter. TCNT_1 is incremented on every overflow/underflow of TCNT_2.
- Timer general register A_1 (TGRA_1) is a 16-bit readable/writable register. TGRA_1 operates as an input capture register.
- Timer I/O control register_1 (TIOR_1) is an 8-bit readable/writable register that specifies the functions of TGRA_1 and TGRB_1. TGRA_1 is set to operate as the input capture register.
- Timer interrupt enable register_1 (TIER_1) is an 8-bit readable/writable register. TIER_1 enables/disables interrupt requests caused by registers TGRA_1 and TGRB_1, overflow flag TCFV, and underflow flag TCFU. It also enables/disables the A/D converter activation request by TGRA_1.
- Timer mode register_1 (TMDR_1) is an 8-bit readable/writable register that specifies the operating mode.
- Timer control register_1 (TCR_1) is an 8-bit readable/writable register that controls the operation of TCNT_1.
- Timer input capture control register (TICCR) is an 8-bit readable/writable register that specifies the input capture conditions when TCNT_1 and TCNT_2 are connected in cascade.
- Timer counter_2 (TCNT_2) is a 16-bit readable/writable counter. Counting by TCNT_2 is driven by the MTU2 clock (MPϕ).
- Timer general register A_2 (TGRA_2) is a 16-bit readable/writable. TGRA_2 operates as an input capture register.
- Timer I/O control register _2 (TIOR_2) is an 8-bit readable/writable register that specifies the functions of TGRA_2 and TGRB_2. TGRA_2 is set to operate as the input capture register.
- Timer interrupt enable register_2 (TIER_2) is an 8-bit readable/writable register. TIER_2 enables/disables interrupt requests caused by registers TGRA_2, overflow flag TCFV, and underflow flag TCFU. It also enables/disables the A/D converter start request by TGRA_2.
- Timer mode register_2 (TMDR_2) is an 8-bit readable/writable register that specifies the operating mode.
- Timer control register_2 (TCR_2) is an 8-bit readable/writable register that controls the operation of TCNT_2.
- The timer start register (TSTR) is an 8-bit readable/writable register that starts/stops the timer counters of channels 0 to 4.

4. Operation

Figure 3 shows the operation of the sample application, and table 1 describes the software and hardware processing.

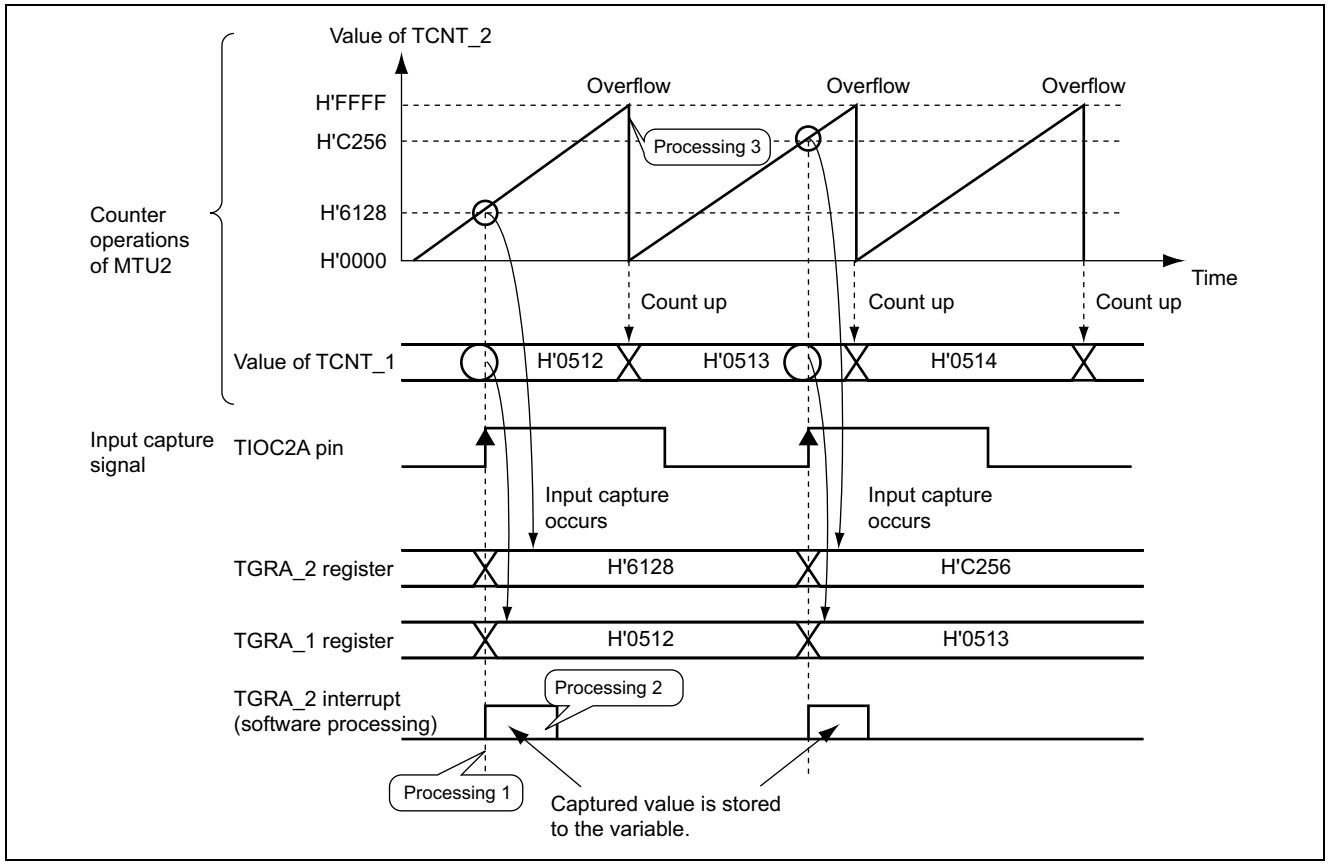


Figure 3 Operation

Table 1 Software and Hardware Processing

	Software Processing	Hardware Processing
Processing 1	—	TGRA_2 input capture occurs at the rising edge on the TIOC2A pin. TGRA_1 input capture occurs at the rising edge on the TIOC2A pin. Stores the captured TCNT_2/TCNT_1 values into the TGRA_2/TGRA_1 registers.
Processing 2	Clears the interrupt flag to 0. Stores the captured values to a variable.	Generates a TGRA_2 input capture interrupt.
Processing 3	—	TCNT_2 overflows. Increments TCNT_1.

5. Description of Software

5.1 Modules

Table 2 describes the modules used in the sample task.

Table 2 Description of Modules

Module Name	Label Name	Functions
Main routine	main()	Makes initial settings for the MTU2 and starts the timer counters.
TGRA_2 input capture interrupt routine	Int_mtu2_tgia2()	Clears the interrupt flag and stores the captured values to a variable.

5.2 Variable

Table 3 shows the variable used for the sample task.

Table 3 Description of Variable

Label Name of Variable	Function	Used in
unsigned long Cap_data32	The captured values of TCNT_1 (lower 16 bits) and TCNT_2 (upper 16 bits) are stored.	TGRA_2 input capture interrupt routine

5.3 Register Settings

The register settings used in the sample application are described below. Note that the setting values are specifically used in the sample task, and that they are different from the initial values.

5.3.1 Settings for the Clock Pulse Generator (CPG)

- Frequency Control Register (FRQCR)
  - Setting value: H'0241
  - Function: Specifies the frequency division ratios.

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	IFC[2] to IFC[0]	000	Frequency division ratio for internal clock (Iϕ) 000: ×1 (80 MHz when the input clock frequency is 10 MHz)
11 to 9	BFC[2] to BFC[0]	001	Frequency division ratio for bus clock (Bϕ) 001: ×1/2 (40 MHz when the input clock frequency is 10 MHz)
8 to 6	PFC[2] to PFC[0]	001	Frequency division ratio for peripheral clock (Pϕ) 001: ×1/2 (40 MHz when the input clock frequency is 10 MHz)
5 to 3	MIFC[2] to MIFC[0]	000	Frequency division ratio for MTU2S clock (MIϕ) 000: ×1 (80 MHz when the input clock frequency is 10 MHz)
2 to 0	MPFC[2] to MPFC[0]	001	Frequency division ratio for MTU2 clock (MPϕ) 001: ×1/2 (40 MHz when the input clock frequency is 10 MHz)

5.3.2 Settings for Power-Down Modes

- Standby Control Register 4 (STBCR4)
  - Setting value: H'bf
  - Function: Controls the operation of the modules in power-down modes.

Bit	Bit Name	Value	Description
7	MSTP23	1	1: Stops supply of the clock signal to the MTU2S.
6	MSTP22	0	0: The MTU2 runs.
5	MSTP21	1	1: Stops supply of the clock signal to the CMT.
4, 3	—	11	Reserved
2	MSTP18	1	1: Stops supply of the clock signal to the A/D_2.
1	MSTP17	1	1: Stops supply of the clock signal to the A/D_1.
0	MSTP16	1	1: Stops supply of the clock signal to the A/D_0.

5.3.3 Settings for Channel 1 of Multi-Function Timer Pulse Unit 2 (MTU2)

- Timer Control Register_1 (TCR_1)
  - Setting value: H'07
  - Function: Controls TCNT of channel 1.

Bit	Bit Name	Value	Description
7 to 5	CCLR[2] to CCLR[0]	000	000: Clearing of TCNT is disabled.
4, 3	CKEG[1], CKEG[0]	00	00: TCNT is incremented on the rising edge.
2 to 0	TPSC[2] to TPSC[0]	111	111: Counting is driven by overflow/underflow of TCNT_2.

- Timer Mode Register_1 (TMDR_1)
  - Setting value: H'00
  - Function: Specifies the operating mode of channel 1.

Bit	Bit Name	Value	Description
7	—	0	Reserved
6	—	0	Reserved in channels 1 to 4
5	—	0	Reserved in channels 1 and 2
4	BFA	0	0: TGRA and TGRC operate normally.
3 to 0	MD[3] to MD[0]	0000	These bits select the operating mode of the timer. 0000: Normal mode

- Timer Counter_1 (TCNT_1)
  - Setting value: H'0000
  - Function: 16-bit counter

- Timer I/O Control Register _1 (TIOR_1)
  - Setting value: H'08
  - Function: Controls TGRs.

Bit	Bit Name	Value	Description
7 to 4	IOB[3] to IOB[0]	0000	0000: TGRB_1 operates as an output compare register. TheTIOC1B pin retains its output level.
3 to 0	IOA[3] to IOA[0]	1000	1000: TGRA_1 operates as an input capture register. Input capture occurs on the rising edge of the TIOC1A pin.

- Timer Interrupt Enable Register_1 (TIER_1)
  - Setting value: H'00
  - Function: Enables/disables interrupt requests from channel 1.

Bit	Bit Name	Value	Description
7	TTGE	0	0: Disables generation of A/D converter start requests.
6	—	0	Reserved
5	TCIEU	0	0: Disables interrupt requests (TCIU) by the TCFU flag.
4	TCIEV	0	0: Disables interrupt requests (TCIV) by the TCFV flag.
3	—	0	Reserved
2	—	0	Reserved
1	TGIEB	0	0: Disables interrupt requests (TGIB) by the TGFB flag.
0	TGIEA	0	0: Disables interrupt requests (TGIA) by the TGFA flag.

- Timer Input Capture Control Register (TICCR)
  - Setting value: H'04
  - Function: Specifies input capture conditions in the case where TCNT_1 and TCNT_2 are cascaded.

Bit	Bit Name	Value	Description
7 to 4	—	0	Reserved
3	I2BE	0	0: TIOC2B pin is not included as a TGRB_1 input capture condition.
2	I2AE	1	1: TIOC2A pin is included as a TGRA_1 input capture condition.
1	I1BE	0	0: TIOC1B pin is not included as aTGRB_2 input capture condition.
0	I1AE	0	0: TIOC1A pin is not included as a TGRA_2 input capture condition.

5.3.4 Settings for Channel 2 of Multi-Function Timer Pulse Unit 2 (MTU2)

- Timer Control Register_2 (TCR_2)
  - Setting value: H'03
  - Function: Controls TCNT of channel 2.

Bit	Bit Name	Value	Description
7 to 5	CCLR[2] to CCLR[0]	000	000: Clearing of TCNT is disabled.
4 and 3	CKEG[1], CKEG[0]	00	00: TCNT is incremented on the rising edge of the clock.
2 to 0	TPSC[2] to TPSC[0]	011	011: Counting is driven by internal clock MPϕ/64.

- Timer Mode Register_2 (TMDR_2)
  - Setting value: H'00
  - Function: Sets the operating mode of channel 2.

Bit	Bit Name	Value	Description
7	—	0	Reserved
6	—	0	Reserved in channels 1 to 4
5	—	0	Reserved in channels 1 and 2
4	BFA	0	0: TGRA and TGRC operate normally.
3 to 0	MD[3] to MD[0]	0000	These bits select the operating mode of the timer. 0000: Normal mode

- Timer Counter_2 (TCNT_2)
  - Setting value: H'0000
  - Function: 16-bit counter

- Timer I/O Control Register _2 (TIOR_2)
  - Setting value: H'08
  - Function: Controls TGRs.

Bit	Bit Name	Value	Description
7 to 4	IOB[3] to IOB[0]	0000	0000: TGRB_2 operates as an output compare register. TheTIOC2B pin retains its output level.
3 to 0	IOA[3] to IOA[0]	1000	1000: TGRA_2 operates as an input capture register. Input capture occurs on the rising edge of the TIOC2A pin.

- Timer Interrupt Enable Register_2 (TIER_2)
  - Setting value: H'01
  - Function: Enables/disables interrupt requests from channel 2.

Bit	Bit Name	Value	Description
7	TTGE	0	0: Disables generation of A/D converter activation requests.
6	—	0	Reserved
5	TCIEU	0	0: Disables interrupt requests (TCIU) by the TCFU flag.
4	TCIEV	0	0: Disables interrupt requests (TCIV) by the TCFV flag.
3	—	0	Reserved
2	—	0	Reserved
1	TGIEB	0	0: Disables interrupt requests (TGIB) by the TGFB flag.
0	TGIEA	1	1: Enables interrupt requests (TGIA) by the TGFA flag.

5.3.5 Settings Common to All Channels of Multi-Function Timer Pulse Unit 2 (MTU2)

- Timer Start Register (TSTR)
  - Setting value: H'06
  - Function: Starts/stops TCNTs of channels 0 to 4.

Bit	Bit Name	Value	Description
7	CTS4	0	0: Stops counting by TCNT_4.
6	CTS3	0	0: Stops counting by TCNT_3.
5 to 3	—	000	Reserved
2	CTS2	1	1: Starts counting by TCNT_2.
1	CTS1	1	1: Starts counting by TCNT_1.
0	CTS0	0	0: Stops counting by TCNT_0.

5.3.6 Settings for Pin Function Controller (PFC)

- Port E Control Register L4 (PECRL4)
  - Setting value: H'0000
  - Function: Selects functions of the multiplexed pins (PE15 to PE12) of port E.

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	PE15MD[2] to PE15MD[0]	000	PE15 mode 000: PE15 I/O (port)
11	—	0	Reserved
10 to 8	PE14MD[2] to PE14MD[0]	000	PE14 mode 000: PE14 I/O (port)
7, 6	—	00	Reserved
5, 4	PE13MD[1] and PE13MD[0]	00	PE13 mode 00: PE13 I/O (port)
3	—	0	Reserved
2 to 0	PE12MD[2] to PE12MD[0]	000	PE12 mode 000: PE12 I/O (port)

- Port E Control Register L3 (PECRL3)
  - Setting value: H'0000
  - Function: Selects functions of the multiplexed pins (PE11 to PE8) of port E.

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	PE11MD[2] to PE11MD[0]	000	PE11 mode 000: PE11 I/O (port)
11	—	0	Reserved
10 to 8	PE10MD[2] to PE10MD[0]	000	PE10 mode 000: PE10 I/O (port)
7	—	0	Reserved
6 to 4	PE9MD[2] to PE9MD[0]	000	PE9 mode 000: PE9 I/O (port)
3	—	0	Reserved
2 to 0	PE8MD[2] to PE8MD[0]	000	PE8 mode 000: PE8 I/O (port)

- Port E Control Register L2 (PECRL2)
  - Setting value: H'0100
  - Function: Selects functions of the multiplexed pins (PE7 to PE4) of port E.

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	PE7MD[2] to PE7MD[0]	000	PE7 mode 000: PE7 I/O (port)
11	—	0	Reserved
10 to 8	PE6MD[2] to PE6MD[0]	001	PE6 mode 001: TIOC2A I/O (MTU)
7	—	0	Reserved
6 to 4	PE5MD[2] to PE5MD[0]	000	PE5 mode 000: PE5 I/O (port)
3	—	0	Reserved
2 to 0	PE4MD[2] to PE4MD[0]	000	PE4 mode 000: PE4 I/O (port)

- Port E Control Register L1 (PECRL1)
  - Setting value: H'0000
  - Function: Selects functions of the multiplexed pins (PE3 to PE0) of port E.

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	PE3MD[2] to PE3MD[0]	000	PE3 mode 000: PE3 I/O (port)
11	—	0	Reserved
10 to 8	PE2MD[2] to PE2MD[0]	000	PE2 mode 000: PE2 I/O (port)
7	—	0	Reserved
6 to 4	PE1MD[2] to PE1MD[0]	000	PE1 mode 000: PE1 I/O (port)
3, 2	—	00	Reserved
1, 0	PE0MD[1] and PE0MD[0]	00	PE0 mode 00: PE0 I/O (port)

- Port E I/O Register L (PEIORL)
  - Setting value: H'0000
  - Function: Selects the signal directions on the port E pins (PE15 to PE0).
    1: output, 0: input

Bit	Bit Name	Value	Description
15	PE15IOR	0	The PE15 pin is set as input.
14	PE14IOR	0	The PE14 pin is set as input.
13	PE13IOR	0	The PE13 pin is set as input.
12	PE12IOR	0	The PE12 pin is set as input.
11	PE11IOR	0	The PE11 pin is set as input.
10	PE10IOR	0	The PE10 pin is set as input.
9	PE9IOR	0	The PE9 pin is set as input.
8	PE8IOR	0	The PE8 pin is set as input.
7	PE7IOR	0	The PE7 pin is set as input.
6	PE6IOR	0	The PE6/TIOC2A pin is set as input.
5	PE5IOR	0	The PE5 pin is set as input.
4	PE4IOR	0	The PE4 pin is set as input.
3	PE3IOR	0	The PE3 pin is set as input.
2	PE2IOR	0	The PE2 pin is set as input.
1	PE1IOR	0	The PE1 pin is set as input.
0	PE0IOR	0	The PE0 pin is set as input.

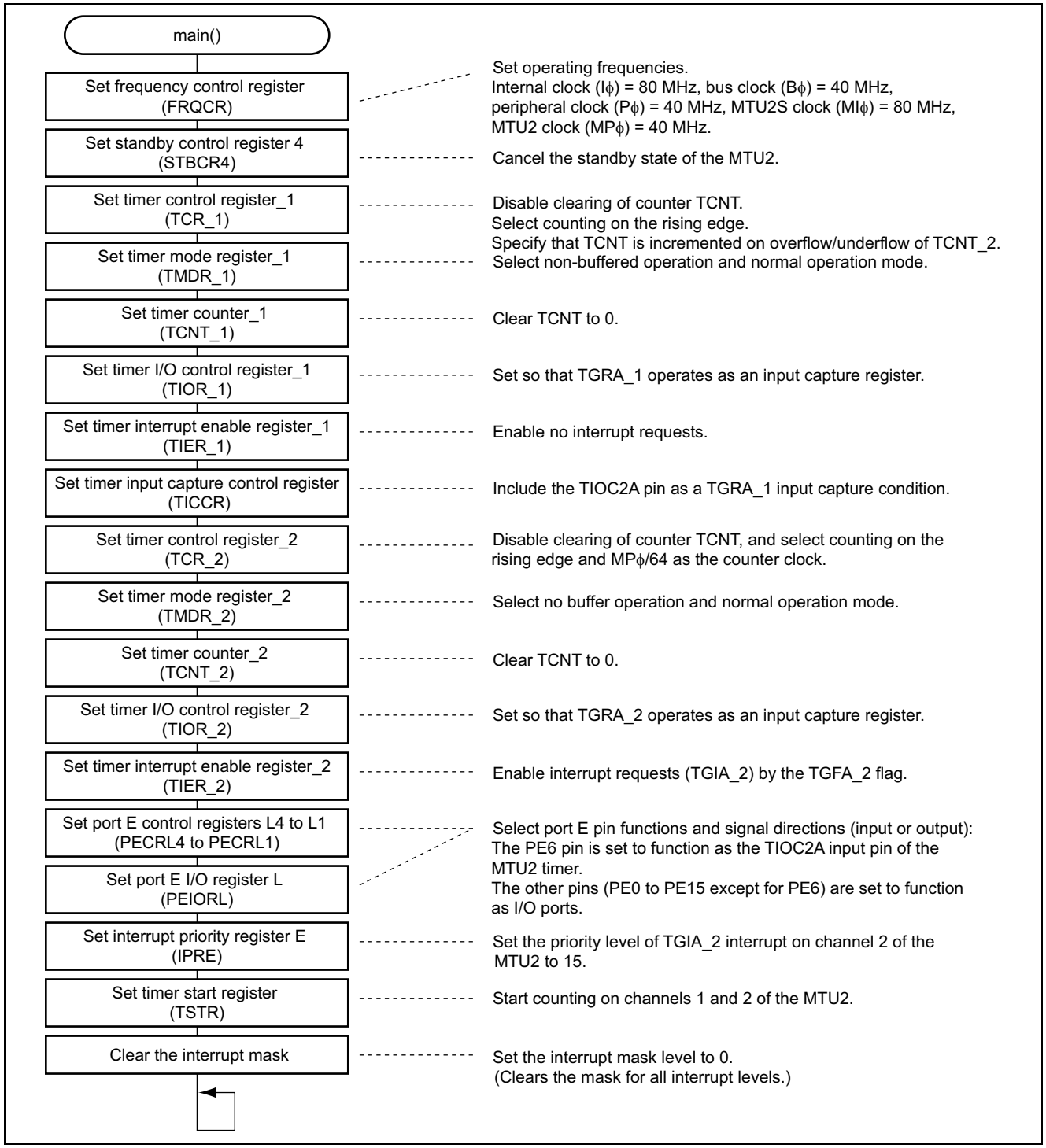
5.3.7 Settings for Interrupt Controller (INTC)

- Interrupt Priority Register E (IPRE)
  - Setting value: H'f000
  - Function: Sets priority levels of the corresponding interrupt requests.

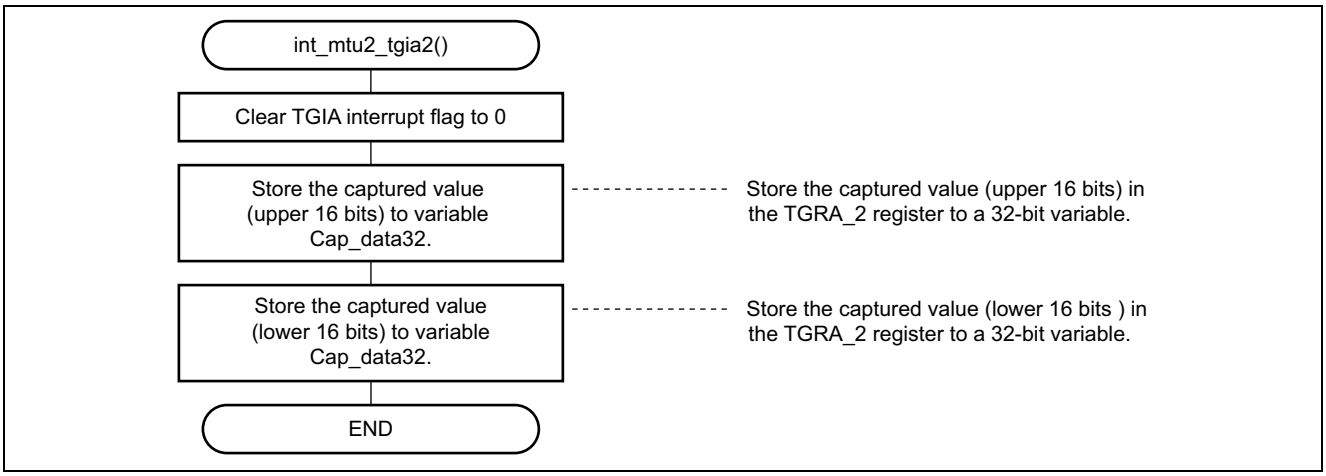
Bit	Bit Name	Value	Description
15 to 12	IPR[15] to IPR[12]	1111	Priority level 15 is set for the TGIA_2 (TGIB_2) interrupt on channel 2 of the MTU2.
11 to 8	IPR[11] to IPR[8]	0000	Priority level 0 is set for the corresponding interrupts.
7 to 4	IPR[7] to IPR[4]	0000	Priority level 0 is set for the corresponding interrupts.
3 to 0	IPR[3] to IPR[0]	0000	Priority level 0 is set for the corresponding interrupts.

6. Flowcharts

6.1 Main Routine



6.2 TGRA_2 Input Capture Interrupt Routine



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		Description	
Rev.	Date	Page	Summary
1.00	Sep.05.05	—	First edition issued

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