IGBT

Tj estimation method

About this document

This document will discuss the method used for IGBT Tj estimation calculation method.

Target Device

IGBT

Contents

1. Introduction

IGBT power modules have evolved as reliable and useful electronic parts due to the increasing relevance of power inverters in power infrastructure, reliability enhancement, and long-life operation. Excessive temperature stresses caused by excessive power losses frequently cause high-power-density IGBT modules to fail. It has been observed that the failure rate of IGBT modules rises as the junction temperature increases. Effective temperature control and thermal management are key strategies to reduce this failure rate. As a result, module temperature monitoring techniques are critical in designing and selecting IGBT modules for high-power-density applications to guarantee that temperature stresses in the various module components remain within the rated values.

2. Power Loss Calculation

This section describes the procedure for calculating the channel temperature Tch from the operating waveform and the device case temperature Tc. The channel temperature Tch calculated here is an estimated value.

2.1 Operation Loss

When driving an inductive load with an IGBT, the loss is largely divided into conduction loss and switching loss. The loss occurring when the IGBT is fully turned on is referred to as conduction loss, and the loss occurring while switching from ON to OFF or OFF to ON is called switching loss. Since loss is determined by integration of voltage and current as shown in the following expression, loss occurs due to the influence of collector-emitter saturation voltage VCE (sat) even in conduction. VCE (sat) must be low, as the loss leads to heat generation in the device. Switching loss is explained in detail in the next section.

Loss (P) = voltage (V) × current (I)

Turn-on loss: P(turn ON) = VCE(sat) × IC

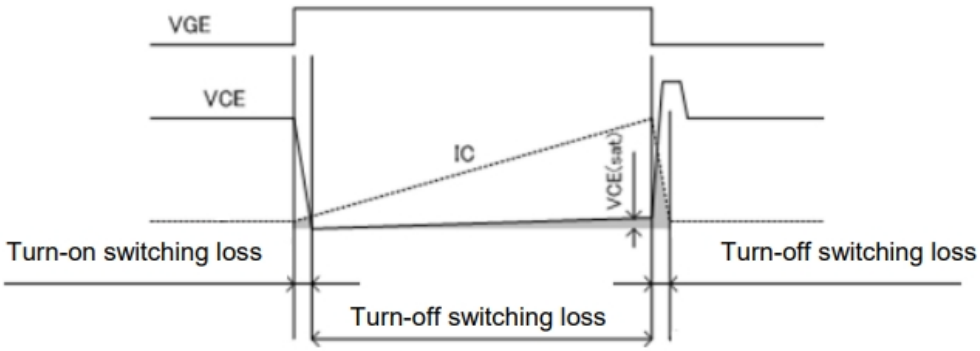

Figure 2-1 Operating Loss: inductive load drive example

2.2 Switching Loss

As IGBT loss is difficult to calculate using switching time, reference data is included in the data sheet to help system designers calculate switching loss. The switching loss characteristics for IGBT are shown in individual product datasheet. Eon and Eoff are highly dependent on collector current, gate resistance, and operating temperature.

- Eon (Turn-on energy loss)
  The amount of loss generated at turn-on under the inductive load conditions, including the recovery loss at reverse recovery of the diode. Eon is measured from when the gate voltage is applied and the collector current starts to flow, until the IGBT completely shifts to the ON state.
- Eoff (Turn-off energy loss)
  The amount of loss generated at turn-off under the inductive load conditions, including the tail current. Eoff is measured from when the gate current is cut off and the collector-emitter voltage starts to rise, until the IGBT completely shifts to the OFF state

3. Tj Estimation Method

3.1 Estimation of Tj using datasheet

Figure 3-1 shows the transient thermal resistance characteristics (from datasheet) of the IGBT and built-in diode of RBN40H65T1FPQ-A0.

This is a characteristic for calculating junction temperature Tj. The pulse width (PW) on the horizontal axis is the operation time, describing the 1 shot single pulse and the conditions of repeated operation. For example, PW = 1ms and D = 0.2 (duty cycle = 20%) means that the repetition frequency is 200Hz because the repetition period is T = 5ms.

Assuming PW-1ms and D = 0.2, using dissipation power Pd=60W, the increase in IGBT junction temperature ΔTj can be calculated as follows:

$$\Delta Tj = Pd \times \theta j\text{-}c(t) = 60 \times 0.4 = 24\ °C$$

$$Tj = Pd \times \theta j\text{-}c(t) + Tc$$

$$= 24 + 25 = 49\ °C$$

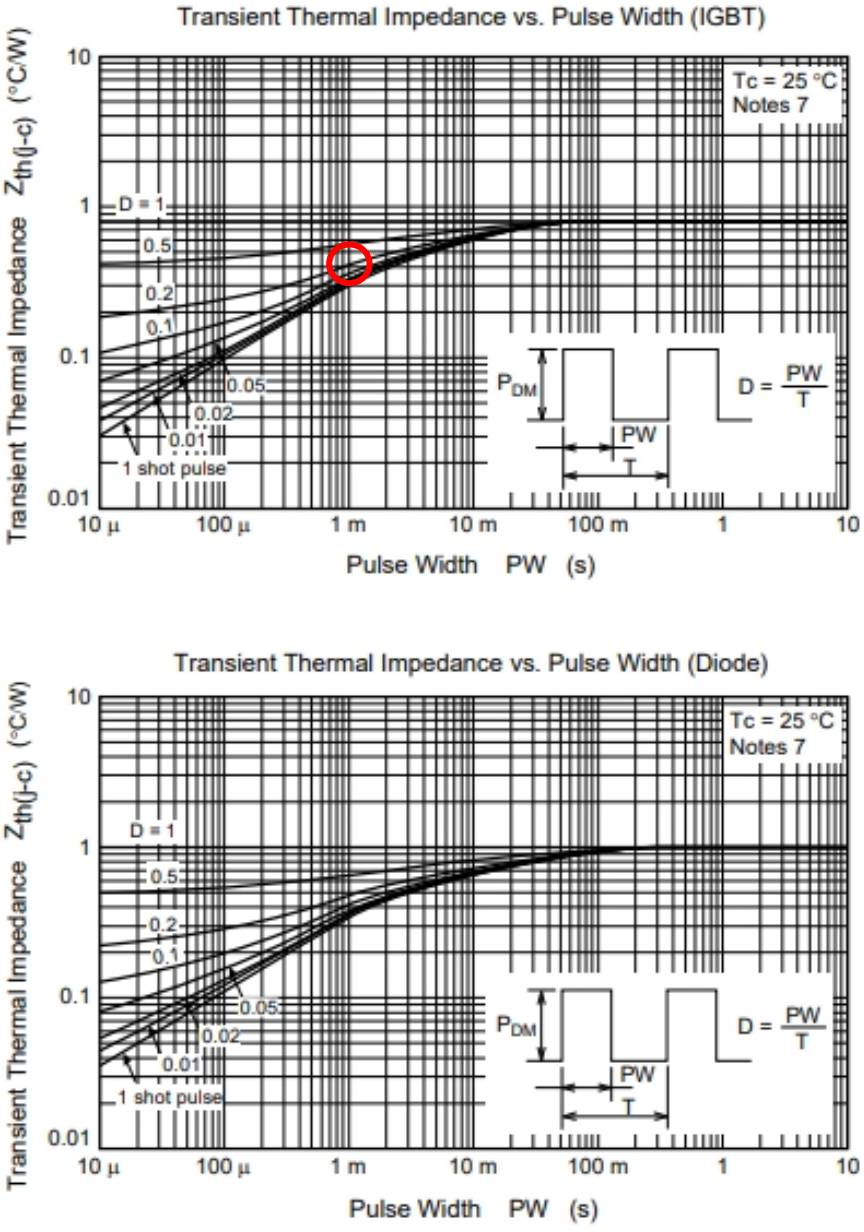

Figure 3-1 Transient Thermal Impedance vs. Pulse Width

3.2 Estimation of Tj using waveform analysis

For this estimation RBN40H65T1FPQ-A0 is used as an example. However, we can estimate this curve based on the conditions we specify (e.g., rectangular wave with 50% duty cycle). It's important to note that the actual waveform depends on the specific application, circuit, and other factors. Additionally, the Ic – fsw is derived from the Tj rating. Therefore, estimating the junction temperature (Tj) from the waveform is preferable to relying solely on the Ic – fsw curve. We can estimate the peak Tj using the method outlined in the next sections. Please review whether this approach is helpful for your consideration. This method involves some approximations and serves as a rough estimation for the first stage of design. It is highly recommended to evaluate our products with an actual circuit board. After performing the evaluation, we can estimate the Tj using the actual waveform measured on the board, if needed.

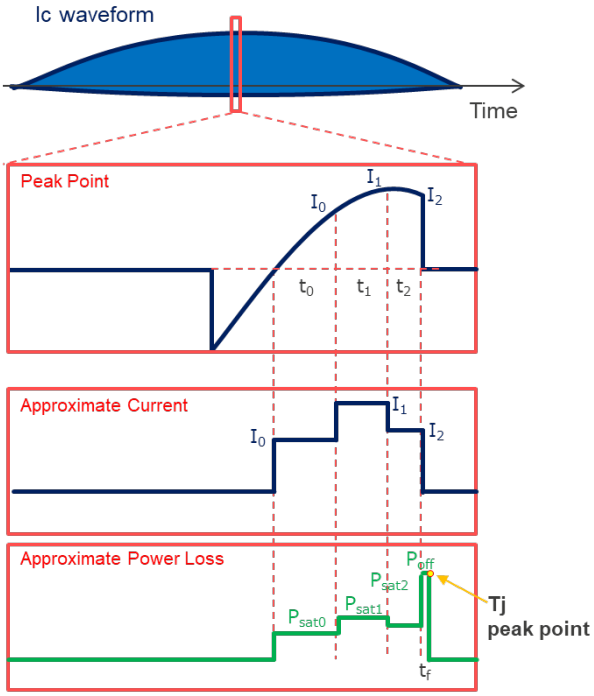

Figure 3-2 Estimation from the IC Waveform

To make the estimation easier, approximate the current wave to rectangle form [*1].

- ✓ Make the Power Loss Wave form.

  $P_{satx} = I_x \times Vce(sat)(150℃, I_x) \times 1.33$ [*2]

  $P_{off} = Eoff(150℃, I_2) \div t_f$

- ✓ Calculate average loss of whole waveform.

  Saturation Loss; $P_{sat\_total}(W) = fsw \times (\Sigma P_{satx} \times t_x) \times 0.7$ [*3]

  Switching Loss; $P_{off\_total}(W) = fsw \times Eoff \times 0.7$ [*3]

  Total Average Loss ; $P_{total}(W) = P_{sat\_total} + P_{off\_total}$

Estimate Tj peak

$$Tj\ peak = Tc\ [*4] + P_{off} \times Zth(t_f) + P_{sat2} \times (Zth(t_f + t_2) - Zth(t_f)) + P_{sat1} \times (Zth(t_f + t_2 + t_1) - Zth(t_f + t_2)) + P_{sat0} \times (Zth(t_f + t_2 + t_1 + t_0) - Zth(t_f + t_2 + t_1)) + Ptotal * (Zth(\infty) - Zth(t_f + t_2 + t_1 + t_0))$$

Notes: 1. FRD current is not considered because our product has IGBT and FRD's chip separately. FRD has very low power loss and is not needed to estimate FRD Tj.
2. This coefficient (1.33) came from Vce (sat) value (25℃); Max. (2.0V)/Typ. (1.5V).
3. This coefficient (0.7) means RMS of sine wave to estimate average loss from peak value.
4. We use 125℃ for Tc in this time but Tc is not equal with Temperature of Collector Pin, Tc depends on thermal design and higher than collector pin usually.
5. We use datasheet value for Vce(sat), Eoff, tr and Zth. Especially Eoff is fully influenced by actual circuit parameters (driver, parasitic inductance/capacitance etc.).

3.3 Key Point of Thermal Calculation

Any combination of power blocks can be calculated using the formula from the previous section.

$$\Delta Tj = \theta j\text{-}c(t0) \times P0 + \{\theta j\text{-}c(t1) - \theta j\text{-}c(t0)\} \times P1 + \{\theta j\text{-}c(t2) - \theta j\text{-}c(t1)\} \times P2 + \{\theta j\text{-}c(t3) - \theta j\text{-}c(t2)\} \times P3 + \{\theta j\text{-}c(\infty) - \theta j\text{-}c(t3)\} \times P4$$

The calculation will be more complex if there are few blocks involved, because every thermal impedance value needs to be read from the datasheet for all number of blocks as shown in Figure 3-3 and Figure 3-4.

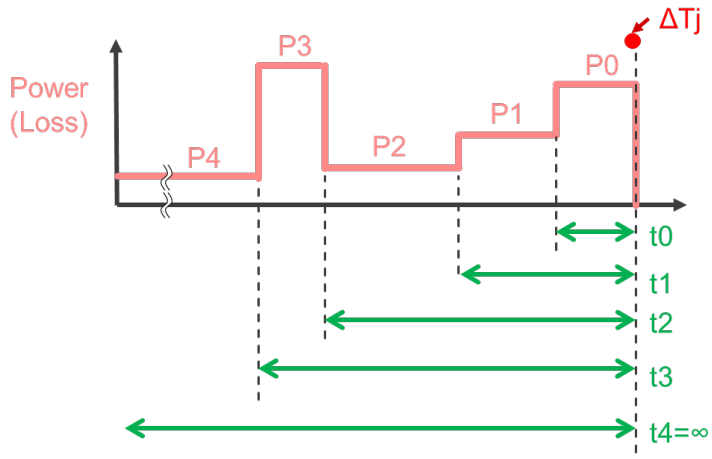

Figure 3-3 Combination of power block

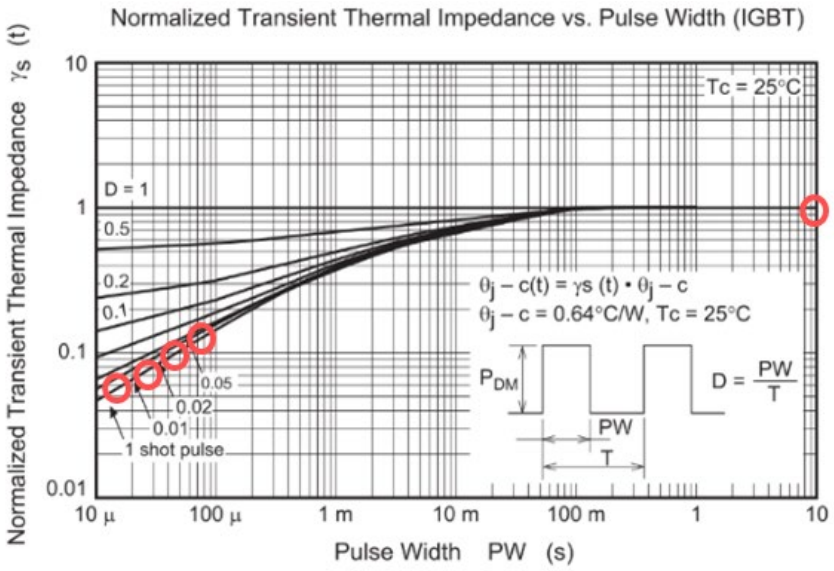

Figure 3-4 Thermal impedance value estimation

To make it simple as possible, the waveform on the upper left,

$$\Delta Tj = \left(\theta j\text{-}c(PW+\Delta PW) - \theta j\text{-}c(PW) \right) \times P$$

If PW ≫ ΔPW (time derivative),

$$\theta j\text{-}c(PW+\Delta PW) \fallingdotseq \theta j\text{-}c(PW) + \theta' j\text{-}c(PW) \times \Delta PW$$

Then the result is:

$$\Delta Tj \fallingdotseq \theta' j\text{-}c(PW) \times \Delta PW \times P$$

The same method can be done to the waveform on the bottom left,

$$\Delta Tj \fallingdotseq \theta' j\text{-}c(PW) \times (\Delta PW/2) \times (2 \times P)$$

Then the result is:

$$= \theta' j\text{-}c(PW) \times \Delta PW \times P$$

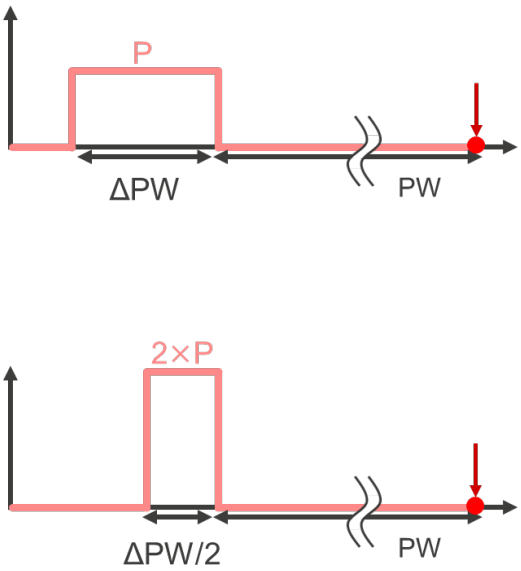

Figure 3-5 Simple estimation of individual waveform

The results achieved for both waveforms are the same individually. Therefore overall, a few blocks of waveform can be illustrated as average value as shown in Figure 3-6

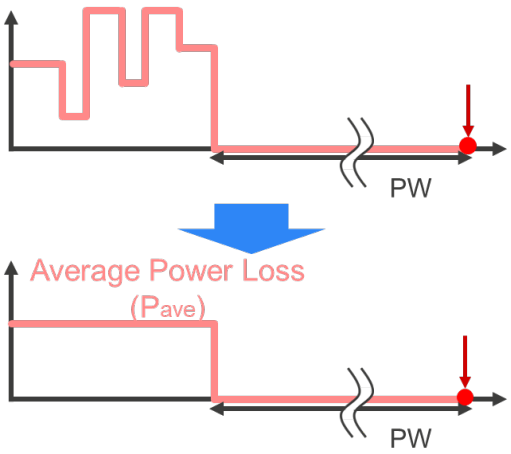

Figure 3-6 Average power loss (Pave)

As a result, the combination of a few blocks with average power loss waveform on the point which far away from the temperature to be measured is acceptable.

As example in Figure 3-7 below shows the rough block of the point which is far away. Eventually, the rough block is the average power of one cycle.

It becomes an error when roughing the near block. From how long and to how rough, it can be decided to depend on calculation work and required accuracy.

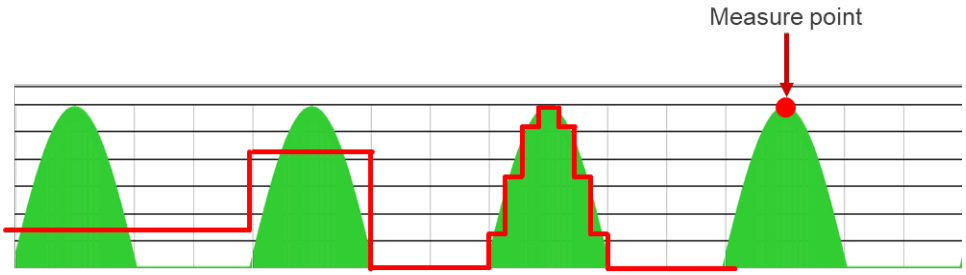

Figure 3-7 Block of point which far away from measured point

4. Result

Tj estimation using waveforms was done by requested few conditions (Scenario1 ~ Senario4) and results of calculation can be referred to below Table 4-1.

In this result, Tj of RBN40H65T1FPQ-A0 will be under rating of 175℃.

Table 4-1 Thermal Estimation Result

	Symbol	Scenario1	Scenario2	Scenario3	Scenario4	Unit
Conduction Loss	Psat0	13.30	27.13	20.83	18.15	W
	Psat1	68.10	49.88	24.26	28.25	W
	Psat2	5.32	21.95	14.52	25.08	W
Switching Loss	tf	0.1	0.08	0.085	0.075	us
	Eoff	0.21	0.4	0.32	0.45	mJ
	Poff	2100	5000	3764.7	6000	W
Frequency	Tsw	20	18.18	15.4	16.67	us
	fsw	50	55.01	64.94	59.99	kHz
Total Loss	Ptotal	18.83	25.00	19.66	25.01	W
Temperature Rise	⊿T	22.40	35.25	27.46	37.62	℃
Case Temperature	Tc	125	125	125	125	℃
Result	Tj	**147.40**	**160.25**	**152.46**	**162.62**	℃

The detailed approximation for each scenario of thermal estimation is shown below.

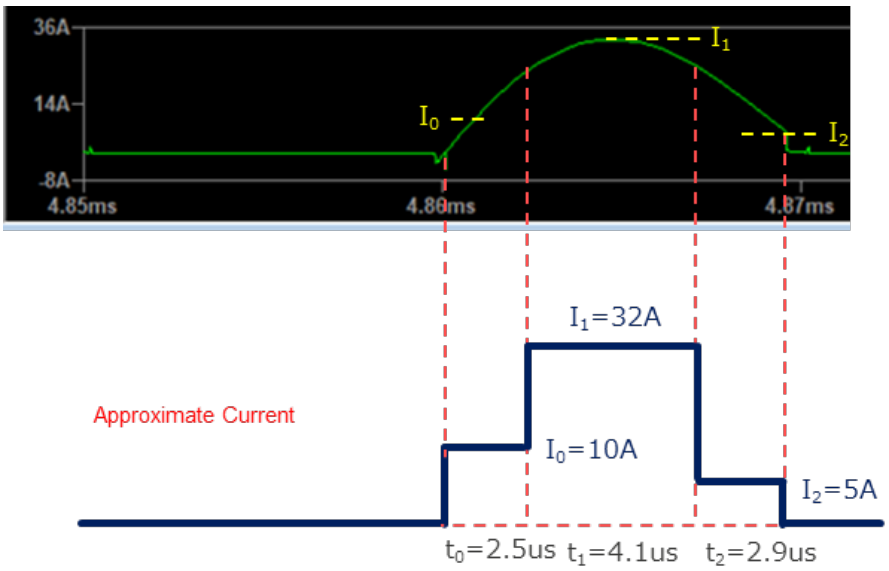

Figure 4-1 Scenario1 of 1600W

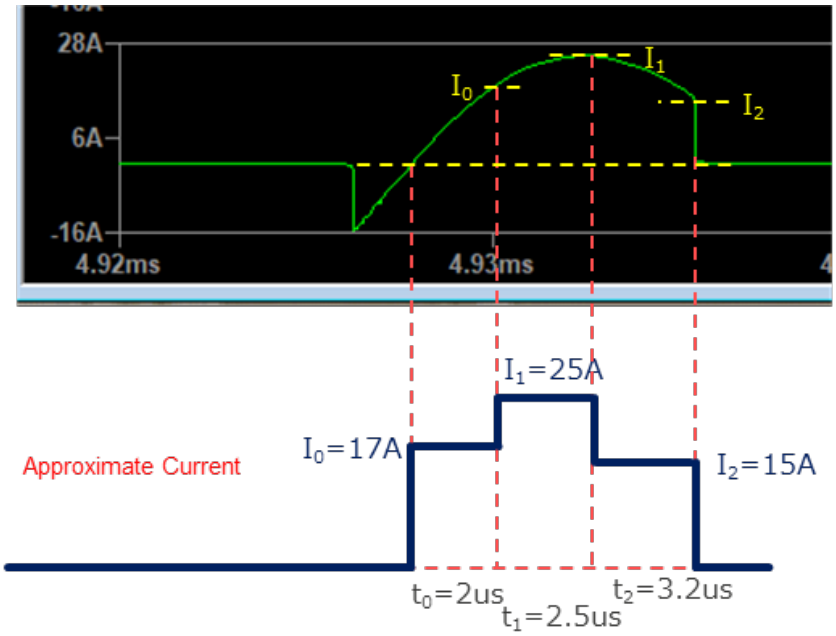

Figure 4-2 Scenario2 of 1200W

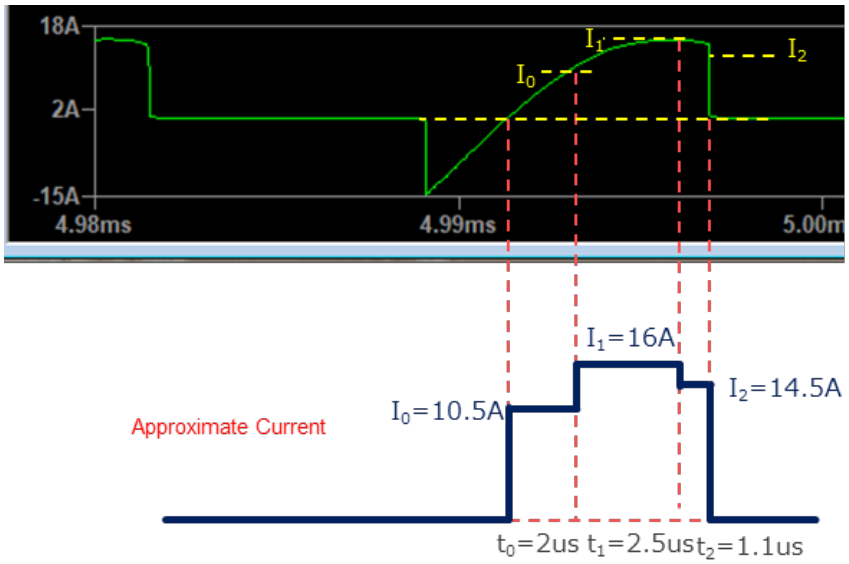

Figure 4-3 Scenario3 of 700W

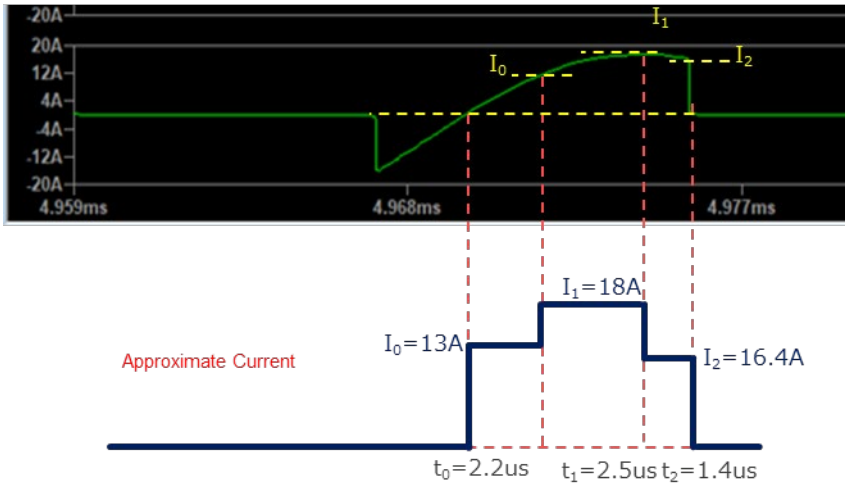

Figure 4-4 Scenario4 of 400W

5. Conclusion

With the proposal of the above simplified method application engineers can perform Tj estimation as alternative way comparing to other complex calculations. This is rough estimation by using several assumptions. Renesas would recommend to customers to refer it as a reference and evaluate under the actual system environment.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec.26.2024	-	First edition

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