How to Meet 112G PAM-4 SerDes Jitter Requirements with FemtoClock™ 3 and FemtoClock 3 Wireless Devices

Introduction

The FemtoClock 3 (FC3) and FemtoClock 3 Wireless (FC3W) families of devices are ultra-high performance clock generators, jitter cleaners, and clock synchronizers that can generate outputs with < 60fs of RMS jitter to be used as reference clocks for 112G PAM-4 SerDes. FC3 and FC3W generated outputs have low phase noise capable of meeting the 112G PAM-4 SerDes phase noise requirements at 10kHz, 100kHz, 1MHz, and > 10MHz with several dBc/Hz of margin.

Contents

Tables

1. Overview

The FC3 and FC3W families of devices are ultra-high performance clock generators, jitter cleaners, and clock synchronizers. The RC32xxx and RC38xxx series have advanced reference clock selection and hitless switching features to meet the stringent ITU-T requirements of communications infrastructure applications. The ultra-low jitter performance of these devices minimizes bit error rates (BER) in applications involving high-speed serial links, such as 112G PAM-4 SerDes.

The FC3 family of devices feature a single-channel synchronizer that can synchronize to one of four differential or single-ended reference clock inputs. Similarly, the FC3W family of devices feature up to three single-channel synchronizers that can synchronize to one of four differential clock inputs. The synchronizer is accompanied by an Analog Phase Locked-Loop (APLL) domain that features Renesas' new generation, ultra-low phase noise VCO, and generates < 60fs rms typical jitter in the frequency band of 12kHz to 20MHz for a 312.5MHz output; both of which exceed the 112G PAM-4 reference clock needs as specified in the standards and for the switch ASICs.

There are additional FOD domains that can be used to generate unrelated frequencies either locked to the reference clock input or the free-run XO input and generates < 120fs rms typical jitter. FC3 and FC3W can generate up to 12 high-performance output clocks with up to four different frequencies.

2. 112G Reference Clock Requirements

The overall allowable jitter in a serial link is dictated by the applicable standard, such as IEEE or OIF. Table 1 displays the maximum allowable transmitter output jitter for various serial link interfaces. The maximum allowable values are obtained from the applicable standards in terms of UI, where 1 UI is equal to the period of the baud rate. The equivalent time domain jitter has been calculated for each interface in Table 1. For example, IEEE 802.3df (800GAUI-8) has a maximum allowable transmitter output jitter of 0.023 × UI and uses a baud rate of 53.125Gbd. One period of the baud rate is therefore equal to $1/(53.125 \times 10^9)$ = 18.8235ps. Therefore, the maximum allowable jitter is 0.023 × 18.8235ps = 433fs (rounded to nearest fs). Only a portion of the overall allowable jitter is allocated to the reference clock. Many SerDes ASIC vendors with 112G PAM4 SerDes require a maximum reference clock jitter of 100fs RMS.

Table 2 displays the phase noise requirements for a 112G receiver.

Table 2 also contains the 112G PAM-4 reference clock Gaussian jitter requirement. The Gaussian jitter, also known as random jitter requirement for a 112G PAM-4 reference clock, is defined as 0.009 × UI (RMS), where 1 UI is equal to the period of the reference clock. For a 312.5MHz reference clock, 1 UI = 1/(312.5 × 10E6) = 3.2ns. The random jitter requirement is therefore 0.009 × 3.2ns = 28.8ps.

For a gaussian distribution, it is possible to predict the peak-to-peak random jitter (RJ_{PP}) using the measured random RMS jitter (RJ_{rms}) and an RMS multiplier (N), where $RJ_{PP} = N * RJ_{rms}$. The RMS multiplier is determined using the required bit error rate (BER) and data transition density (DTD). Table 3 shows the RMS multiplier for bit error rates of 10^{-3} to 10^{-15} for DTD = 0.5 and DTD = 1.

Table 1. Maximum Allowable Transmitter Output Jitter for Various Serial Link Interfaces

Interface	Baud Rate	Maximum Allowable Transmitter Output Jitter	Description
CEI-112G-XSR-PAM4	Between 36Gsym/s and 58Gsym/s	0.0224*UI [1] (RMS) = 622fs for 36Gsym/s = 386fs for 58Gsym/s	From OIF-CEI-05.1, section 24 “CEI-112G-XSR-PAM4 Extra Short Reach Interface”
CEI-112G-MR-PAM4		0.023 × 5 UI (RMS) = 638fs for 36Gsym/s = 396fs for 58Gsym/s	From OIF-CEI-05.1, section 26 “CEI-112G-MR-PAM4 Medium Reach Interface” and section 27 “CEI-112G-LR-PAM4 Long Reach Interface”
CEI-112G-LR-PAM4			
IEEE 802.3ck	25.78125 or 26.5625 GBd	0.023*UI (RMS) = 892fs for 25.78125 GBd, = 866fs for 26.5625 GBd, = 433fs for 53.125 GBd	From IEEE Std 802.3ck™-2022, IEEE Std 802.3cu™-2021, IEEE P802.3df™/D2.0
IEEE 802.3cu	26.5625 or 53.125 GBd		
IEEE 802.3df (800GAUI-8)	53.125 GBd		

Table 2. 112G Reference Clock Requirements

Interface	Reference Clock	Description
High Frequency Uncorrelated Unbounded Gaussian Jitter	0.009*UI (RMS) = 28.8ps for 312.5MHz	The reference clock is typically set to be 1/64th of the baud rate. However, most 112G SerDes or Switch ASICs use 312.5 MHz for a reference clock.
Single Side Band (SSB) Phase Noise	-131 dBc/Hz	At 10kHz offset
	-137 dBc/Hz	At 100kHz offset
	-143 dBc/Hz	At 1MHz offset
	-158 dBc/Hz	At >10MHz offset

1. 1 Ui is equal to the period of the baud rate.

Table 3. RMS Multipliers for Bit Error Rates of 10^{-3} to 10^{-15}

BER	RMS Multiplier (N), DTD = 0.5	RMS Multiplier (N), DTD = 1
10^{-3}	6.180	6.582
10^{-4}	7.438	7.782
10^{-5}	8.530	8.834
10^{-6}	9.507	9.784
10^{-7}	10.399	10.654
10^{-8}	11.224	11.462
10^{-9}	11.996	12.218
10^{-10}	12.723	1.934
10^{-11}	13.412	13.614
10^{-12}	14.069	14.260
10^{-13}	14.698	14.882
10^{-14}	15.301	15.478
10^{-15}	15.883	16.028

3. Meeting 112G Reference Clock Requirements with FC3

For a 312.5MHz SerDes reference clock, Renesas recommends using of a 62.5MHz crystal along with an APLL VCO frequency of 10GHz to attain the best jitter and phase noise when using FC3 in synthesizer mode. When using FC3 in jitter attenuator mode to generate a 312.5MHz SerDes reference clock, Renesas recommends the use of a 49.152MHz crystal along with an APLL VCO frequency of 10GHz.

Figure 1 shows the phase noise plot for a 312.5MHz FC3 output with a crystal input frequency of 62.5MHz (synthesizer mode) measured using a Rohde & Schwarz FSWP. Figure 2 shows the phase noise plot for a 312.5MHz FC3 output with a crystal input frequency of 49.152MHz (jitter attenuator mode) and a reference input clock frequency of 25MHz. The RMS jitter value of a 312.5MHz output is approximately 56fs when using synthesizer mode with a 62.5MHz crystal, and approximately 66fs when using jitter attenuator mode with a 49.152MHz crystal. Therefore, the RMS jitter of FC3 is far below the typical maximum of 100fs used for many SerDes ASICs. Comparing Figure 1, Figure 2, Figure 3, and Figure 5 to Table 2, which displays the phase noise requirements for a 112G receiver, FC3 meets the requirements at 10kHz, 100kHz, 1MHz, and > 10MHz with several dBc/Hz of margin.

112G PAM-4 SerDes uses a CDR bandwidth of 4MHz, which acts as a high-pass filter on the reference clock. Depending on the method used to simulate this 4MHz high-pass filter, a 312.5MHz FC3 output clock will have RMS jitter of ~18fs to 21.5fs.

Using Table 3, for the case where BER = 10^{-15} and DTD = 1, which will yield the highest RMS multiplier of N = 16.028, and using RJ_{rms} = 65.464fs as shown in Figure 3, RJ_{PP} = 16.028 × 65.464fs = 1.049ps for synthesizer mode with a 62.5MHz crystal and a 312.5MHz output. For jitter attenuator mode with a 49.152MHz crystal, a 312.5MHz output has RJ_{rms} = 72.471fs, as shown in Figure 5. Thus, RJ_{PP} = 16.028 × 72.471fs = 1.161ps and the random jitter produced by a FC3W output is far below the recommended maximum of 28.8ps for a 312.5MHz SerDes reference clock.

Renesas primarily uses two phase noise measurement instruments, the Keysight E5052B and the Rohde & Schwarz FSWP. Each instrument simulates filters differently. The Keysight E5052B can simulate a 4MHz high pass filter by using its equation editor feature to apply a high-pass filter equation to the data trace. The Rohde & Schwarz can simulate a 4MHz high pass filter by using its weighting filter feature. For more details on how to set up these features, see the Applying Filters to Phase Noise Measurements with Keysight E5052 and Rohde & Schwarz FSWP application note.

3.1 FC3 With a 4MHz High Pass Filter Using the Rohde & Schwarz FSWP

Simulating a 4MHz high pass filter using the Rohde & Schwarz FSWP involves applying a weighting filter to integrated measurement. The weighting filter feature only has an effect on the integrated measurement results and has no effect in the noise diagram or other numerical results.

Figure 1. Phase Noise Plot for a 312.5MHz Output from an RC32312 FC3 Device Operating in Synthesizer Mode, using a 62.5MHz Crystal along with an APLL VCO Frequency of 10GHz, measured using a Rohde & Schwarz FSWP; RMS Jitter also displayed

Figure 2. Phase Noise Plot for a 312.5MHz Output from an RC32312 FC3 Device Operating in Jitter Attenuator Mode, using a 49.152MHz Crystal along with an APLL VCO Frequency of 10GHz, and a 25MHz + 1ppm Reference Input, measured using a Rohde & Schwarz FSWP; RMS Jitter also displayed

3.2 FC3 With a 4MHz High Pass Filter Using the Keysight E5052B

Simulating a 4MHz high pass filter using the Keysight E5052B involves applying a mathematical function to the measured data for an integration range of 12kHz to 20MHz.The mathematical function to apply to the data is as follows:

$$F(x) = data - 20\log_{10}\sqrt{1+\frac{F_c^2}{x^2}}$$

Equation 1. Function Used to Approximate a 4MHz High-Pass Filter For FC3

Where F_C is the corner frequency in Hz, which is equal to 4000000 in this case, and x is the offset frequency in Hz. Figure 4 shows the phase noise after applying Equation 1 to the data shown in Figure 3. Similarly, Figure 6 shows the phase noise after applying Equation 1 to the data shown in Figure 5. Using this method, the approximate RMS jitter on the receiver after the 4MHz high-pass filter will be ~20.4fs when using synthesizer mode with a 62.5MHz crystal, and ~21.5fs when using jitter attenuator mode with a 49.152MHz crystal.

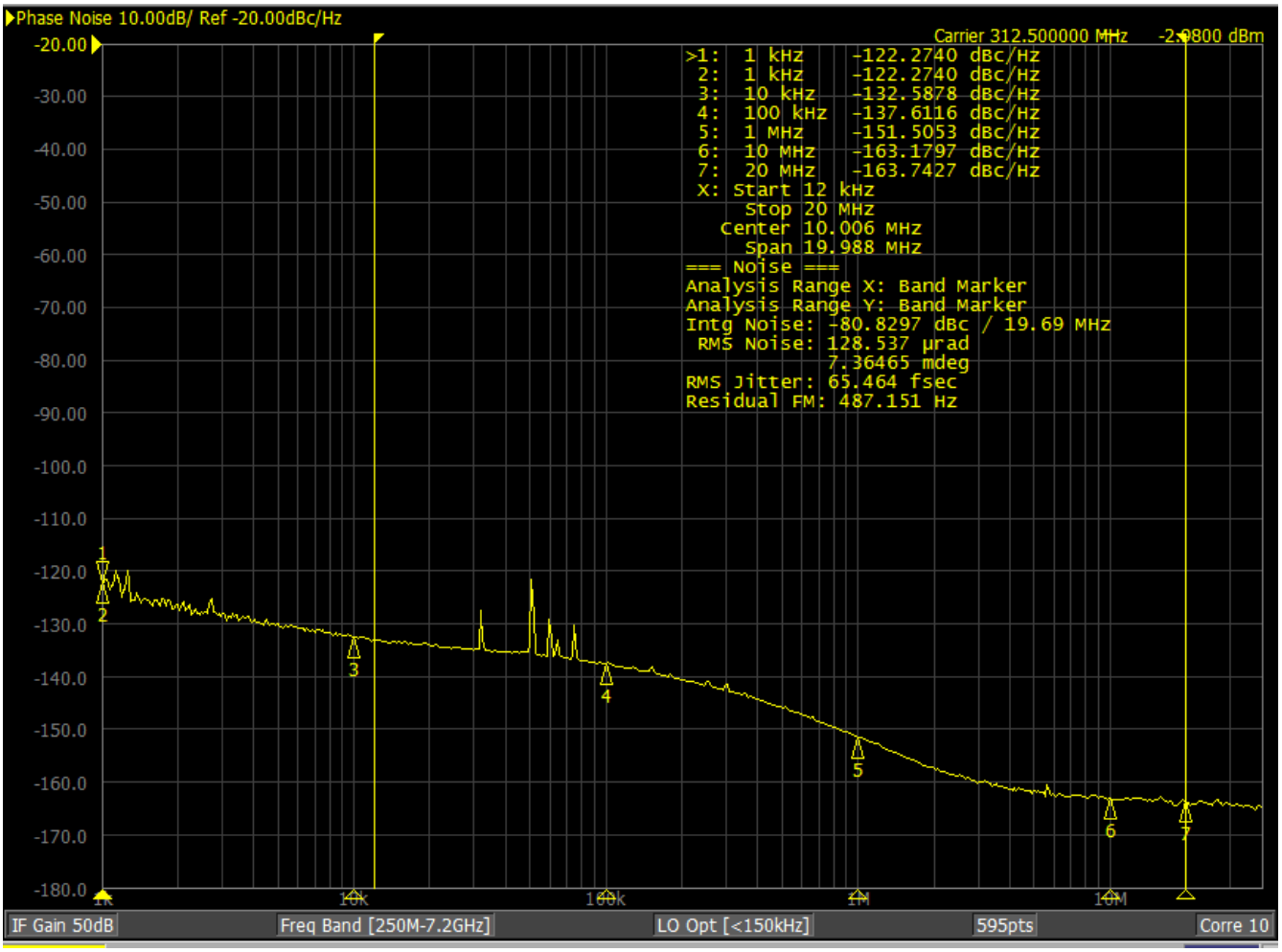


Figure 3. Phase Noise Plot for a 312.5MHz Output from an RC32312 FC3 Device Operating in Synthesizer Mode, using a 62.5MHz Crystal along with an APLL VCO Frequency of 10GHz; RMS Jitter also displayed

Figure 4. Phase Noise Plot with a 4MHz High-Pass Filter applied on a 312.5MHz Output from an RC32312 FC3 Device Operating in Synthesizer Mode using a 62.5MHz Crystal along with an APLL VCO Frequency of 10GHz; RMS Jitter also displayed

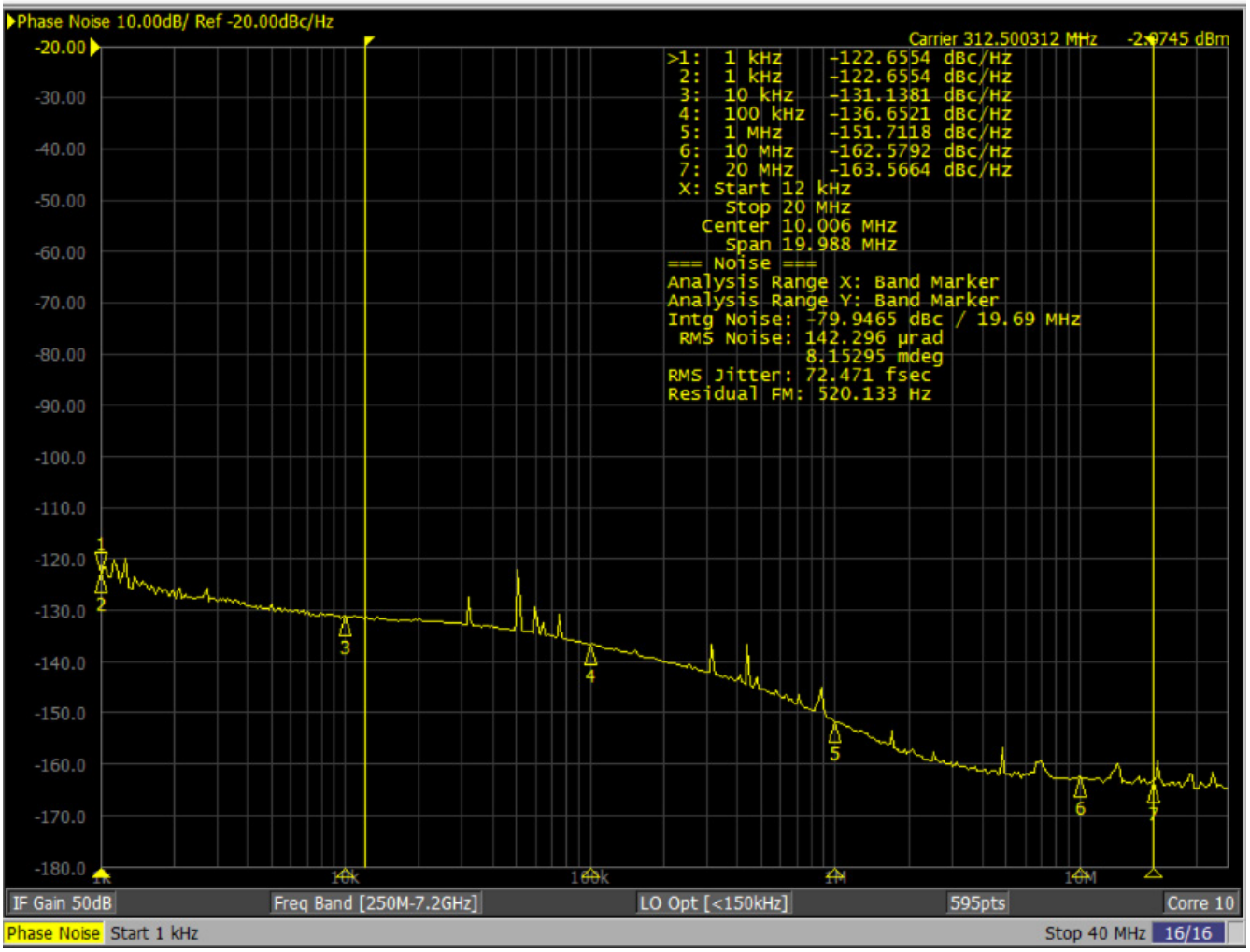


Figure 5. Phase Noise Plot for a 312.5MHz Output from an RC32312 FC3 Device Operating in Jitter Attenuator Mode, using a 49.152MHz Crystal along with an APLL VCO Frequency of 10GHz, and a 25MHz + 1ppm Reference Clock Input; RMS Jitter also displayed

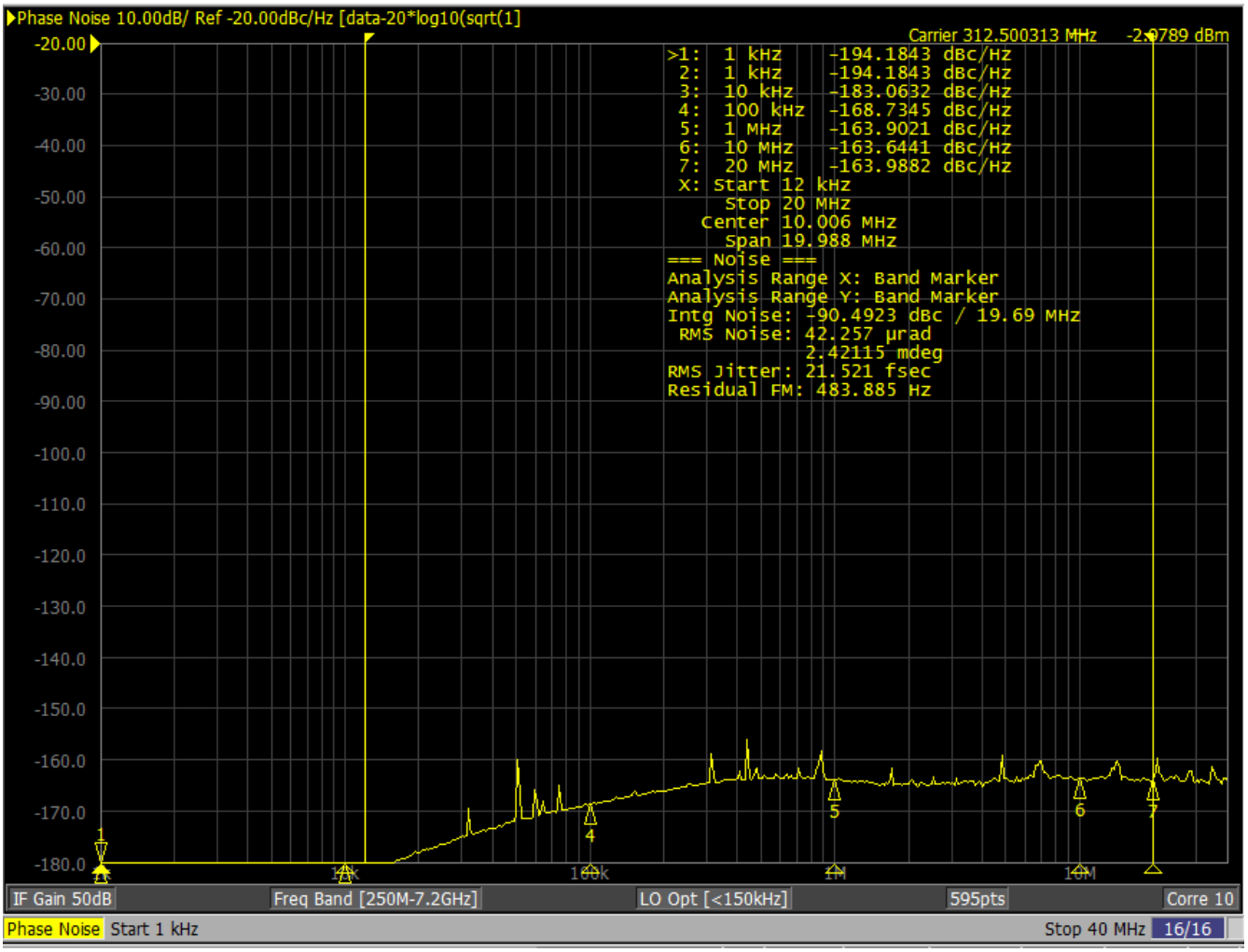


Figure 6. Phase Noise Plot with a 4MHz High Pass Filter applied on a 312.5MHz Output from an RC32312 FC3 Device Operating in Jitter Attenuator Mode using a 49.152MHz Crystal and a 25MHz Reference Clock Input; RMS Jitter also displayed

4. Meeting 112G Reference Clock Requirements with FC3W

For a 312.5MHz SerDes reference clock, Renesas recommends using of a 62.5MHz crystal along with an APLL VCO frequency of 9.375GHz to attain the best jitter and phase noise when using FC3W in synthesizer mode. When using FC3W in jitter attenuator mode to generate a 312.5MHz SerDes reference clock, Renesas recommends the use of a 49.152MHz, 54MHz, or 73MHz crystal along with an APLL VCO frequency of 9.375GHz. This document explores an example of using a 49.152MHz crystal for jitter attenuator mode.

Figure 7 shows the phase noise plot for a 312.5MHz FC3W output with a crystal input frequency of 62.5MHz (synthesizer mode) measured using a Rohde & Schwarz FSWP. Figure 8 shows the phase noise plot for a 312.5MHz FC3 output with a crystal input frequency of 54MHz (jitter attenuator mode) and a reference input clock frequency of 25MHz measured using a Rohde & Schwarz FSWP. The RMS jitter value of a 312.5MHz output is approximately 56.3fs when using synthesizer mode with a 62.5MHz crystal, and approximately 68.6fs when using jitter attenuator mode with a 49.152MHz crystal. Therefore, the RMS jitter of FC3W is far below the typical maximum of 100fs used for many SerDes ASICs. Comparing Figure 7, Figure 8, Figure 9, and Figure 11 to Table 2, which displays the phase noise requirements for a 112G receiver, FC3W meets the requirements at 10kHz, 100kHz, 1MHz, and > 10MHz.

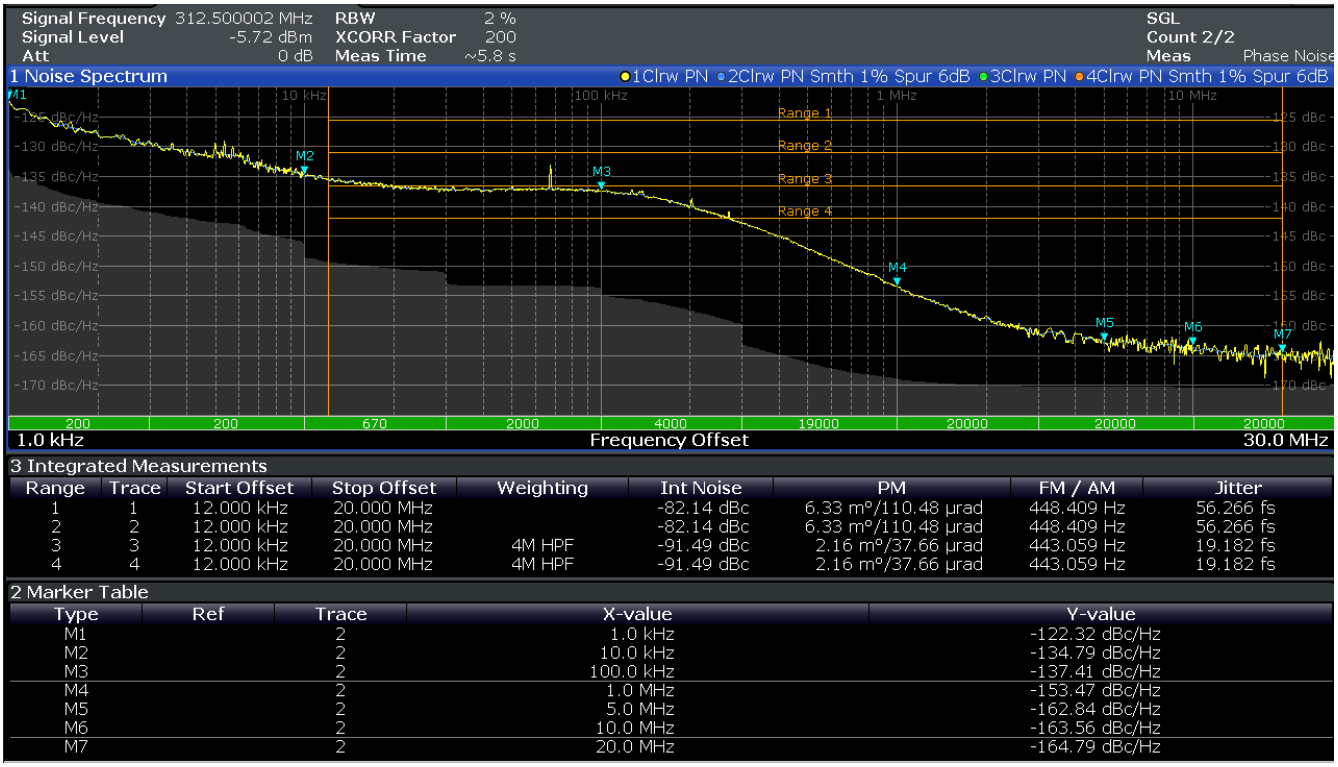
112G PAM-4 SerDes uses a CDR bandwidth of 4MHz, which acts as a high-pass filter on the reference clock. Depending on the method used to simulate this 4MHz high-pass filter, a 312.5MHz FC3W output clock will have RMS jitter of ~19.4fs to ~23.7fs.

Renesas primarily uses two phase noise measurement instruments, the Keysight E5052B and the Rohde & Schwarz FSWP. Each instrument simulates filters differently. The Keysight E5052B can simulate a 4MHz high-pass filter by using its equation editor feature to apply a high-pass filter equation to the data trace. The Rohde & Schwarz can simulate a 4MHz high-pass filter by using its weighting filter feature. For more details on how to set up these features, see the Applying Filters to Phase Noise Measurements with Keysight E5052 and Rohde & Schwarz FSWP application note.

Using Table 3 for the case where BER = 10^{-15} and DTD = 1, which will yield the highest RMS multiplier of N = 16.028, and using RJ_{rms} = 67.068fs as shown in Figure 9, RJ_{PP} = 16.028 × 67.068fs = 1.075ps for synthesizer mode with a 62.5MHz crystal and a 312.5MHz output. For jitter attenuator mode with a 49.152MHz crystal, a 312.5MHz output has RJ_{rms} = 77.065, as shown in Figure 11. Thus, RJ_{PP} = 16.028 × 77.065 = 1.235ps and the random jitter produced by a FC3W output is far below the recommended maximum of 28.8ps for a 312.5MHz SerDes reference clock.

4.1 FC3W With a 4MHz High Pass Filter Using the Rohde & Schwarz FSWP

Simulating a 4MHz high-pass filter using the Rohde & Schwarz FSWP involves applying a weighting filter to integrated measurement. The weighting filter feature only has an effect on the integrated measurement results and has no effect in the noise diagram or other numerical results.



3 Integrated Measurements

Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	12.000 kHz	20.000 MHz		-82.14 dBc	6.33 m°/110.48 µrad	448.409 Hz	56.266 fs
2	2	12.000 kHz	20.000 MHz		-82.14 dBc	6.33 m°/110.48 µrad	448.409 Hz	56.266 fs
3	3	12.000 kHz	20.000 MHz	4M HPF	-91.49 dBc	2.16 m°/37.66 µrad	443.059 Hz	19.182 fs
4	4	12.000 kHz	20.000 MHz	4M HPF	-91.49 dBc	2.16 m°/37.66 µrad	443.059 Hz	19.182 fs

2 Marker Table

Type	Ref	Trace	X-value	Y-value
M1		2	1.0 kHz	-122.32 dBc/Hz
M2		2	10.0 kHz	-134.79 dBc/Hz
M3		2	100.0 kHz	-137.41 dBc/Hz
M4		2	1.0 MHz	-153.47 dBc/Hz
M5		2	5.0 MHz	-162.84 dBc/Hz
M6		2	10.0 MHz	-163.56 dBc/Hz
M7		2	20.0 MHz	-164.79 dBc/Hz

Figure 7. Phase Noise Plot of a 312.5MHz Output from an RC38312 FC3W Device Operating in Synthesizer Mode using a 62.5MHz Crystal with an APLL VCO Frequency of 9.375GHz; measured using a Rohde & Schwarz FSWP. Range 1 and 2 show Unfiltered RMS Jitter. Range 3 and 4 show RMS Jitter with a 4MHz High-Pass Filter applied

Figure 8. Phase Noise Plot of a 312.5MHz Output from an RC38312 FC3W Device Operating in Jitter Attenuator Mode using a 49.152MHz Crystal with an APLL VCO Frequency of 9.375GHz and a 25MHz + 1ppm Reference Input; measured using a Rohde & Schwarz FSWP. Range 1 and 2 show Unfiltered RMS Jitter. Range 3 and 4 show RMS Jitter with a 4MHz High-Pass Filter applied

4.2 FC3W With a 4MHz High Pass Filter Using the Keysight E5052B

Simulating a 4MHz high-pass filter using the Keysight E5052B involves applying a mathematical function to the measured data for an integration range of 12kHz to 20MHz.The mathematical function to apply to the data is as follows:

$$F(x) = data - 20\log_{10}\sqrt{1+\frac{F_c^2}{x^2}}$$

Equation 2. Function Used to Approximate a 4MHz High-Pass Filter for FC3W

Where F_C is the corner frequency in Hz, which is equal to 4000000 in this case, and x is the offset frequency in Hz. Figure 10 shows the phase noise after applying Equation 2 to the data shown in Figure 9. Similarly, Figure 12 shows the phase noise after applying Equation 2 to the data shown in Figure 11. Using this method, the approximate RMS jitter on the receiver after the 4MHz high-pass filter will be ~23.4fs when using synthesizer mode with a 62.5MHz crystal, and ~23.7fs when using jitter attenuator mode with a 49.152MHz crystal.

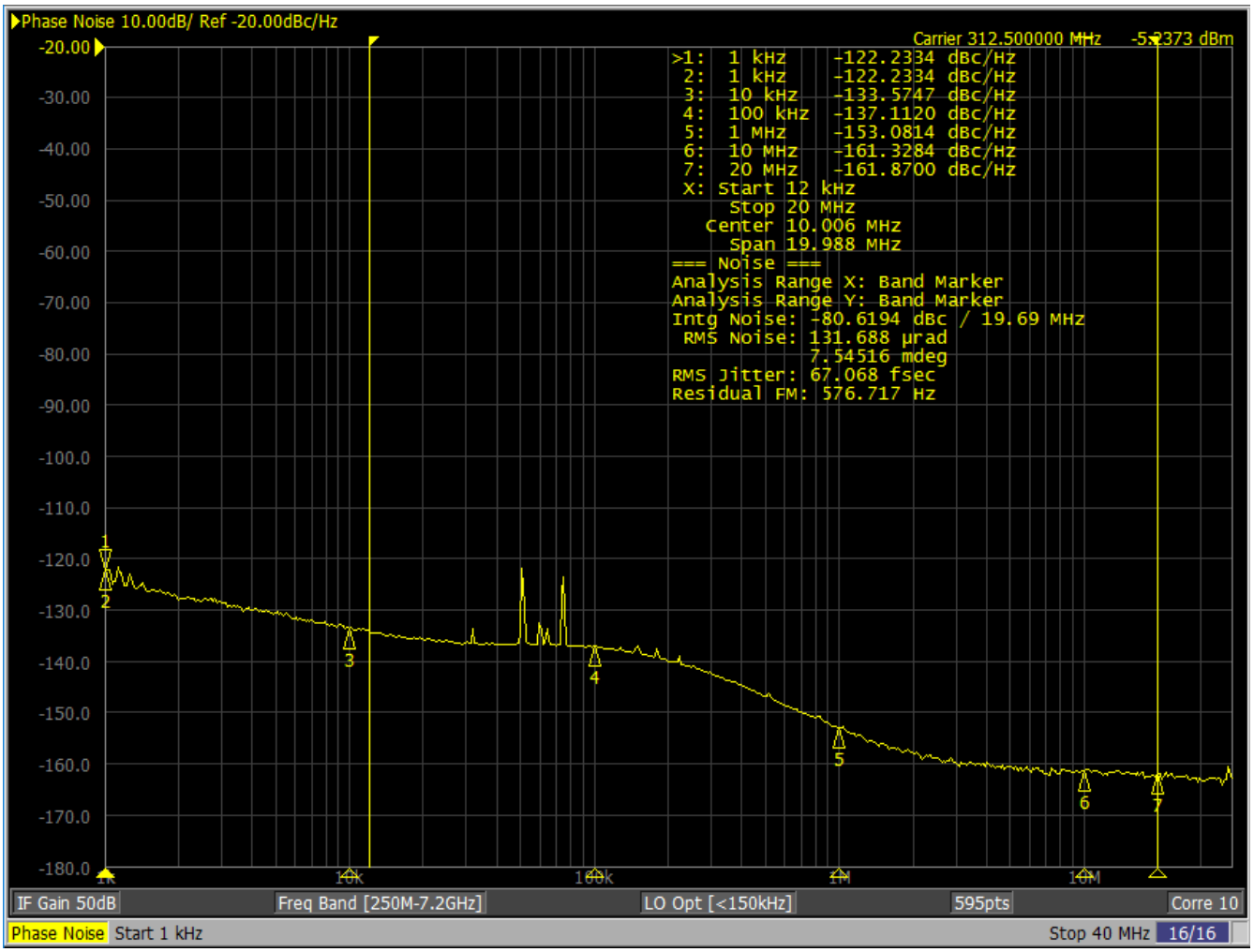


Figure 9. Phase Noise Plot for a 312.5MHz Output from an RC38312 FC3W Device Operating in Synthesizer Mode using a 62.5MHz Crystal with an APLL VCO Frequency of 9.375GHz; RMS Jitter also displayed

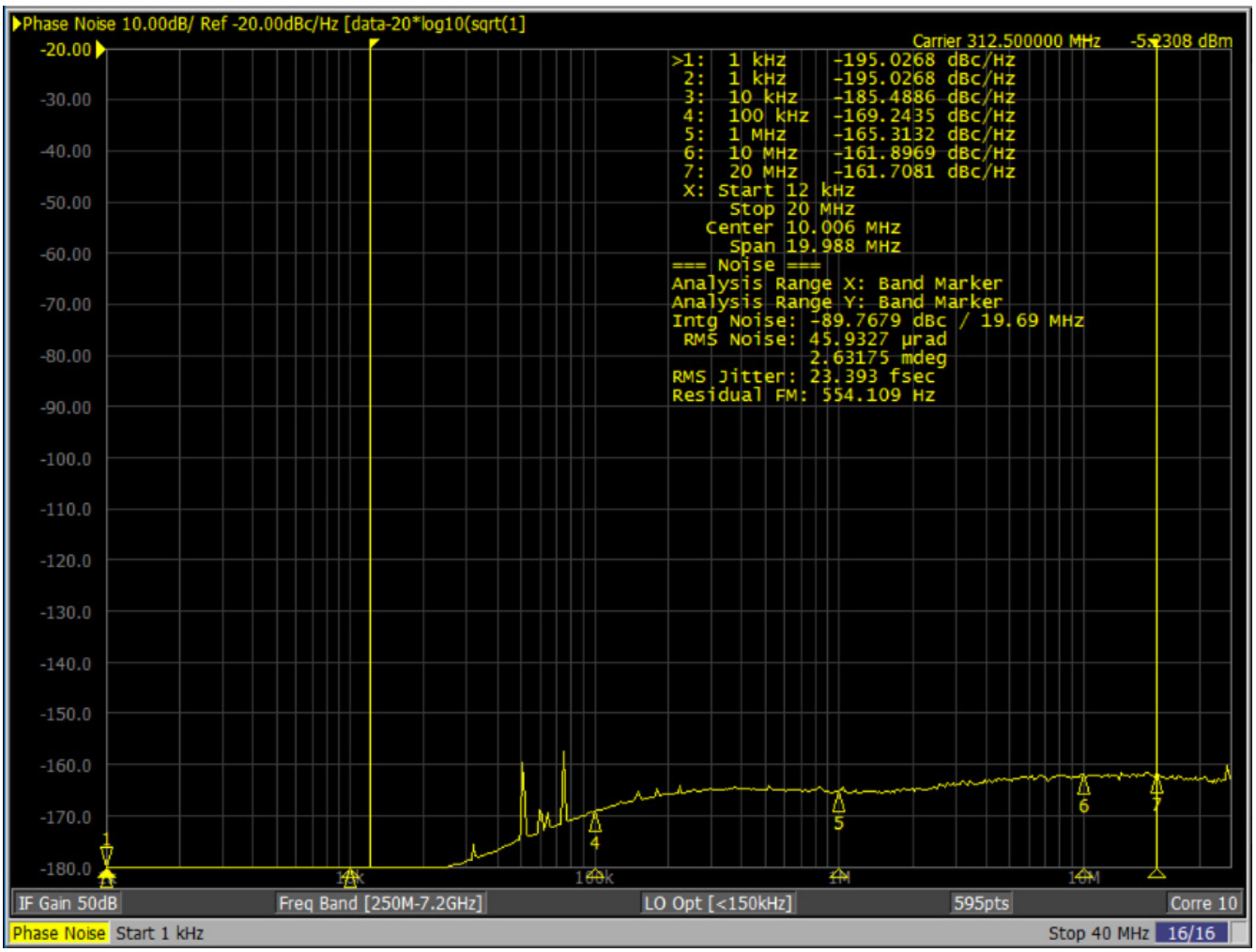


Figure 10. Phase Noise Plot using a Keysight E5052B to Approximate the Effects of a 4MHz High-Pass Filter on a 312.5MHz Output from an RC38312 FC3W device Operating in Synthesizer Mode using a 62.5MHz Crystal along with an APLL VCO Frequency of 9.375GHz; RMS Jitter also displayed

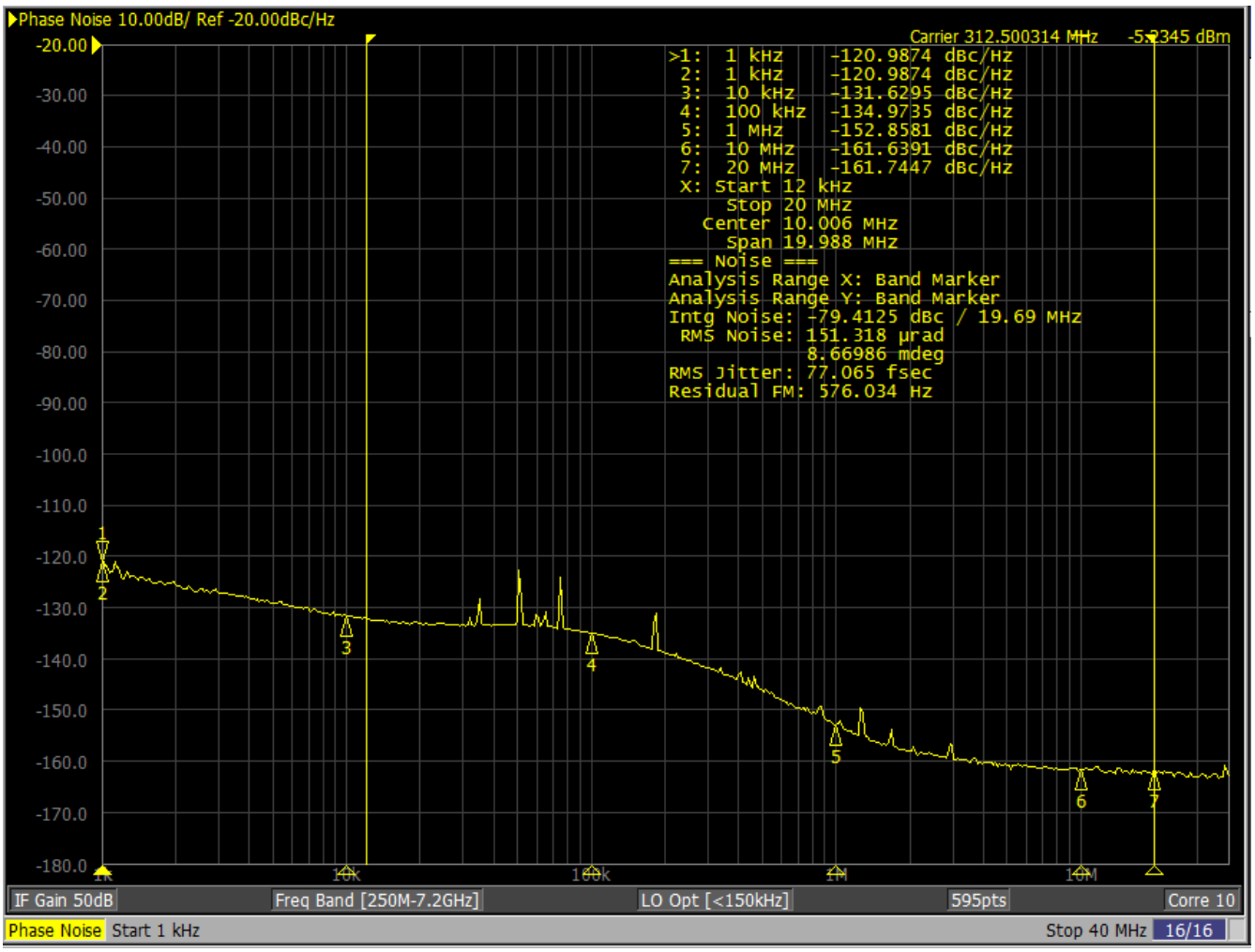


Figure 11. Phase Noise Plot for a 312.5MHz Output from an RC38312 FC3 Device Operating in Jitter Attenuator Mode using a 49.152MHz Crystal along with an APLL VCO Frequency of 9.375GHz, and a 25MHz + 1ppm Reference Clock Input; RMS Jitter also displayed

Figure 12. Phase Noise Plot using a Keysight E5052B to Approximate the Effects of a 4MHz High-Pass Filter on a 312.5MHz Output from an RC38312 FC3W Device Operating in Jitter Attenuator Mode using a 49.152MHz crystal, and a 25MHz + 1ppm Reference Clock Input; RMS jitter also displayed

5. Crystal Recommendations for FC3 to Meet 112G PAM-4 SerDes Reference Clock Requirements

FC3 crystal requirements are explained in the Choosing the Correct Crystal or XO for FemtoClock™3 application note. For a 312.5MHz 112G PAM-4 reference clock using FC3, Renesas recommends using a crystal or XO with a frequency of 62.5MHz if using synthesizer mode or a frequency of 49.152MHzMHz if using jitter attenuator mode. When using FC3W, Renesas recommends using a crystal or XO with a frequency of 62.5MHz if using synthesizer mode or a frequency of 54MHz if using jitter attenuator mode.

Table 4 and Table 5 list several crystals and XOs that Renesas recommends that will allow FC3 and FC3W to meet the SerDes reference clock requirements.

Table 4. FC3 and FC3W Crystal Recommendations to Meet Requirements for a 312.5MHz 112G PAM-4 SerDes Reference Clock

Manufacturer	Type	Part Number	Product Size (mm)	Freq. (MHz)	ESR (Ω)	C_L (pF)	Typical Drive Level (µW)	Freq. Tolerance (ppm)	Frequency Stability (ppm)	Aging (ppm/year at 25°C)	Temperature Range (ºC)
TXC	XTAL	7M49172003	3.2 × 2.5	49.152	20	8	300	±10	±15	±5	-40 to +85
TXC	XTAL	8Y49172005	2.0 × 1.6	49.152	30	12	100	±10	±15	±1	-40 to +85
TXC	XTAL	7M54072002	3.2 × 2.5	54	50	8	100	±12	±15	±3	-40 to +85
TXC	XTAL	8Y62572002	2.0 × 1.6	62.5	40	8	100	-5 to 12	-15 to 12	±1	-40 to +85
TXC	XTAL	8Z62572001	2.5 × 2.0	62.5	40	8	100	-5 to 12	-15 to 12	±1	-40 to +85
TXC	XTAL	8Y73072002	2.0 × 1.6	73	40	8	100	-5 to 12	-15 to 12	±1	-40 to 85
NDK	XTAL	EXS00A-CS15295	2.0 × 1.6	62.5	35	9	200	±30	-	-	-40 to +85

Table 5. FC3 and FC3W XO Recommendations to Meet Requirements for a 312.5MHz 112G PAM-4 SerDes Reference Clock

Manufacturer	Type	Part Number	Product Size (mm)	Frequency (MHz)	Voltage (V)	Total Frequency Stability (ppm)	Temperature Range (°C)
TXC	XO	8W49170004	2.5 × 2.0	49.152	3.3	±25	-40~+85
TXC	XO	8W62570006	2.5 × 2.0	62.5	3.3	±50	-40~+105
TXC	XO	8W73070001	2.5 x 2.0	73	3.3	±50	-40~+105
NDK	XO	RNA5024A	2.5 × 2.0	54	3.3	±30	-40~+105

6. Revision History

Revision	Date	Description
1.04	Jan 8, 2025	▪ Replaced all screen shots with updated images and data. ▪ Updated sections 3 and 4 with revised text and new sub-sections.
1.03	Jun 14, 2024	▪ Updated descriptive text in section 4. ▪ Added two entries of 49.152MHz XTAL specifications (part numbers 7M49172003 and 8Y49172005) to Table 4. ▪ Added 73MHz XTAL specification (part number 8Y73072002) to Table 4. ▪ Added 49.152MHz XO specification (part number 8W49170004) to Table 5. ▪ Added 73MHz XO specification (part number 8W73070001) to Table 5.
1.02	Jun 6, 2024	▪ Updated document title to include FemtoClock 3 Wireless. ▪ Added FemtoClock 3 Wireless (FC3W) content throughout.
1.01	Nov 2, 2023	Updated the titles of Figures 4, 5, and 6.
1.00	Nov 1, 2023	Initial release.

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