Countdown Timer Example
SLG47910

Abstract

This application shows how to build a down-counter which can be used as a countdown timer to count down from the user specified value down to 0.

This application note comes complete with a design file which can be found in the References Section.

Contents

1. Terms and Definitions

FPGA	Field Programmable Gate Array
FPGA Editor	Main FPGA design and simulation window
Go Configure Software Hub	Main window for device selection.
ForgeFPGA Window	Main FPGA project window for debug and IO programming

2. References

For related documents and software, please visit https://www.renesas.com/eu/en/products/programmable-mixed-signal-asic-ip-products/forgefpga-low-density-fpgas. Download our free ForgeFPGA™ Designer software [1] to open the .ffpga design files [2] and view the proposed circuit design.

[1] ForgeFPGA Designer Software, Software Download and User Guide

[2] AN-FG-007 Countdown Timer Example.ffpga, ForgeFPGA Design File

[3] ForgeFPGA SLG47910, Datasheet, Renesas Electronics

3. Introduction

This application shows how a countdown timer works. It explains how to design a down counter (Figure 1) which will count down from a user defined value down to zero. But in such cases where the start value is user defined and the width of the counter cannot be determined, a mathematical function is used to determine the number of bits needed for the width of the counter.

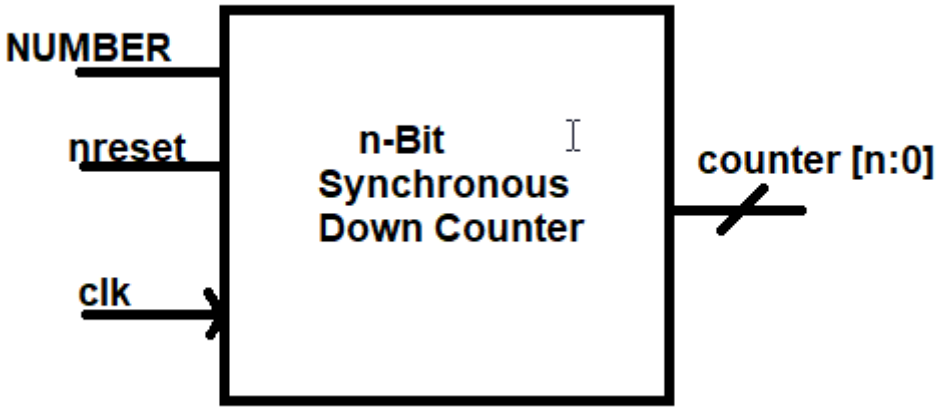

Figure 1: n-bit Down Counter

The following signal names are the PINs that are used in the design.

- NUMBER - parameter to define the start of the counter.
- clk - input clock signal
- nreset - input negative reset signal
- counter - output signal of width [$clog2() :0]

Using the ForgeFPGA Workshop software, the Verilog code was synthesized, and the bit stream was loaded on to the SLG47910 device. The functional waveforms below (see Figure 2) shows the countdown timer counting from 100 (default setup) down to 0.

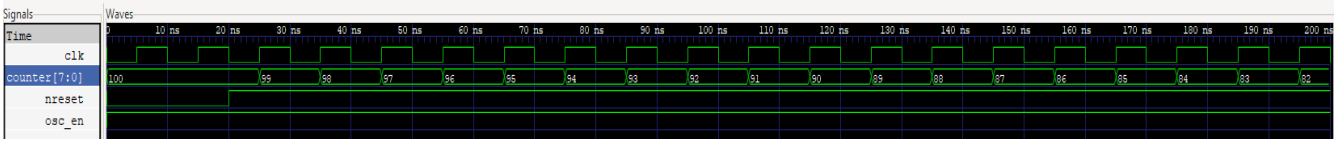

Figure 2: Countdown Timer Functional Waveform

4. Ingredients

- ForgeFPGA Device SLG47910V
- Latest Revision of ForgeFPGA Workshop software
- GTKWave software (inbuilt in ForgeFPGA Workshop software)

5. Countdown Timer Verilog Code

Shown below is the (*top*) module named Timer. It is available for download (AN-FG-007 Countdown Timer Example.ffpga)

```
// Timer Example counting down from the specified value

(* top *) module timer
      #(parameter NUMBER = 100)(    // user can set the number here
      (* iopad_external_pin, clkbuf_inhibit *) input clk,
      (* iopad_external_pin *) input nreset, // external reset though GPIO18
      (* iopad_external_pin *) output[$clog2(NUMBER):0] counter_oe, //[7:0]in this
case
      (* iopad_external_pin *) output osc_en,
      (* iopad_external_pin *) output[$clog2(NUMBER):0] counter // [7:0]in this
case
      //$clog2() returns the ceiling of the logarithm to the base 2
);

    reg [$clog2(NUMBER):0] count;
    reg count_stop = 'b0;
    //OE
    assign counter_oe =8'b11111111;
    assign osc_en = 1;

    always @(posedge clk or negedge nreset) begin
      if (!nreset)
            count <= NUMBER;
        else
        if(count != count_stop)           //  count down till value equals 0
           count <= count - 4'd1;
        else
            count = 0 ;
       end

 assign counter = count;

endmodule
```

Note :

$clog2() is a Verilog function which returns the ceiling of the logarithm to the base 2. In cases where the answer is a decimal number; the function rounds it to the next integer value. The argument can be an integer or an arbitrary sized vector value. The argument shall be treated as an unsigned value, and an argument value of 0 shall produce a result of 0.

Example :

`$clog2(8) = 3`

`$clog2(15) = 3.907  ≈ 4`

`$clog2(4095) = 12`

Hence, with the help of $clog2() function we can determine the maximum number of bits needed for the counter output.

6. Floorplan: CLB Utilization

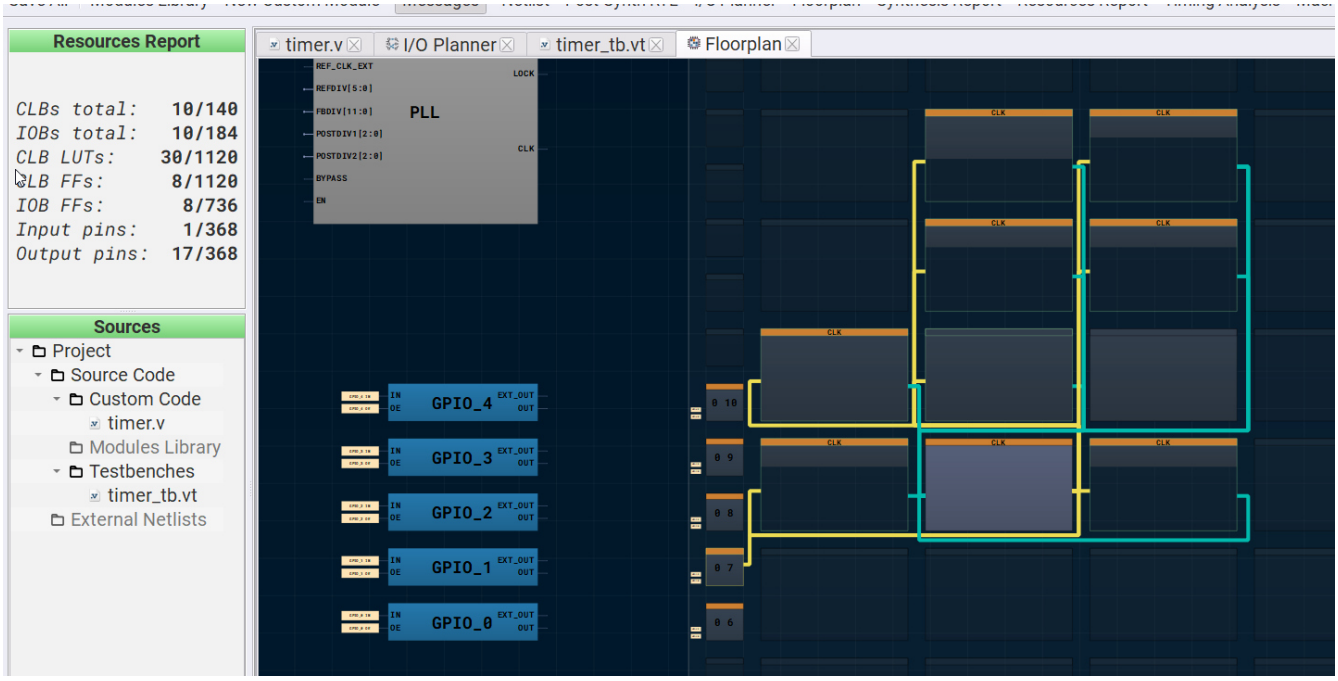

Figure 3: Countdown Timer CLB Utilization

The Floor planner tab in the FPGA Editor shows the placement of CLBs and FFs (Figure 3). The resource utilization is shown in the top left corner.

7. Design Steps

1. Launch the latest version of the Go Configure Software Hub. Select the SLG47910V device and the ForgeFPGA Workshop software will load.
2. Download the design example Countdown Timer Example.ffpga. If you are not familiar with the ForgeFPGA Workshop software, review the Four-Bit Counter application notes that cover the basic design steps.
3. Open the Countdown Timer Example.ffpga file after downloading.
4. Open the FPGA editor and review the Verilog code and the testbench code. Enter the desired NUMBER you want to countdown from (default 100).
5. Open the IO planner tab on the FPGA editor and review the pin assignment.
6. Next select the Synthesize button on the lower left side of the FPGA editor. Select the Generate Bitstream button on the lower left side of the FPGA editor. Check the Logger and Issues tabs to make sure that the bit steam was generated correctly.
7. Now click on the Floorplan tab and see the CLB utilization (Figure 3). Press the Ctrl and the mouse wheel to zoom-in. Confirm that the IOs selected in the IO Planner are shown in the floorplan.
8. Now click on the Simulate Testbench button at the top. The GTKWave will automatically open if there are no Syntax errors in the testbench. Check logger for errors.
9. In the GTKWave software, select the signals you want to view and Click Insert on the left corner to insert the signals in the wave window. Once the desired signals are selected, click on Reload (Figure 2).
10. You can observe the countdown in the waveform displayed in the GTKWave software. The same results can also be observed in the Logger of the ForgeFPGA Workshop software. The countdown value can be observed in the Logger along with its corresponding time unit it occurs at.

8. Conclusions

This application note shows how the SLG47910 can be used to count down from a user specified value and how the width of the number can be determined using $clog2() function accurately. This testcase is available for download (AN-FG-007 Countdown Timer Example.ffpga). If interested, please contact the ForgeFPGA Business Support Team.

9. Revision History

Revision	Date	Description
1.0	01-April-2022	Initial Version
2.0	23-Feb-2024	Updated according to BB revision
3.0	17-Jul-24	Updated as per ForgeFPGA Workshop v6.43

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