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H8/38086R Group

ΔΣ A/D Converter

Introduction

The H8/38086R internal ΔΣ A/D converter is used to measure the voltage input to the Ain pin and store the measured voltage in the internal RAM.

Target Device

H8/38086R

Contents

1. Voltage Measurement Using the ΔΣ A/D Converter When an External Reference Voltage Used

1.1 Specifications

- As shown in figure 1, the H8/38086R internal ΔΣ A/D converter is used to measure the voltage input to the Ain pin.
- The external input voltage is used as the reference voltage for the ΔΣ A/D converter.
- The voltage input to the Ain pin and measured is converted from analog data to digital values, and the results of the A/D conversion are stored in the internal RAM. A/D conversion is performed twice, with the results of the first conversion being discarded. Only the results of the second conversion are stored in internal RAM. The 14-bit results of the A/D conversion that are read from the A/D Data Register (ADDR) are stored in the internal RAM after being shifted to the right 2 bits.
- As the conversion mode, the wait mode is used, the oversampling frequency is ϕ, and programmable gain amplifier (PGA) bypass mode is used to perform A/D conversion.
- A transition to the sleep (high-speed) mode is made during A/D conversion to reduce the noise generated by the CPU and other modules. By using the A/D conversion end interrupt, the sleep (high-speed) mode is canceled, a transition to the active (high-speed) mode is made, and the results of A/D conversion are stored in the internal RAM. The module standby function is used to place the internal peripheral modules except the ΔΣ A/D converter (such as the SCI3, A/D converter, timer F, RTC, TPU, IIC2, PWM, AEC, watchdog timer, and LCD) in the module standby mode.

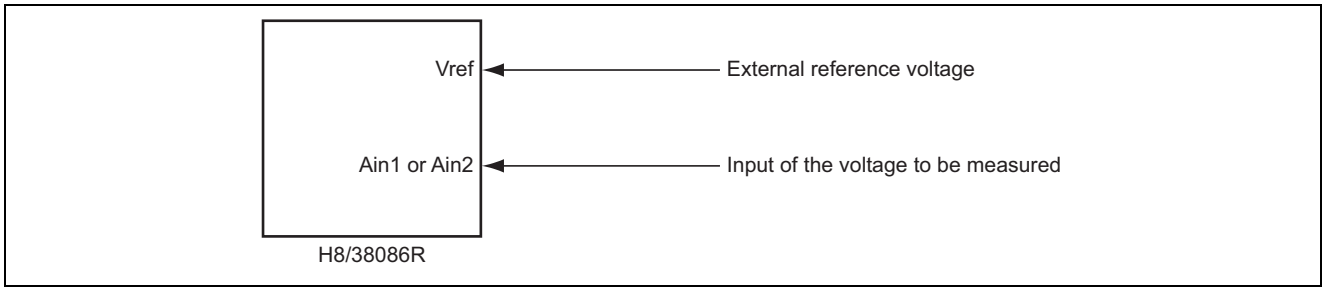


Figure 1 Voltage Measurement Using the ΔΣ A/D Converter (External Reference Voltage Used)

1.2 ΔΣ A/D Converter Measurement Conditions

Figure 2 shows the measurement circuit for this sample task.

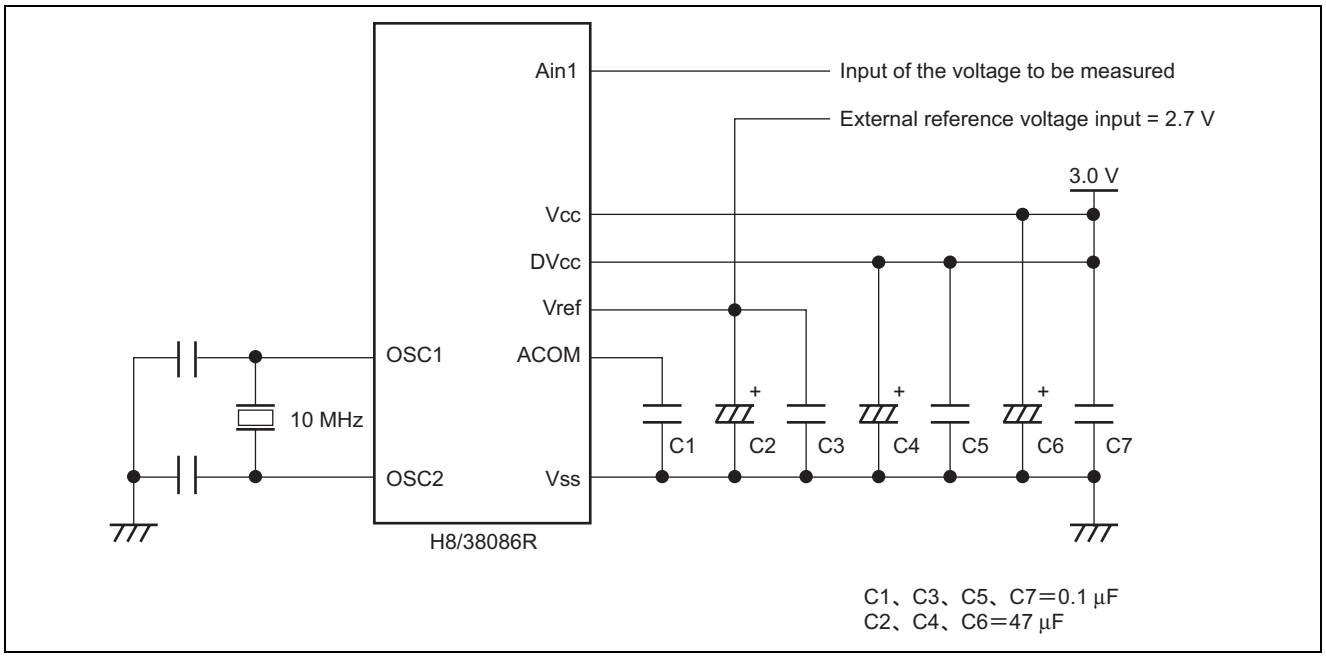


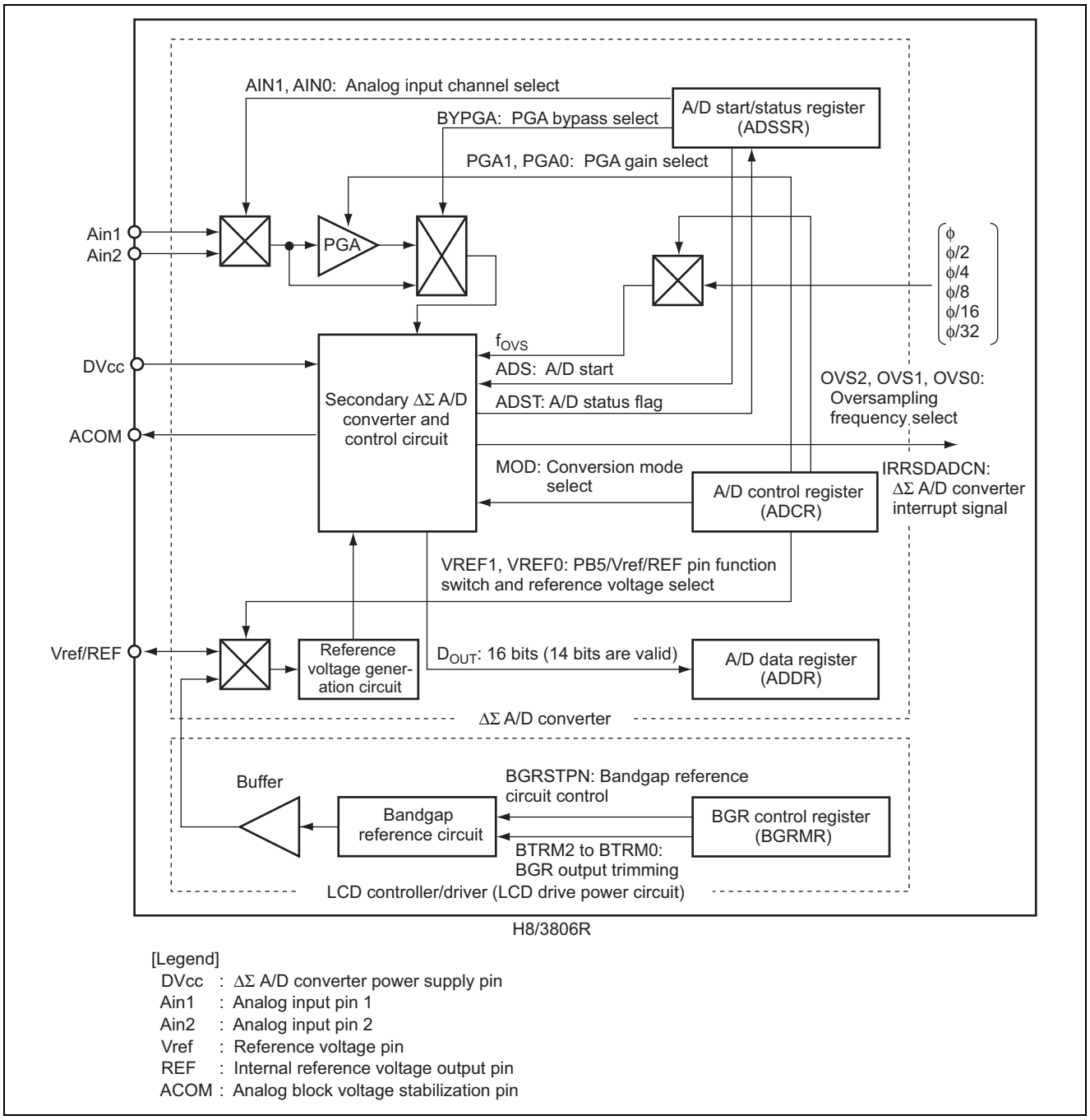
Figure 2 ΔΣ A/D Converter Measurement Circuit (External Reference Voltage Used)

The following are the measurement conditions for a voltage measurement for the ΔΣ A/D converter when an external voltage is used:

- Vcc = 3.0 V
- DVcc = 3.0 V
- Vref = External input of 2.7 V
- System clock frequency (ϕ) = 10 MHz
- Oversampling frequency (f_{OVS}) = ϕ
- PGA = Bypass
- Conversion mode = Wait mode
- Input voltage range= 0.2 V to Vref (2.7 V)

1.3 Description of Functions Used

Figure 3 shows a block diagram of the ΔΣ A/D converter.



[Legend]
DVcc : ΔΣ A/D converter power supply pin
Ain1 : Analog input pin 1
Ain2 : Analog input pin 2
Vref : Reference voltage pin
REF : Internal reference voltage output pin
ACOM : Analog block voltage stabilization pin

Figure 3 ΔΣ A/D Converter Block Diagram

The functions of the ΔΣ A/D converter are described below.

1.3.1 Features

- Resolution: 14 bits
- Number of input channels: 2
- Conversion method: Secondary ΔΣ, 320-times oversampling
- Conversion time: 32 µs per channel (at 10-MHz operation)
- Number of interrupt sources: 1 (A/D conversion end interrupt request)
- Capability of isolating the module in standby mode using the module standby mode when the ΔΣ A/D converter is not in use.

1.3.2 Input/Output Pins

The pins used by the ΔΣ A/D converter are described in table 1.

Table 1 ΔΣ A/D Converter Pins

Pin Name	Symbol	I/O	Function
Reference voltage pin	Vref	Input	External reference voltage input
Internal reference voltage output pin	REF	Output	Internal reference voltage output
Analog block voltage stabilization pin	ACOM	Output	Connection to capacitor of 0.1 µF for stabilization
Analog input pin 1	Ain1	Input	Analog input pin
Analog input pin 2	Ain2	Input	Analog input pin
ΔΣ A/D converter analog power supply pin	DVcc	Input	Power supply pin

1.3.3 Internal Registers Used

The ΔΣ A/D converter has the following registers:

- A/D Data Register (ADDR)
  ADDR is a 16-bit read-only register that stores the result of A/D conversion. ADDR is always readable from the CPU. During A/D conversion, the ADDR value is undefined. After conversion, fourteen bits of converted data is stored in the upper 14 bits of ADDR. ADDR holds this data until the next conversion is started. The initial ADDR value is undefined.
- BGR Control Register (BGRMR)
  BGRMR controls operation of the bandgap reference circuit (BGR) and adjusts the internal reference voltage (BGR output voltage) output from the REF pin.
- A/D Control Register (ADCR)
  ADCR sets the conversion mode, sets the PGA (programmable gain amplifier) multiplication, selects the PB5/Vref/REF pin function, sets the reference voltage, and sets the oversampling frequency.
- A/D Start/Status Register (ADSSR)
  ADSSR sets the A/D conversion status flag, selects the analog input channel, and selects PGA bypass mode.

1.3.4 ΔΣ A/D Converter

The ΔΣ A/D converter, which uses a ΔΣ modulator, converts the analog input voltage range determined by the Vref pin to digital values with 14-bit resolution. The ΔΣ A/D converter consists of an analog block whose main part is the ΔΣ modulator and a digital block based on a digital filtering control circuit.
In the analog block, the voltages from analog input pins 1 and 2 (Ain1 and Ain2) are sampled with a frequency 320 times that of the conversion cycle (oversampling frequency), and then converted to a 1-bit digital value string by the secondary ΔΣ modulator. The result of conversion is passed through a decimation filter in the digital block and then output to the A/D Data Register (ADDR) as 14-bit unsigned binary data. In ADDR, bit 13 is the MSB and bit 0 the LSB.

1.3.5 Conversion Modes of the ΔΣ A/D Converter

The ΔΣ A/D converter supports two conversion modes: the wait mode and the continuous mode.

(1) Wait mode

In the wait mode, A/D conversion is performed one time for the analog input on the specified channel in the following steps:

1. When the ADS bit of the A/D Start/Status Register (ADSSR) is set to 1 by software, A/D conversion of the analog input on the specified channel starts.
2. When the A/D conversion is complete, the result is transferred to the A/D Data Register (ADDR).
3. When the A/D conversion has been completed, the A/D converter interrupt request flag (IRRSAD) of Interrupt Request Register 2 (IRR2) is set to 1. At this point, if the A/D Converter Interrupt Request Enable bit (IENSAD)of Interrupt Enable Register 2 (IENR2) is 1, an A/D conversion end interrupt request is generated.
4. The ADST bit is held at 1 during A/D conversion, and when the conversion finishes, it is automatically cleared to 0, and the A/D converter enters the wait state.

(2) Continuous mode

In the continuous mode, A/D conversion is performed continuously for the analog input on the specified channel in the following steps:

1. When the MOD bit of the A/D Control Register (ADCR) is set to 1 by software, A/D conversion of the analog input on the specified channel starts.
2. When the A/D conversion is complete, the result is transferred to the A/D Data Register.
3. When the A/D conversion has been completed, the A/D converter interrupt request flag (IRRSAD) of Interrupt Request Register 2 (IRR2) is set to 1. At this point, if the A/D Converter Interrupt Request Enable bit (IENSAD) of Interrupt Enable Register 2 (IENR2) is 1, an A/D conversion end interrupt request is generated.
4. Steps 2 and 3 are repeated. The continuous mode is released by resetting, by placing the converter in the watch mode, sub-active mode, sub-sleep mode, or standby mode, or by clearing the MOD bit of the ADCR register to 0.

1.3.6 ΔΣ A/D Converter Registers and the MCU Operating Modes

The states of the ΔΣ A/D converter registers in the MCU operating modes are shown in table 2.

Table 2 ΔΣ A/D Converter Operating Modes

Operating Mode	At a Reset	Active	Sleep	Watch	Sub-Active	Sub-Sleep	Standby	Module Standby
ADCR register	Reset	Operating	Retained	Retained	Retained	Retained	Retained	Retained
ADSSR register	Reset	Operating	Operating	Retained	Retained	Retained	Retained	Retained
ADDR register	Retained*	Operating	Operating	Retained	Retained	Retained	Retained	Retained
BGRMR register	Reset	Operating	Retained	Retained	Operating	Retained	Retained	Retained

Note: * Undefined after a power-on reset.

1.3.7 Pin Assignments

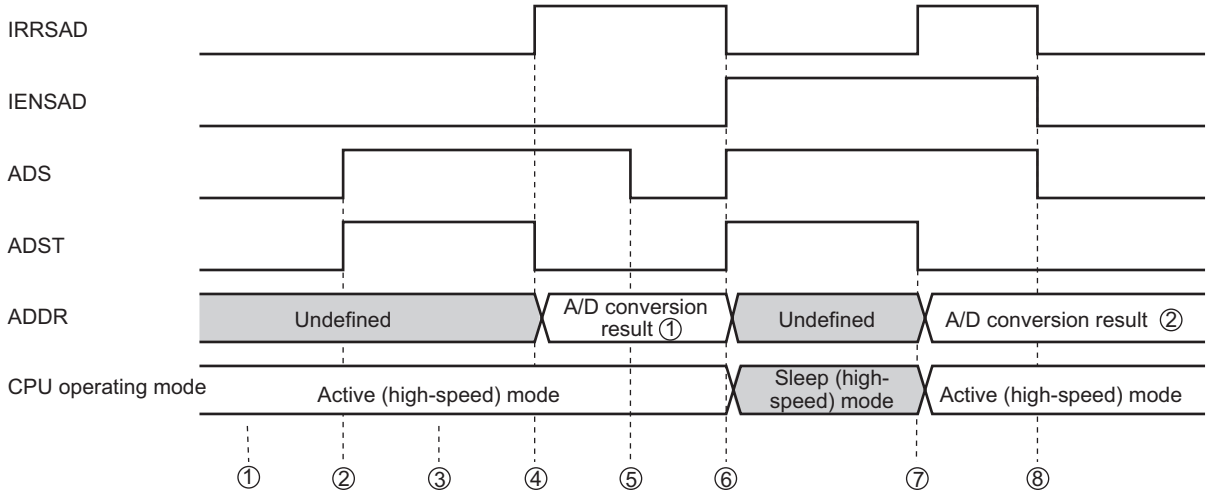
Pin assignments in this sample task are listed in table 3.

Table 3 Assignment of Functions

Pin Name	Description
Vref/REF	The external reference voltage 2.7 VDC is input to the Vref input pin.
DVcc	3.0 VDC is input to the ΔΣ A/D converter from this analog input pin.
Ain1	The measured value is input to this analog input pin.
Ain2	Unused
ACOM	Connected to a 0.1-μF capacitor as the analog block voltage stabilization pin.

1.4 Principles of Operation

Figure 4 illustrates the principles of operation of ΔΣ A/D conversion in this sample task, in which the wait mode is used. In this sample task, software polling is used to determine when the first A/D conversion has ended. In the second A/D conversion, an interrupt is used to cancel the sleep (high-speed) mode.



① Initial setting of the ΔΣ A/D converter

Software processing	1. Set ADCR to H'04. (conversion mode: wait mode, oversampling frequency: ϕ, PB5/Vref/REF pin function: Vref input pin, Reference voltage: External reference voltage) 2. Set ADSSR to H'18. (Analog input channel: Ain1, PGA bypass)

② Start of the first A/D conversion

Hardware processing	Set the ADST bit of ADSSR to 1, and the ΔΣ A/D converter is performing A/D conversion.
Software processing	Set the ADST bit of ADSSR to 1 to start A/D conversion.

③ Waiting for the first A/D conversion to end

Hardware processing	Convert the analog input to digital values.
Software processing	Wait until the ADST bit of ADSSR becomes 0 (software polling).

④ End of the first A/D conversion

Hardware processing	Clear the ADST bit of ADSSR to 0 and transfer the A/D conversion result to ADDR.

⑤ Reading of the result of the first A/D conversion

Software processing	Clear the ADS bit of ADSSR to 0.

⑥ Start of the second A/D conversion

Hardware processing	1. Set the ADST bit of ADSSR to 1. The ΔΣ A/D converter performs A/D conversion. 2. Make a transition to the sleep (high-speed) mode.
Software processing	1. Set the ADS bit of ADSSR to 1 to start A/D conversion. 2. Clear the IRRSAD bit of IRR2 to 0, set the IENSAD bit to 1, and enable A/D conversion end interrupts. 3. Make a transition to the sleep (high-speed) mode in response to a sleep instruction.

⑦ End of the second A/D conversion

Hardware processing	1. Clear the ADST bit of ADSSR to 0 and transfer the A/D conversion result to ADDR. 2. Cancel the sleep (high-speed) mode and make a transition to the active (high-speed) mode in response to an A/D conversion end interrupt request.

⑧ Reading of the result of the second A/D conversion (A/D conversion end interrupt processing)

Software processing	1. Clear the IRRSAD and IENSAD bits of IRR2 to 0 to disable A/D conversion end interrupts. 2. Clear the ADS bit of ADSSR to 0, read the result of A/D conversion from ADDR, and store it in the internal RAM.

Figure 4 Voltage Measurement with the ΔΣ A/D Converter Using an External Reference Voltage

1.5 Description of Software

1.5.1 Internal Registers Used

This section describes the internal registers used in this sample task.

(1) A/D Data Register (ADDR) Address: H'F062

Table 4 A/D Data Register (ADDR)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
15	ADD13	Undefined	R	This 16-bit read-only register stores the result of A/D conversion. The upper 14 bits store 14 bits of A/D conversion data. During A/D conversion, the ADDR value is undefined.	—
14	ADD12				
13	ADD11				
12	ADD10				
11	ADD9				
10	ADD8				
9	ADD7				
8	ADD6				
7	ADD5				
6	ADD4				
5	ADD3				
4	ADD2				
3	ADD1				
2	ADD0				
1	—	Undefined	—	—	—
0	—	Undefined	—	—	—

(2) A/D Control Register (ADCR) Address: H'F060

Table 5 A/D Control Register (ADCR)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	MOD	0	R/W	Conversion Mode Select This bit selects conversion mode. When MOD=1, A/D conversion is performed regardless of the ADS bit of ADSSR register. 0: Wait mode 1: Continuous mode	0
6	OVS2	0	R/W	Oversampling Frequency Select These bits select the oversampling frequency. 000: φ 001: φ/2 010: φ/4 011: φ/8 100: φ/16 101: φ/32 11x: Setting prohibited	0 0 0
5	OVS1	0	R/W		
4	OVS0	0	R/W		

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
3	VREF1	0	R/W	PB5/Vref/REF Pin Function Switch and	0
2	VREF0	0	R/W	Reference Voltage Select These bits set whether to use the PB5/Vref/REF pin as the PB5 pin, Vref pin, or REF pin. In addition, these bits select whether to use an external reference voltage (Vref) or the internal reference voltage (REF) as the reference voltage to the ΔΣ A/D converter. Note, however, that when REF is used, the BGRSTPN bit of BGRMR must be set to 1 before setting these bits, to start operation of BGR (bandgap reference circuit). 00: The pin functions as the PB5 input pin. 01: The pin functions as the Vref input pin, and an external reference voltage (Vref) is input to the reference voltage generation circuit. 10: The pin functions as the REF output pin. 11: The pin functions as the REF output pin, and the internal reference voltage (REF) is input to the reference voltage generation circuit. Setting B'11 causes the REF pin to output the internal reference voltage (REF), which is then input to the reference voltage generation circuit in the ΔΣ A/D converter. Set these bits to B'11 to use the internal reference voltage (REF) for ΔΣ A/D converter operation.	1
1	PGA1	0	R/W	PGA Gain Select	0
0	PGA0	0	R/W	These bits specify an analog input voltage multiplied with multipliers ranging from 1/3 to 4. 00: x1 01: x2 10: x4 11: x1/3	0

(3) A/D Start/Status Register (ADSSR) Address: H'F061

Table 6 A/D Start/Status Register (ADSSR)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	ADS	0	R/W	A/D Start In the wait mode (the MOD bit of ADCR is 0), setting this bit to 1 starts A/D conversion.	1
6	ADST	0	R	A/D Status Flag In the wait mode (the MOD bit of ADCR is 0), this bit can be read to determine the status of A/D conversion. 0: In an idle state 1: A/D conversion in operation	—
5	AIN1	0	R/W	Analog Input Channel Select	0
4	AIN0	0		These bits select the analog input channel. 00: Deselected 01: Ain1 10: Ain2 11: Deselected	1
3	BYPGA	0	R/W	PGA Bypass Select This bit selects whether to input the analog data to the PGA or the secondary ΔΣ A/D converter. 0: Inputs the analog data to the PGA. 1: Inputs the analog data to the secondary ΔΣ A/D converter.	1
2	—	0	—	Reserved (these bits cannot be modified)	—
1	—	0	—		—
0	—	0	—		—

(4) Interrupt Enable Register 2 (IENR2) Address: H'FFF4

Table 7 Interrupt Enable Register 2 (IENR2)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
5	IENSAD	0	R/W	ΔΣ A/D Converter Interrupt Request Enable Setting this bit to 1 enables ΔΣ A/D converter interrupt requests. 0: Disables ΔΣ A/D converter interrupt requests. 1: Enables ΔΣ A/D converter interrupt requests.	1

(5) Interrupt Request Register 2 (IRR2) Address: H'FFF7

Table 8 Interrupt Request Register 2 (IRR2)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
5	IRRSAD	0	R/(W)*	ΔΣ A/D Converter Interrupt Request Flag [Setting condition] When ΔΣ A/D conversion is completed [Clearing condition] When 0 is written	0

Note: * Only 0 can be written to clear the flag.

(6) System Control Register 1 (SYSCR1) Address: H'FFF0

Table 9 System Control Register 1 (SYSCR1)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	SSBY	0	R/W	Software Standby This bit selects the mode to which a transition to be made when the SLEEP instruction is executed. 0: The transition is to the sleep mode or the sub-sleep mode. 1: The transition is to the standby mode or the watch mode.	0
3	LSON	0	R/W	Low-Speed On Flag This bit selects whether to use the system clock (ϕ) or the subclock (ϕ_{SUB}) as the CPU operating clock when the watch mode is canceled. 0: Uses the system clock (ϕ) as the CPU operating clock. 1: Uses the subclock (ϕ_{SUB}) as the CPU operating clock.	0

(7) System Control Register 2 (SYSCR2) Address: H'FFF1

Table 10 System Control Register 2 (SYSCR2)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
3	DTON	0	R/W	Direct Transfer On Flag This bit selects the target of transition to be made after the SLEEP instruction is executed together with SYSCR1's SSBY, TMA3, LSON bits, and SYSCR2's MSON bit.	0
2	MSON	0	R/W	Middle Speed On Flag This bit selects whether operation is to be in the active (high speed) mode or the active (middle speed) mode after the standby mode, the watch mode, or the sleep mode is canceled.	0

(8) Clock Stop Register 1 (CKSTPR1) Address: H'FFFA

Table 11 Clock Stop Register 1 (CKSTPR1)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	S4CKSTP	1	R/W*1	SCI4 Module Standby When this bit is set to 0, SCI4 enters the standby mode. 0: Places SCI4 in the module standby mode. 1: Cancels the module standby mode of SCI4.	1
6	S31CKSTP	1	R/W	SCI3_1 Module Standby*2 When this bit is set to 0, SCI3_1 enters the standby mode. 0: Places SCI3_1 in the module standby mode. 1: Cancels the module standby mode of SCI3_1.	0
5	S32CKSTP	1	R/W	SCI3_2 Module Standby2 When this bit is set to 0, SCI3_2 enters the standby mode. 0: Places SCI3_2 in the module standby mode. 1: Cancels the module standby mode of SCI3_2.	0
4	ADCKSTP	1	R/W	A/D Converter Module Standby When this bit is set to 0, the A/D converter enters the standby mode. 0: Places the A/D converter in the module standby mode. 1: Clears the module standby mode of the A/D converter.	0

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
3	DADCKSTP	1	R/W	ΔΣ A/D Converter Module Standby When this bit is set to 0, the ΔΣ A/D converter enters the standby mode. 0: Places the ΔΣ A/D converter in the module standby mode. 1: Cancels the module standby mode of the ΔΣ A/D converter.	1
2	TFCKSTP	1	R/W	Timer F Module Standby When this bit is set to 0, timer F enters the standby mode. 0: Places the timer F in the module standby mode. 1: Cancels the module standby mode of the timer F.	0
1	FROMCKSTP	1	R/W	Flash Memory Module Standby When this bit is set to 0, the flash memory enters the standby mode. 0: Places the flash memory in the module standby mode. 1: Cancels the module standby mode of the flash memory.	1
0	RTCCKTP	1	R/W	RTC Module Standby When this bit is set to 0, the RTC enters the standby mode. 0: Places the RTC in the module standby mode. 1: Cancels the module standby mode of the RTC.	0

Notes: *1. Reserved bits that can be neither written nor read in the masked ROM version.
*2. When SCI3 is placed in the module standby mode, all the registers of SCI3 are reset.

(9) Clock Stop Register 2 (CKSTPR2) Address: H'FFFB

Table 12 Clock Stop Register (CKSTPR2)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	ADBCKSTP	1	R/W	Address Break Module Standby When this bit is set to 0, address break module enters the standby mode. 0: Places address break module in the module standby mode. 1: Cancels the module standby mode of address break module.	1

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
6	TPUCKSTP	1	R/W	TPU Module Standby When this bit is set to 0, the TPU enters the standby mode. 0: Places the TPU in the module standby mode. 1: Cancels the module standby mode of the TPU.	0
5	IICCKSTP	1	R/W	IIC2 Module Standby When this bit is set to 0, IIC2 enters the standby mode. 0: Places IIC2 in the module standby mode. 1: Cancels the module standby mode of IIC2.	0
4	PW2CKSTP	1	R/W	PWM2 Module Standby When this bit is set to 0, PWM2 enters the standby mode. 0: Places PWM2 in the module standby mode. 1: Cancels the module standby mode of PWM2.	0
3	AECCKSTP	1	R/W	Asynchronous Event Counter Module Standby When this bit is set to 0, the asynchronous event counter enters the standby mode. 0: Places the asynchronous event counter in the module standby mode. 1: Cancels the module standby mode of the asynchronous event counter.	0
2	WDCKSTP	1	R/W*1	Watchdog Timer Module Standby When this bit is set to 0, the watchdog timer enters the standby mode. 0: Places the watchdog timer in the module standby mode. 1: Cancels the module standby mode of the watchdog timer.	0
1	PW1CKSTP	1	R/W	PWM1 Module Standby When this bit is set to 0, PWM1 enters the standby mode. 0: Places PWM1 in the module standby mode. 1: Cancels the module standby mode of PWM1.	0

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
0	LDCKSTP	1	R/W	LCD Controller/Driver Module Standby When this bit is set to 0, the LCD controller/driver enters the standby mode. 0: Places the LCD controller/driver in the module standby mode. 1: Cancels the module standby mode of the LCD controller/driver.	0

Note: *1. WDCKSTP is valid when WDON of TCSRWD1 is cleared to 0. Although clearing WDCKSTP to 0 when WDON is set to 1 (the watchdog timer is operating) sets WDCKSTP to 0, the watchdog timer does not enter the module standby mode and, instead, continues the watchdog function. As soon as the watchdog function is terminated and WDON is cleared to 0 by software, WDCKSTP takes effect, and the watchdog timer is placed in the module standby mode.

1.5.2 Description of Modules

Table 13 describes the modules in this sample task.

Table 13 List of Modules

Module Name	Function
main( )	Main routine Performs initial setting of the ΔΣ A/D converter, waits for the first ΔΣ A/D conversion to end, enables ΔΣ A/D conversion end interrupt requests, and makes a transition to the sleep (high-speed) mode.
int_dsadc( )	ΔΣ A/D converter interrupt processing routine Clears ΔΣ A/D converter interrupt request flags, disables ΔΣ A/D converter interrupt requests, and stores the result of A/D conversion in the internal RAM.

1.5.3 RAM Usage

Table 14 describes RAM usage in this sample task.

Table 14 RAM Usage

Label Name	Function	Data Size	Address	Used In
ad_data	14-bit result of ΔΣ A/D conversion (lower 14 bits)	2 bytes	H'F780	main( ) int_dsadc( )

1.5.4 Link Address Specifications

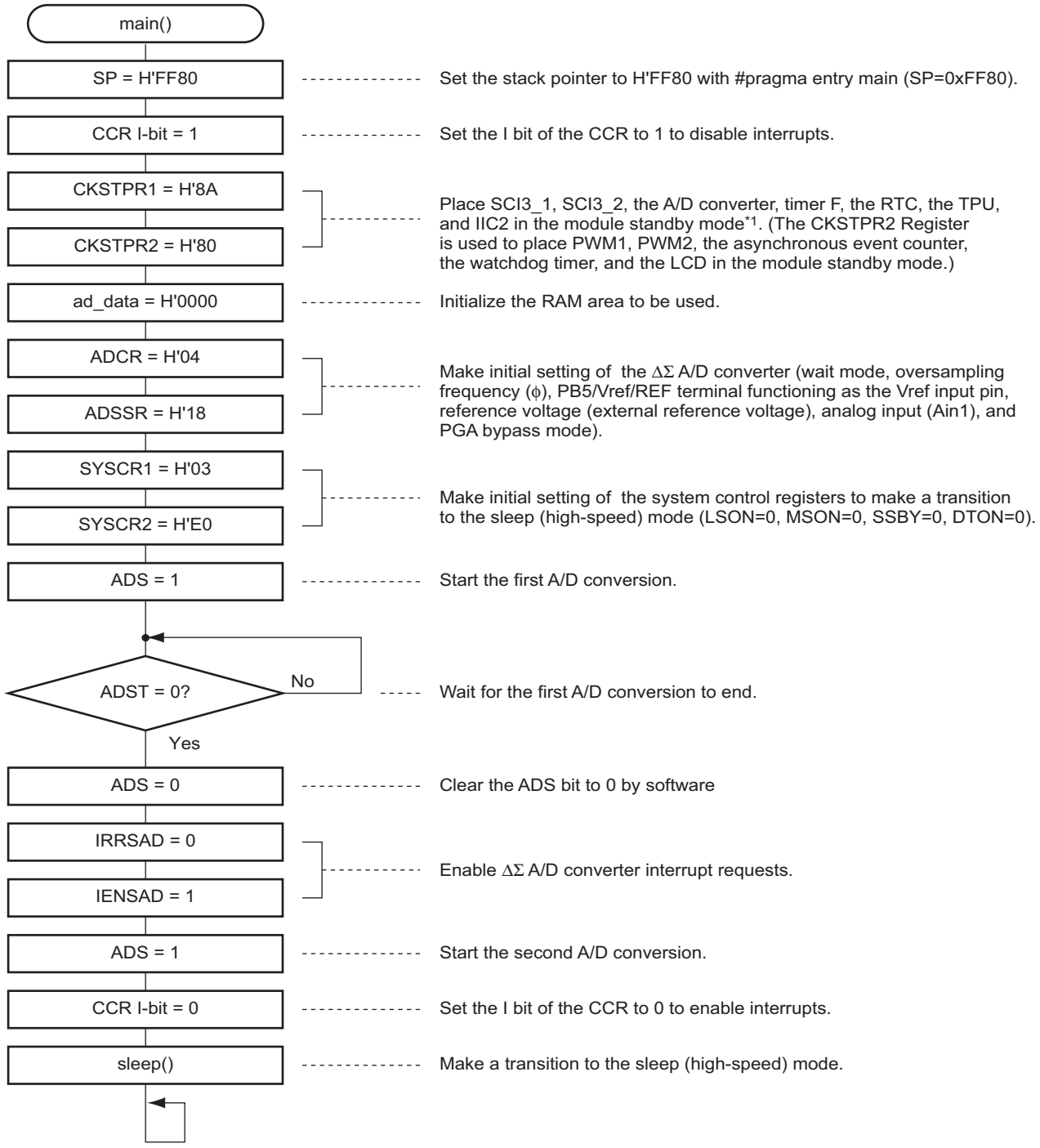
Table 15 provides a description of the link addresses specified in this sample task.

Table 15 Link Addressing

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

1.6 Flowcharts

1.6.1 Main Routine



Note: *1. In this sample task, all internal peripheral modules except SCI4, flash memory, address break, and ΔΣ A/D converter are set to the module standby mode. The user should write 1 to the corresponding bits in the clock stop registers for placing the peripheral modules out of the module standby mode as required.

Figure 5 Main Routine Flowchart

1.6.2 ΔΣ A/D Converter Interrupt Processing Routine

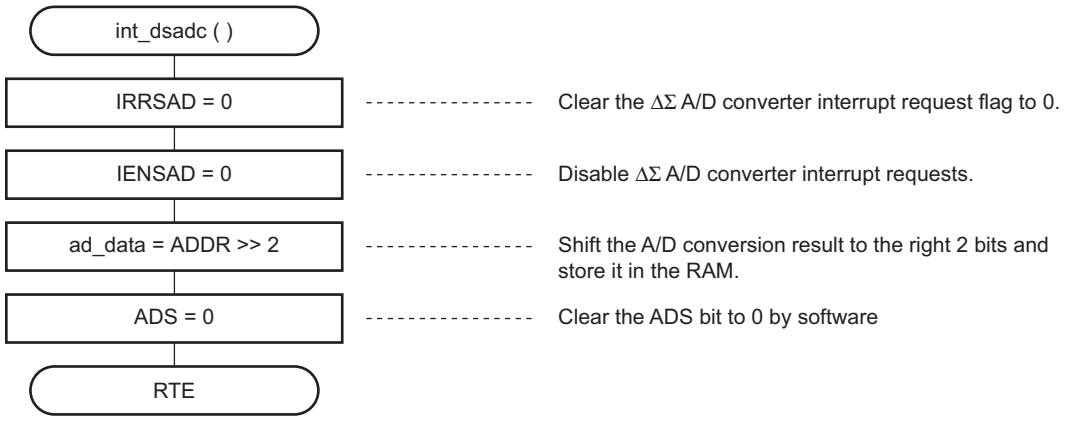


Figure 6 ΔΣ A/D Converter Interrupt Processing Routine

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.13.05	—	First edition issued

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