DA9292 Unused Pin Configuration

This application note describes the recommended configuration for unused pins in applications that use either the DA9292 power management IC.

Contents

Tables

1. Terms and Definitions

CH<x>	Channel <x>, where x = 1 to 2
CPU	Central processing unit
GPU	Graphics processing unit
IC	Integrated circuit
SoC	System on chip

2. References

[1] DA9292_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

DA9292 is a high-performance Power Management IC suitable for supplying high-current rails in CPUs, GPUs, SoCs in multiple end-applications. The device is capable of supporting up to 52 A of peak current in a compact offering, with fully integrated power devices. DA9292 can be configured as either a 20 A quad-phase buck converter or two 10 A dual-phase buck converters.

In some applications, certain functions or features may not be required and, to minimize any potential issues with these unused functions, the pins related to them need to be configured correctly. This document provides guidance on how to configure unused connections on the DA9292.

4. DA9292 Functional Blocks

The following tables describe the recommended configurations for unused pins. Mandatory means that the pin is used in all applications.

Table 1: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DOD	Digital output open drain	AO	Analog output
DIOD	Digital input/output open drain	AIO	Analog input/output
PWR	Power	GND	Ground

Table 2: Pin Description

Pin #	Pin Name	Type (Table 1)	Drive (mA)	Description	If Unused	
					1CH4PH Operation	2CH2PH Operation
A1, B1, C1	VDD1	PWR	5000	Power supply for phase1	Mandatory	Connect to GND (no cap required)
A2, B2, C2	LX1	AIO	5000	LX node of phase1	Mandatory	Leave floating (L and Cout not required)
A3, B3, C3	GND1	GND	5000	Power ground of phase1	Mandatory	Mandatory
A4, B4, C4	GND2	GND	5000	Power ground of phase2	Mandatory	Mandatory

Pin #	Pin Name	Type (Table 1)	Drive (mA)	Description	If Unused	
					1CH4PH Operation	2CH2PH Operation
A5, B5, C5	LX2	AIO	5000	LX node of phase2	Mandatory	Leave floating (L and Cout not required)
A6, B6, C6	VDD2	PWR	5000	Power supply for phase2	Mandatory	Connect to GND (no cap required)
D1	FBN1	AI	10	Negative remote sense input for CH1	Mandatory	Connect to GND
D2	EN1	DI	10	Enable/disable input of CH1	Connect to GND	Connect to GND
D3	VSEL1	DI	10	External voltage control pin of CH1	Connect to GND	Connect to GND
D4	INT_N	DOD	10	Interrupt output, active low	Leave floating	Leave floating
D5	TW_N	DOD	10	Thermal warning output, active low	Leave floating	Leave floating
D6	VDDIO	PWR	15	Power supply for IO	Mandatory	Mandatory
E1	FBP1	AI	10	Positive remote sense input of CH1	Mandatory	Connect to GND
E2	AGND	GND	15	Ground of internal analog circuitry	Mandatory	Mandatory
E3	SCL	DI	15	I^2C clock	Mandatory - though can be connected to GND if I^2C control/monitoring is not required	Mandatory - though can be connected to GND if I^2C control/monitoring is not required
E4	SDA	DIOD	15	I^2C data	Mandatory - though can be connected to GND if I^2C control/monitoring is not required	Mandatory - though can be connected to GND if I^2C control/monitoring is not required
E5	CE	DI	10	Chip enable	Mandatory	Mandatory
E6	FBP2	AI	10	Positive remote sense input of CH2	Leave floating	Connect to GND
F1	AVDD	PWR	10	Power supply for internal analog circuitry	Mandatory	Mandatory
F2	PB_N	DOD	10	Power-bad output, active low	Leave floating	Leave floating
F3	CONF	DI	10	Configuration mode select (1Ch-4Ph or 2Ch-2Ph+2Ph)	Mandatory	Mandatory
F4	VSEL2	DI	10	External voltage control pin of CH2	In 1Ch-4Ph configuration, connect to AGND In 2Ch-2Ph+2Ph configuration, connect to GND	Connect to GND
F5	EN2	DI	10	Enable/disable input of CH2	In 1Ch-4Ph configuration, connect to AGND In 2Ch-2Ph+2Ph configuration, connect to GND	Connect to GND
F6	FBN2	AI	10	Negative remote sense input of CH2	Leave floating	Connect to GND
G1, H1, J1	VDD3	PWR	5000	Power supply for phase3	Mandatory	Connect to GND (no cap required)

Pin #	Pin Name	Type (Table 1)	Drive (mA)	Description	If Unused	
					1CH4PH Operation	2CH2PH Operation
G2, H2, J2	LX3	AIO	5000	LX node of phase3	Mandatory	Leave floating (L and Cout not required)
G3, H3, J3	GND3	GND	5000	Power ground of phase3	Mandatory	Mandatory
G4, H4, J4	GND4	GND	5000	Power ground of phase4	Mandatory	Mandatory
G5, H5, J5	LX4	AIO	5000	LX node of phase4	Mandatory	Leave floating (L and Cout not required)
G6, H6, J6	VDD4	PWR	5000	Power supply for phase4	Mandatory	Connect to GND (no cap required)

5. Conclusion

Adherence to the recommendations of this document helps minimize spurious application issues such as noise and increased current consumption and may avoid device damage due to incorrectly biased pins. For further information please consult your Renesas Electronics local sales representative.

Revision History

Revision	Date	Description
1.0	Nov 26, 2024	First version.
2.0	Mar 31, 2025	Section 4: Updated Pin Description

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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