Application Note

DA9292 PCB Layout Recommendations

AN-PM-189

Abstract

This application note provides recommendations on how to place and route DA9292 device. It also gives guidance on the passive components needed for proper functioning of the system. This document is a guideline only; target applications may have different requirements.

DA9292 PCB Layout Recommendations

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1 Terms and Definitions

FET	Field effect transistor
GND	Ground
GPIO	General purpose input or output
IC	Integrated circuit
PCB	Printed circuit board
WLCSP	Wafer level chip scale packaging

2 References

[1] DA9292, Datasheet, Dialog Semiconductor.

3 Introduction

Dialog Semiconductor's DA9292 device is power management IC with integrated power FETs, see datasheet [1]. DA9292 can be configured either as a single channel, quad-phase buck converter or as a two-channel, dual-phase buck converter.

The input voltage range of 2.2 V to 5.5 V makes it suited for a wide range of low voltage systems, including all single cell battery powered systems. The output voltage is programmable from 0.3 V to 1.275 V in 5 mV steps or from 0.6 V to 1.9 V in 10 mV steps.

The recommended components and connections for DA9292 in 1ch-4ph config is shown in Figure 1, 2ch-2ph config is shown in Figure 2.

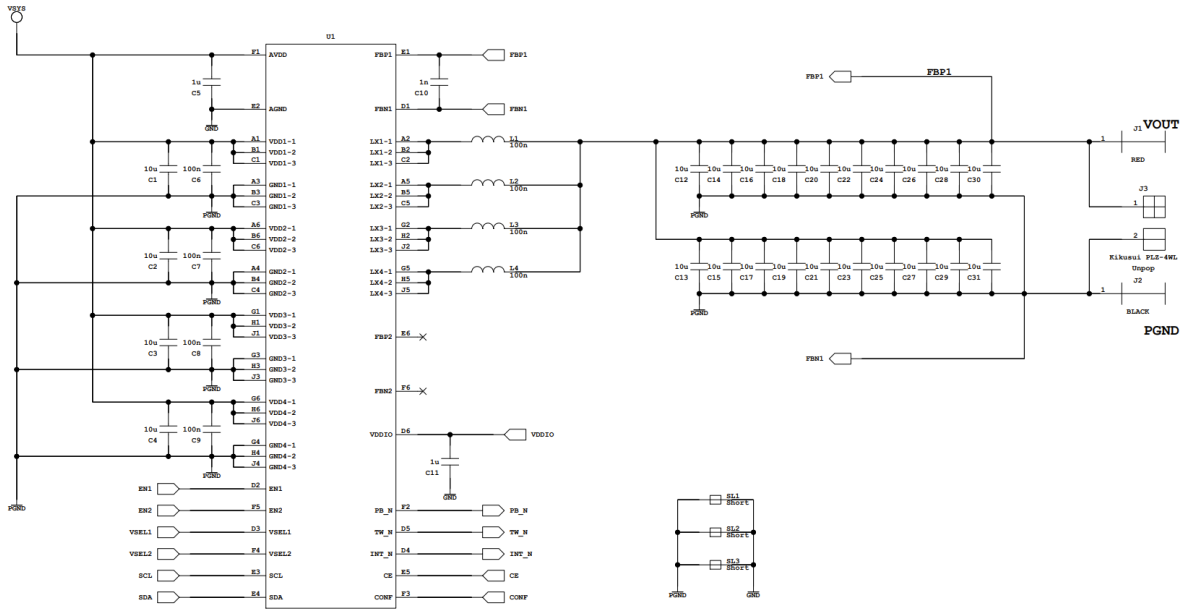


Figure 1: DA9292 Recommended Components and Connections (1ch-4ph)

Table 1: DA9292 Recommended Components (1ch-4ph)

Application	Part Reference	Value	Temp. Char.	Voltage Rating	ISAT and ITEMP
AVDD Bypass Cap	C5	1 µF	X5R or better	10 V or above	N/A
PVDD Bypass Cap	C1-C4	10 µF	X5R or better	10 V or above	N/A
PVDD Bypass Cap	C6-C9	100 nF	X5R or better	10 V or above	N/A
VOUT Bypass Cap	C12-31	10 µF	X5R or better	6.3 V or above	N/A
FB Bypass Cap	C10	1 nF	X5R or better	6.3 V or above	N/A
VDDIO Bypass Cap	C11	1 nF	X5R or better	6.3 V or above	N/A
Output Inductor	L1, L2, L3, L4	100 nH	N/A	N/A	13 A or above for per-phase maximum load current.

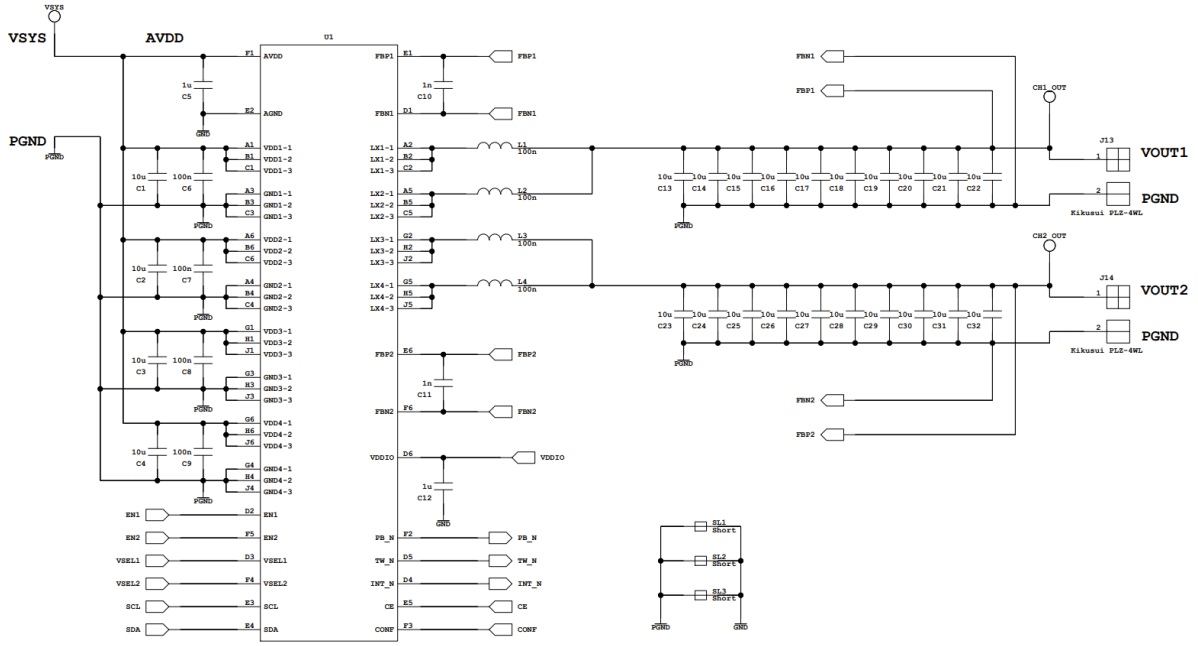


Figure 2: DA9292 Recommended Components and Connections (2ch-2ph)

Table 2: DA9292 Recommended Components (2ch-2ph)

Application	Part Reference	Value	Temp. Char.	Voltage Rating	ISAT and ITEMP
AVDD Bypass Cap	C5	1 µF	X5R or better	10 V or above	N/A
PVDD Bypass Cap	C1-C4	10 µF	X5R or better	10 V or above	N/A
PVDD Bypass Cap	C6-C9	100 nF	X5R or better	10 V or above	N/A
VOUT1 Bypass Cap	C13-C22	10 µF	X5R or better	6.3 V or above	N/A
VOUT2 Bypass Cap	C23-C32	10 µF	X5R or better	6.3 V or above	N/A
FB1 Bypass Cap	C10	1 nF	X5R or better	6.3 V or above	N/A
FB2 Bypass Cap	C11	1 nF	X5R or better	6.3 V or above	N/A
VDDIO Bypass Cap	C12	1 µF	X5R or better	6.3 V or above	N/A
Output Inductor	L1, L2, L3, L4	100 nH	N/A	N/A	13 A or above for per-phase maximum load current.

4 Layout Recommendations

DA9292 is packaged in a 54-pin WLCSP package with a 0.4 mm pitch.

Although the PCB layout recommendations described in this application note is with reference to the Dialog DA9292 Evaluation Board, a six-layer PCB, the required number of routing layers and other PCB parameters are also determined by the other devices in the system.

4.1 DA9292 Package Information

4.1.1 Ball Map

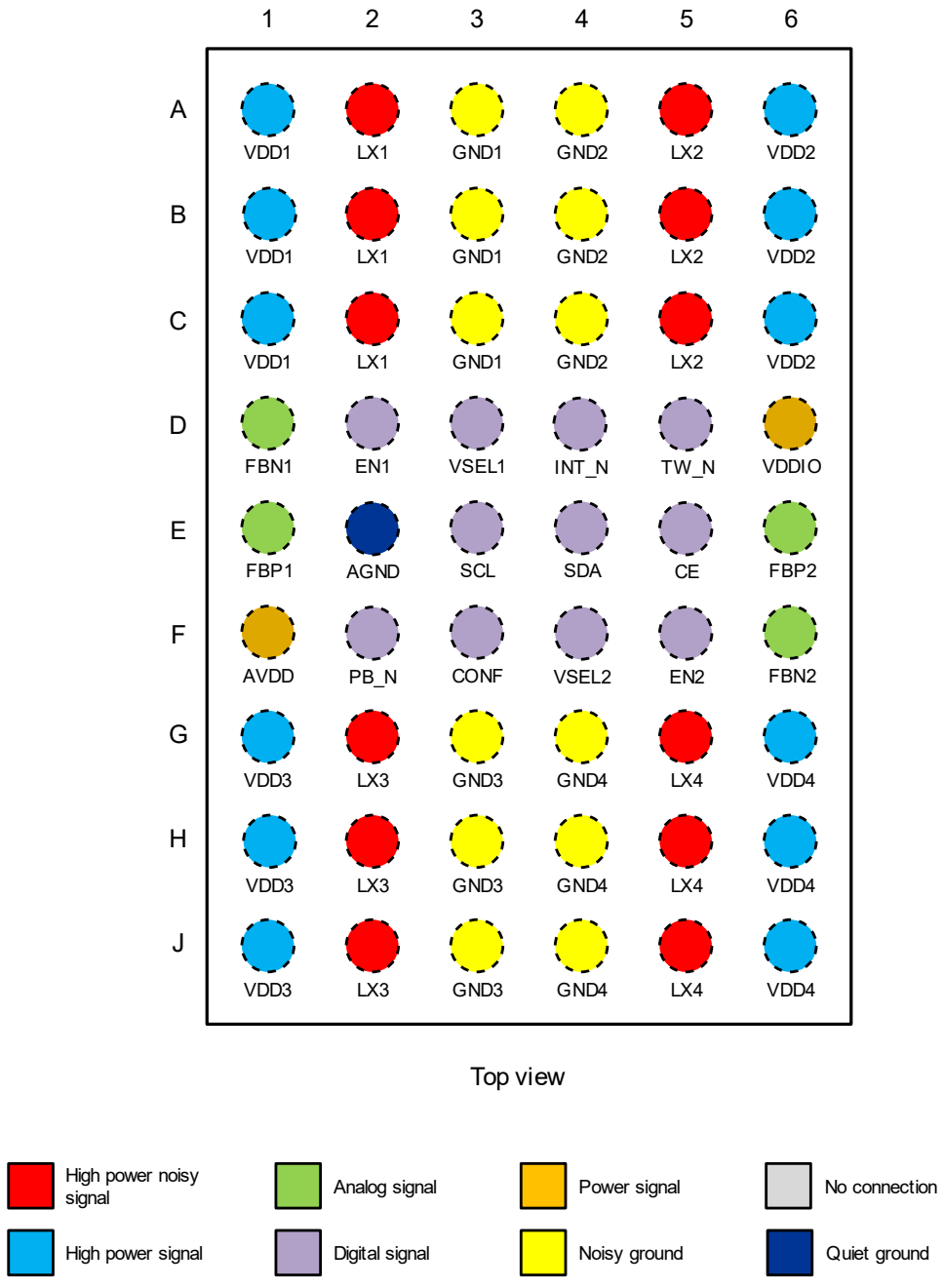


Figure 3: DA9292 Ball Map

4.1.2 Package Information

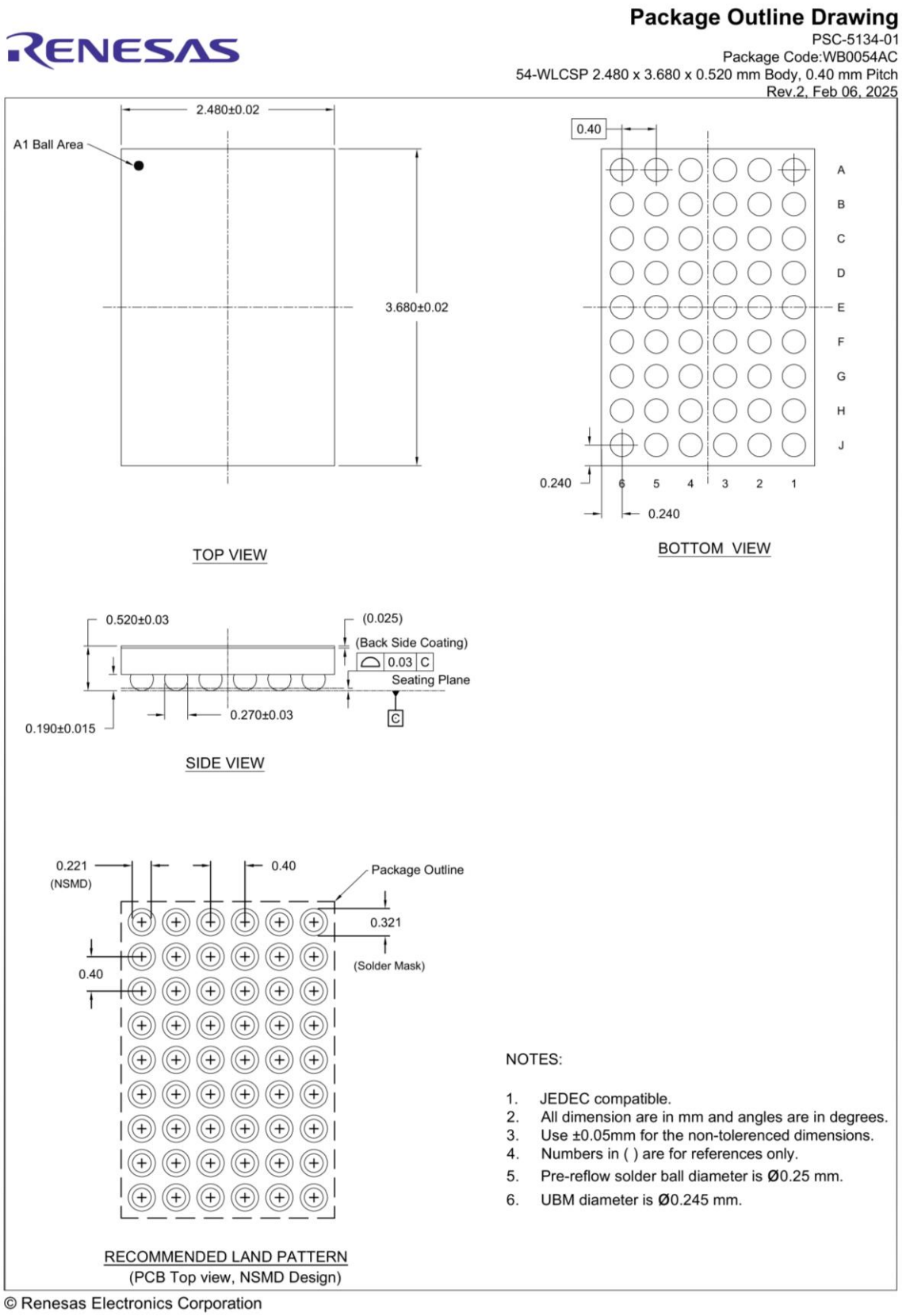


Figure 4: WLCSP6x9 Package Outline Drawing

4.2 Buck Converter

4.2.1 DA9292 Input

In a buck converter layout, the input capacitor location is critical. Locate the input capacitor as close as possible to the device's input and power GND pins to minimize the parasitic inductance.

In DA9292 layout design, the input capacitor for each phase should be placed as close as possible to the VDD<x> and GND<x> pins, and on the same layer as the DA9292 device.

If multiple layers are used, it is recommended to use as many as possible microvias (or through-hole vias) to minimize line resistance.

The DA9292 has a separate AVDD supply pin for the internal analog circuits. A 1 µF bypass capacitor should be placed close to the device's AVDD pin. The AVDD pin input and buck converter input (VDD<x>) share the same net, but it is important to separate these traces. Do not connect both traces directly on the same layer.

Ensure that the AVDD pin is connected to the input voltage (VSYS) plane far enough from the buck's input voltage so switching noise from the buck converter input (VDD<x> pins) is not injected to the AVDD pin.

Figure 5 shows the input capacitor placement and routing recommendation.

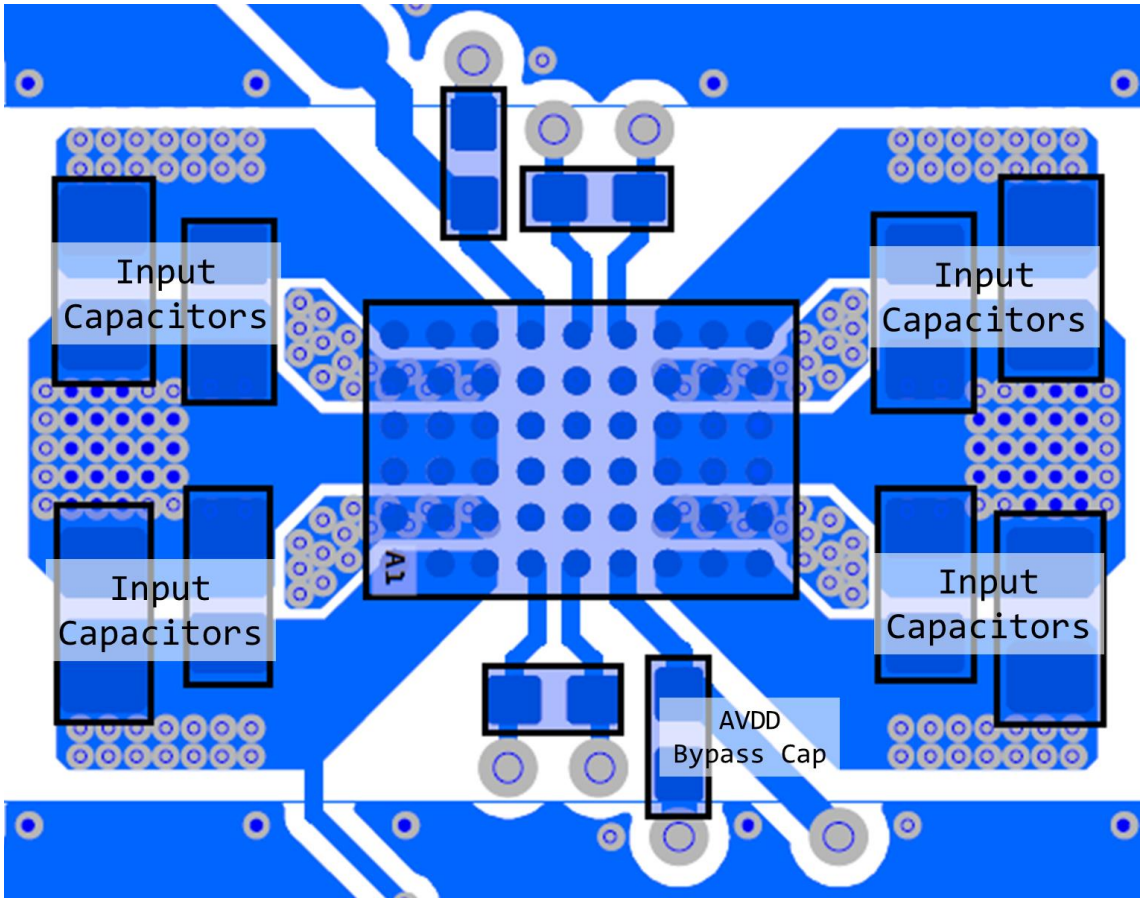


Figure 5: Recommended Input Capacitor Placement and Routing

4.2.2 Ground Connections

Special care should be taken with ground connections because of the high current capability of DA9292 and because of the device's high-performance requirements.

The power GND terminals (GND<x>) of the DA9292 are placed between each phase's LX pin.

It is best practice to isolate quiet analog GND (AGND) from noisy power GND terminals (GND<x>) and to connect them at a single point.

On Dialog's DA9292 Evaluation Board, AGND is isolated from the power GND terminals (GND<x>) at the top layer (component layer) and connected at a single point on the bottom layer.

Layer 2 can be used as a return power GND plane, where the device's power GND pins and output capacitor GND can be connected. It is recommended to minimize the line impedance of the power GND pins and output capacitor GND connections by using as many vias as possible. This will also improve the heat dissipation.

NOTE
It is always recommended to use copper plugged vias to achieve the minimum parasitic via impedance and best thermal performance.

Example of GND terminals connection is illustrated in Figure 6.

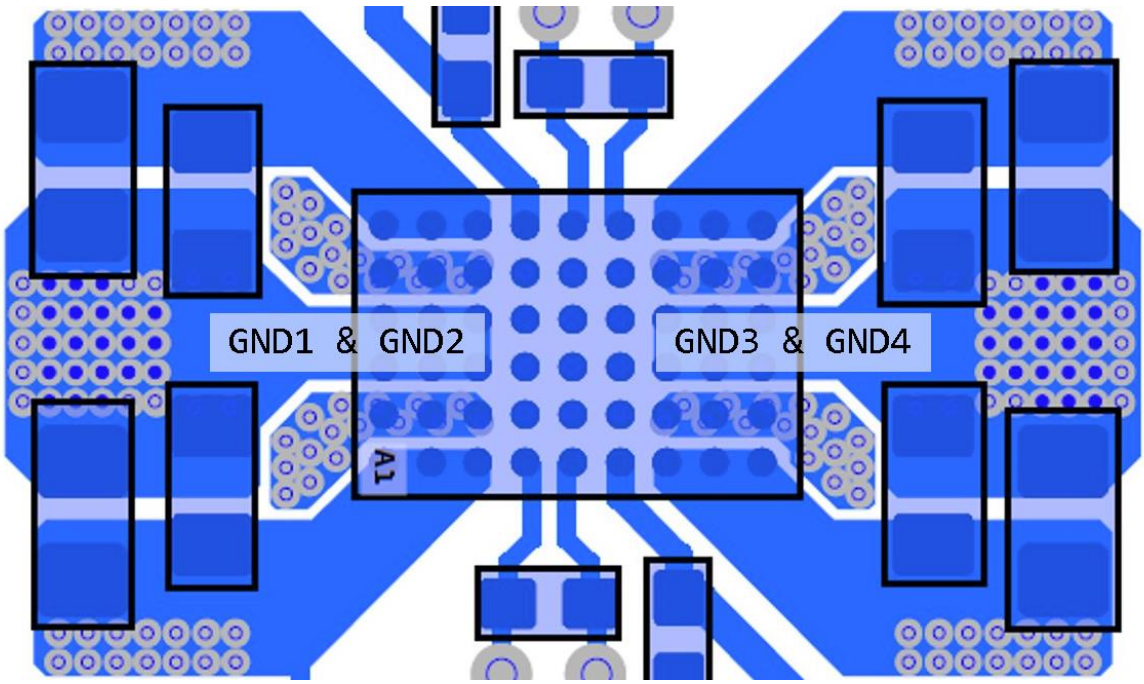


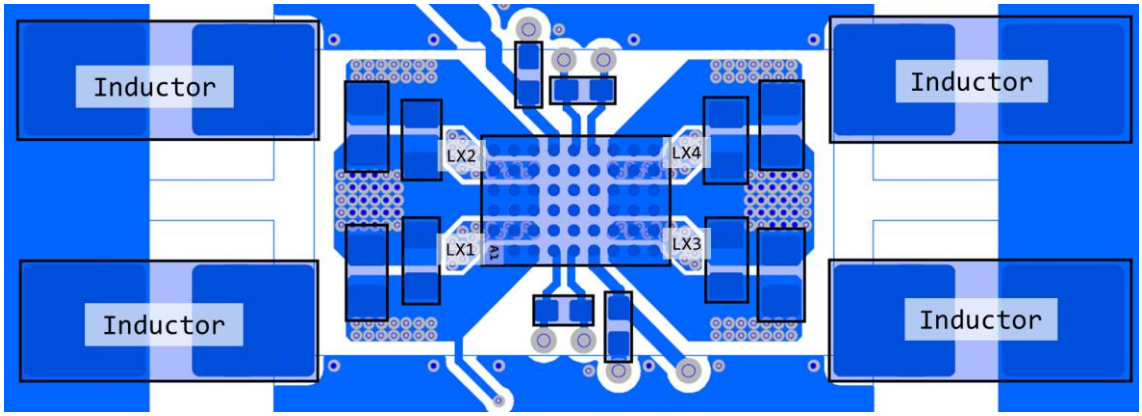
Figure 6: GND Terminals Connection

4.2.3 LX Routing

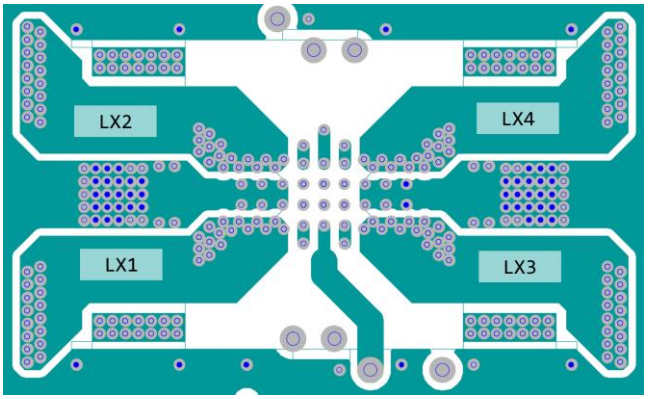
Switch node/LX node traces (traces between LX pins and output inductors) need to be kept as short as possible since this node generates switching noise, which can interfere with buck converter stability. Very high current will flow through these traces and so the minimum width of trace used for this LX node must be considered. Also, ensure that there are enough vias to deliver the current.

The LX node patterns on Dialog's DA9292 Evaluation Board are shown in Figure 7.

Layer 1



Layer 2



Layer 3

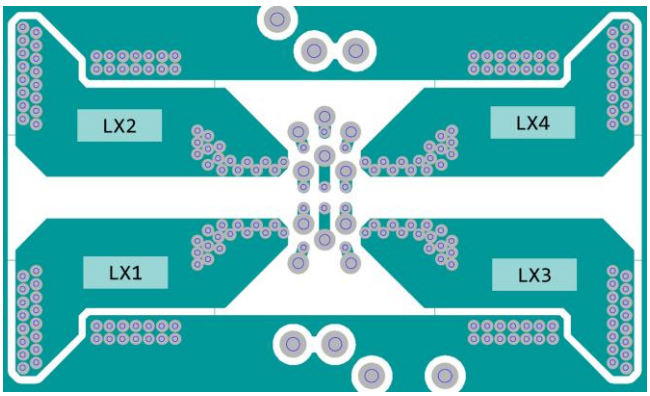


Figure 7: LX Node Pattern on DA9292 Evaluation Board

4.2.4 Buck Output

Output capacitors should be placed as close as possible to the load. Do not split the output capacitors into local capacitors (close to the output inductor) and remote capacitors (close to the load) as this may affect the stability of the buck converter.

However, minimizing the distance (which minimizes the line impedance) from the output inductors to the output capacitors (the load) is also important since it directly affects the efficiency and load transient response performance of the buck converter. Care must be taken with the size of the output traces to accommodate the high output current that DA9292 need to support.

It is best practice to transfer the output current at the top layer directly without using any vias. This will give the best performance in terms of efficiency and load transient response performance.

4.2.5 Feedback Lines

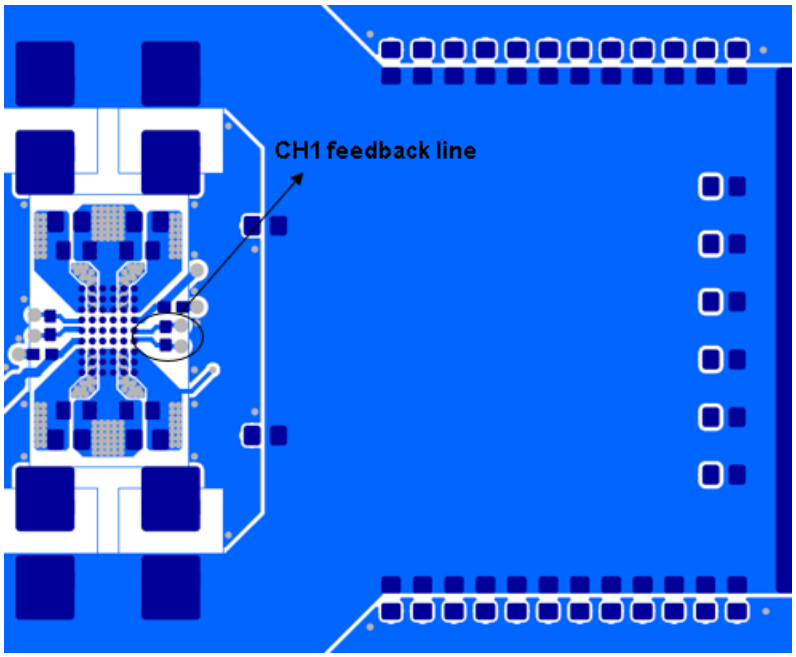
Feedback lines must be routed as a differential pair far from any noise source (for example, output inductors, LX node, and so on). It is strongly recommended to place a bypass capacitor (typically 1 nF) between the positive and negative sides of the differential feedback. The bypass capacitor should be placed as close as possible to the IC. It is useful for filtering noise which may be injected to the feedback lines due to a layout limitation (for example, a long feedback pattern or noise from other devices in the system).

Also, ensure that the feedback lines are not overlapping any noisy node traces (for example, the LX node trace) without an insulation plane in between.

NOTE
• The negative feedback trace is at ground potential and care should be taken not to connect any part of the trace to the ground plane. • The feedback lines must be routed directly from the load point in order to achieve the best voltage accuracy and stability.

Examples of output-voltage feedback-line routing, on the Dialog DA9292 Evaluation Board, is shown in Figure 8.

Layer 1



Layer 6

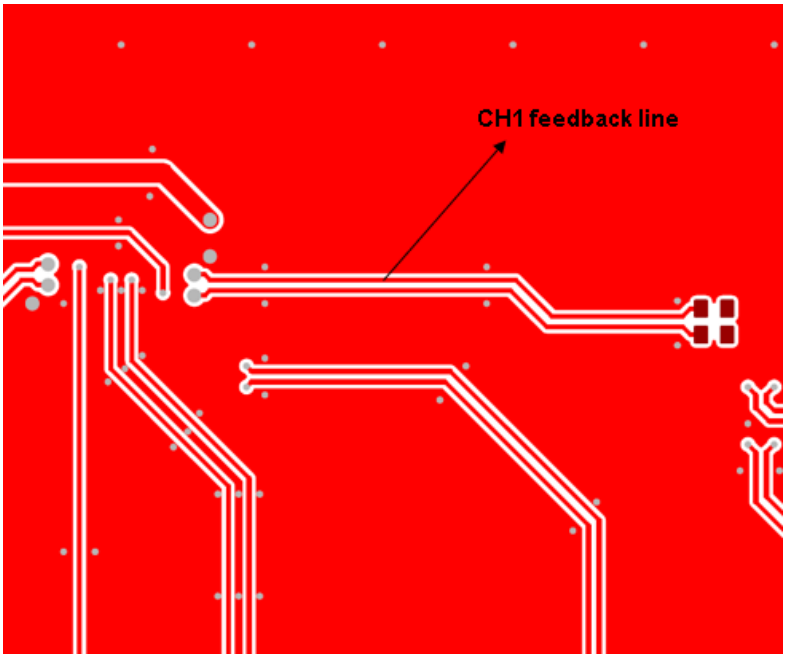


Figure 8: Output Voltage Feedback Line Routing on DA9292 Evaluation Board

4.3 Communication Interface (I^2C)

It is recommended to route the communication interface far from any noise source.

Care must also be taken regarding the noise produced by the interface signal in order to avoid coupling to the sensitive analog references and feedbacks. The routing layer is not critical, but it is recommended to use the bottom or top layer.

4.4 GPIO Signals

Generally, GPIOs have the lowest routing priority. Any layer can be used for routing these signals.

However, care must be taken regarding the noise produced by the GPIOs in order to avoid coupling to the sensitive analog references and feedbacks.

Revision History

Revision	Date	Description
1	18-Oct-2021	Initial version.
2	03-Apr-2025	Watermark removed and Figure 4 updated.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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