Application Note

DA9292-AKOVx Variant Overview

AN-PM-191

Abstract

This application note describes all the register default settings of the DA9292-AKOVx variant.

Contents

Tables

1 Terms and Definitions

CH	Channel
DVC	Dynamic voltage control
OTP	One Time Programmable
WLCSP	Wafer Lever Chip Scale Package

2 References

[1] DA9292_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3 Variant Table and Ordering Information

Table 1: Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9292-AKOV2	WLCSP 54L	2.48 x 3.68 x 0.4 mm pitch	Tape & Reel	10000
DA9292-APOVC				1000

4 DA9292-AKOVx Detailed Description - Production Release

4.1 CONF = AVDD (2CH2PH)

Key settings:

- 2CH2PH operation
- VCH1_LO = VCH1_HI = 0.3 V, VCH2_LO = VCH2_HI = 0.3 V
- CH1 & CH2 are OFF by default, CH1/2_EN functions enabled (EN1/2_PD enabled)
- CH1 & CH2 operate in PWM mode, 3 MHz
- I²C standard speed. I²C slave address = 0x6A (7-bit) / 0xD4 (8-bit)

Table 2: Register Settings DA9292-AKOVx Variant - CONF = AVDD (2CH2PH)

Register Address	Function	Default Value	Description
0x04	PMC_MASK_00	0xFF	IRQ events masked
0x05	PMC_MASK_01	0x07	IRQ events masked
0x06	PMC_CTRL_00	**0x01**	**Set to 2CH2PH**
0x07	PMC_CTRL_01	0x00	VCH1/2 range = 0.3 V to 1.275 V, CH1/2 PD enabled, VSEL1/2 low and EN1/2 disabled
0x08	PMC_CTRL_02	0x35	CH1 operates in Full Phase (2-phase), CH2 operates in 2-phase
0x09	PMC_CTRL_03	**0x55**	**CH1/2 operate in PWM mode**
0x0A	PMC_VOUT_CH1_00	**0x3C**	**VCH1_VSEL_LO = 0.3 V**
0x0B	PMC_VOUT_CH1_01	**0x3C**	**VCH1_VSEL_HI = 0.3 V**
0x0C	PMC_VOUT_CH2_00	**0x3C**	**VCH2_VSEL_LO = 0.3 V**
0x0D	PMC_VOUT_CH2_01	**0x3C**	**VCH2_VSEL_HI = 0.3 V**
0x0E	PMC_CFG_00	**0x33**	**EN1/2_EN functions enabled, EN1/2_PD enabled**
0x0F	PMC_CFG_01	**0x22**	**CH1/2_ILIM=12.5A**
0x10	PMC_CFG_02	0x00	VSEL1/2 debounce OFF
0x11	PMC_CFG_03	0x00	EN1/2 debounce OFF
0x12	PMC_CFG_04	0xFF	CH1/2 slew rate (startup/shutdown) is 5 mV/µs
0x13	PMC_CFG_05	0xFF	CH1/2 DVS slew rate (up/down) is 10 mV/µs
0x14	PMC_CFG_06	0xA0	I2C timeout enabled, Voutmax=1.275 V, OV masked, OC & PG not masked, PB configured as Power-Bad
0x15	PMC_CFG_07	0x04	Event flags are not cleared
0x16	PMC_CFG_08	**0x00**	**PB and TW are not configured**
0x17	PMC_CFG_09	0x50	PB debounce set to 10 µs, TW_N debounce is OFF
0x18	PMC_CFG_0A	**0xD4**	**I2C slave address is 0xD4 (8-bit) [0x6A (7-bit)] (standard/fast-mode)**

DA9292-AKOVx Variant Overview

Register Address	Function	Default Value	Description
0x1B	PMC_CFG_REV	0x0**A**	OTP variant: 0x0**A**(hex) = **10**(dec) is equivalent to A**K** (0=AA, 1=AB and 1**0**=A**K**)

5 DA9292-AKOVx Variant Overview

Table 3: OTP Variant Overview

Reg Add	Function	Standard Variant DA9292-AKOVx
		CONF = AVDD (2CH2PH)
0x04	PMC_MASK_00	0xFF
0x05	PMC_MASK_01	0x07
0x06	PMC_CTRL_00	**0x01**
0x07	PMC_CTRL_01	0x00
0x08	PMC_CTRL_02	0x35
0x09	PMC_CTRL_03	**0x55**
0x0A	PMC_VOUT_CH1_00	**0x3C**
0x0B	PMC_VOUT_CH1_01	**0x3C**
0x0C	PMC_VOUT_CH2_00	**0x3C**
0x0D	PMC_VOUT_CH2_01	**0x3C**
0x0E	PMC_CFG_00	**0x33**
0x0F	PMC_CFG_01	**0x22**
0x10	PMC_CFG_02	0x00
0x11	PMC_CFG_03	0x00
0x12	PMC_CFG_04	0xFF
0x13	PMC_CFG_05	0xFF
0x14	PMC_CFG_06	0xA0
0x15	PMC_CFG_07	0x04
0x16	PMC_CFG_08	**0x00**
0x17	PMC_CFG_09	0x50
0x18	PMC_CFG_0A	**0xD4**
0x1B	PMC_CFG_REV	**0x0A**

Revision History

Revision	Date	Description
1	15-Apr-2024	Initial version.
2	30-Aug-2024	Updated I2C slave address information in section 4.1.
3	03-Apr-2024	Updated section 3.

DA9292-AKOVx Variant Overview

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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DA9292-AKOVx Variant Overview

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