DA9217

DA9217-17V7x OTP Variant Overview

This application note describes all the register default settings of the DA9217-17V7x OTP variant (the x denotes the package option).

Contents

Contents **1**
Tables **1**
1. Terms and Definitions **2**
2. References **2**
3. Variant Table and Ordering Information **3**
4. DA9217-17V7x Detailed Description **4**
5. DA9217-17V7x Variant Overview **6**
6. Revision History **7**

Tables

Table 1. Ordering Information 3
Table 2. DA9217-17V7x, CONF=Low (I^2C Slave Address is 0x68 for 7-bits, 0xD0 for 8-bits) Register Settings 4
Table 3. DA9217-17V7x, CONF=High (I^2C Slave Address is 0x58 for 7-bits, 0xB0 for 8-bits) Register Settings 5
Table 4. DA9217-17V7x, CONF=Hi-Z (I^2C Slave Address is 0x60 for 7-bits, 0xC0 for 8-bits) Register Settings 5
Table 5. OTP Variant Overview 6

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1. Terms and Definitions

GPIO	General purpose input output
OTP	One-time programmable
DVC	Dynamic voltage control
WLCSP	Wafer-level chip-scale package

2. References

[1] DA9217 Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Variant Table and Ordering Information

Table 1. Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9217-17V72	24 WLCSP	2.48 x 1.68	T&R	4500
DA9217-17V76	24 WLCSP	2.48 x 1.68	Waffle Tray	140

4. DA9217-17V7x Detailed Description

Key settings:

- Single-channel dual-phase buck converter
- Maximum allowed output voltage set to 1.90 V
- Default operation mode set to Auto mode
- Soft start-up slew rate set to 10 mV/µs and active shutdown slew rate set to 20 mV/µs
- DVC ramp-up and ramp-down slew rate set to 20 mV/µs
- Current limit set to 5.5 A per-phase (peak inductor current)
- Chip configuration (CONF) feature enabled

Table 2. DA9217-17V7x, CONF=Low (I^2C Slave Address is 0x68 for 7-bits, 0xD0 for 8-bits) Register Settings

Register Address	Function	Default Value	Description
0x07	SYS_MASK_0	0x07	nIRQ interrupt, all masked
0x08	SYS_MASK_1	0xFF	nIRQ interrupt, all masked
0x09	SYS_MASK_2	0x07	nIRQ interrupt, all masked
0x0A	SYS_MASK_3	0x0F	nIRQ interrupt, all masked
0x0D	SYS_CONFIG_2	0x01	Over current latch-off function is disabled. PG is not masked during DVC. 1CH-2PH configuration.
0x0E	SYS_CONFIG_3	0x02	Oscillator tuning (OSC_TUNE) is off. I2C_TIMEOUT is enabled.
0x10	SYS_GPIO0_0	0x00	GPIO0 is set to CONF pin.
0x11	SYS_GPIO0_1	0x00	-
0x12	SYS_GPI01_0	0x00	GPIO1 is unused.
0x13	SYS_GPI01_1	0x00	-
0x14	SYS_GPI02_0	0x00	GPIO2 is unused.
0x15	SYS_GPI02_1	0x00	-
0x20	BUCK_BUCK1_0	0x49	CH1 is enabled by default. DVC ramp-up and ramp-down slew rate is set to 20 mV/µs.
0x21	BUCK_BUCK1_1	0x46	VOUT discharge resistor is enabled. Soft start slew rate is set to 10 mV/µs and shut-down slew rate is set to 20 mV/µs.
0x22	BUCK_BUCK1_2	0x05	ILIM is set to 5.5 A/phase.
0x23	BUCK_BUCK1_3	0xBE	Maximum output voltage is set to 1.9 V.
0x24	BUCK_BUCK1_4	0x0F	Buck is set to auto mode (both CH1_A_MODE and CH1_B_MODE). CH1_A_VOUT is selected by default.
0x25	BUCK_BUCK1_5	0xA5	CH1_A_VOUT = 1.65 V
0x26	BUCK_BUCK1_6	0xA5	CH1_B_VOUT = 1.65 V

Table 3. DA9217-17V7x, CONF=High (I^2C Slave Address is 0x58 for 7-bits, 0xB0 for 8-bits) Register Settings

Register Address	Function	Default Value	Description
0x07	SYS_MASK_0	0x07	nIRQ interrupt, all masked
0x08	SYS_MASK_1	0xFF	nIRQ interrupt, all masked
0x09	SYS_MASK_2	0x07	nIRQ interrupt, all masked
0x0A	SYS_MASK_3	0x0F	nIRQ interrupt, all masked
0x0D	SYS_CONFIG_2	0x01	Over current latch-off function is disabled. PG is not masked during DVC. 1CH-2PH configuration.
0x0E	SYS_CONFIG_3	0x02	Oscillator tuning (OSC_TUNE) is off. I2C_TIMEOUT is enabled.
0x10	SYS_GPIO0_0	0x00	GPIO0 is set to CONF pin.
0x11	SYS_GPIO0_1	0x00	-
0x12	SYS_GPI01_0	0x11	GPIO1 is set to power good. Push-pull configuration.
0x13	SYS_GPI01_1	0x00	-
0x14	SYS_GPI02_0	0x00	GPIO2 is unused.
0x15	SYS_GPI02_1	0x00	-
0x20	BUCK_BUCK1_0	0x49	CH1 is enabled by default. DVC ramp-up and ramp-down slew rate is set to 20 mV/µs.
0x21	BUCK_BUCK1_1	0x46	VOUT discharge resistor is enabled. Soft start slew rate is set to 10 mV/µs and shut-down slew rate is set to 20 mV/µs.
0x22	BUCK_BUCK1_2	0x05	ILIM is set to 5.5 A/phase.
0x23	BUCK_BUCK1_3	0xBE	Maximum output voltage is set to 1.9 V.
0x24	BUCK_BUCK1_4	0x0F	Buck is set to auto mode (both CH1_A_MODE and CH1_B_MODE). CH1_A_VOUT is selected by default.
0x25	BUCK_BUCK1_5	0x50	CH1_A_VOUT = 0.8 V
0x26	BUCK_BUCK1_6	0x50	CH1_B_VOUT = 0.8 V

Table 4. DA9217-17V7x, CONF=Hi-Z (I^2C Slave Address is 0x60 for 7-bits, 0xC0 for 8-bits) Register Settings

Register Address	Function	Default Value	Description
0x07	SYS_MASK_0	0x07	nIRQ interrupt, all masked.
0x08	SYS_MASK_1	0xFF	nIRQ interrupt, all masked.
0x09	SYS_MASK_2	0x07	nIRQ interrupt, all masked.
0x0A	SYS_MASK_3	0x0F	nIRQ interrupt, all masked.
0x0D	SYS_CONFIG_2	0x01	Over current latch-off function is disabled. PG is not masked during DVC. 1CH-2PH configuration.
0x0E	SYS_CONFIG_3	0x02	Oscillator tuning (OSC_TUNE) is off. I2C_TIMEOUT is enabled.
0x10	SYS_GPIO0_0	0x00	GPIO0 is set to CONF pin.
0x11	SYS_GPIO0_1	0x00	-
0x12	SYS_GPI01_0	0x00	GPIO1 is unused.
0x13	SYS_GPI01_1	0x00	-
0x14	SYS_GPI02_0	0x00	GPIO2 is unused.
0x15	SYS_GPI02_1	0x00	-
0x20	BUCK_BUCK1_0	0x49	CH1 is enabled by default. DVC ramp-up and ramp-down slew rate is set to 20 mV/µs.
0x21	BUCK_BUCK1_1	0x46	VOUT discharge resistor is enabled. Soft start slew rate is set to 10 mV/µs and shut-down slew rate is set to 20 mV/µs.
0x22	BUCK_BUCK1_2	0x05	ILIM is set to 5.5 A/phase.
0x23	BUCK_BUCK1_3	0xBE	Maximum output voltage is set to 1.9 V.
0x24	BUCK_BUCK1_4	0x0F	Buck is set to auto mode (both CH1_A_MODE and CH1_B_MODE). CH1_A_VOUT is selected by default.
0x25	BUCK_BUCK1_5	0xA5	CH1_A_VOUT = 1.65 V

Register Address	Function	Default Value	Description
0x26	BUCK_BUCK1_6	0xA5	CH1_B_VOUT = 1.65 V

5. DA9217-17V7x Variant Overview

Table 5. OTP Variant Overview

Register Address	Function	CONF=Low I²C Slave Address: 0x68 (7-bits)	CONF=High I²C Slave Address: 0x58 (7-bits)	CONF=Hi-Z I²C Slave Address: 0x60 (7-bits)
0x07	SYS_MASK_0	0x07	0x07	0x07
0x08	SYS_MASK_1	0xFF	0xFF	0xFF
0x09	SYS_MASK_2	0x07	0x07	0x07
0x0A	SYS_MASK_3	0x0F	0x0F	0x0F
0x0D	SYS_CONFIG_2	0x01	0x01	0x01
0x0E	SYS_CONFIG_3	0x02	0x02	0x02
0x10	SYS_GPIO0_0	0x00	0x00	0x00
0x11	SYS_GPIO0_1	0x00	0x00	0x00
0x12	SYS_GPI01_0	**0x00**	**0x11**	**0x00**
0x13	SYS_GPI01_1	0x00	0x00	0x00
0x14	SYS_GPI02_0	0x00	0x00	0x00
0x15	SYS_GPI02_1	0x00	0x00	0x00
0x20	BUCK_BUCK1_0	0x49	0x49	0x49
0x21	BUCK_BUCK1_1	0x46	0x46	0x46
0x22	BUCK_BUCK1_2	0x05	0x05	0x05
0x23	BUCK_BUCK1_3	0xBE	0xBE	0xBE
0x24	BUCK_BUCK1_4	0x0F	0x0F	0x0F
0x25	BUCK_BUCK1_5	**0xA5**	**0x50**	**0xA5**
0x26	BUCK_BUCK1_6	**0xA5**	**0x50**	**0xA5**

6. Revision History

Revision	Date	Description
01.01	Feb 19, 2025	Conversion to new template
01.00	Apr 09, 2024	First version.

STATUS DEFINITIONS

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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