# Application Note

## DA9061 / NXP i.MX 6UL / ULL Power Connections

### AN-PM-101


## Abstract

*This document describes the connectivity between the Dialog Semiconductor DA9061 Power Management Integrated Circuit (PMIC) and NXP i.MX 6UL/6ULL system application processors.*

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# 1 Terms and Definitions

| | |
|---|---|
| GUI | Graphical User Interface |
| PMIC | Power Management Integrated Circuit |
| DVC | Dynamic Voltage Control |
| DVS | Dynamic Voltage Scaling. Analogous to DVC. |
| POR | Power-On Reset |
| RTC | Real-Time Clock |
| SNVS | Secure Non-Volatile Storage |

# 2 References

[1] i.MX 6UL Applications Processors for Industrial Products, Datasheet, IMX6ULIEC Rev. 2.2, 05/2017, NXP.

[2] i.MX 6ULL Applications Processors for Industrial Products, Datasheet, IMX6ULLIEC Rev. 1.1, 05/2017, NXP.

[3] i.MX 6UL Applications Processor Reference Manual, IMX6ULRM, Rev. 0, 04/2016, NXP

[4] i.MX 6ULL Applications Processor Reference Manual, IMX6ULLRM, Rev. 0, 09/2016, NXP

[5] Common Hardware Design for i.MX 6Dual/6Quad and i.MX 6ULL, AN4397, Rev. 2, 07/2015, NXP

[6] Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors, IMX6DQ6SDLHDG, Rev 1, 06/2013, NXP

[7] DA9061, Datasheet, Dialog Semiconductor

[8] Schematic, DA9061_iMX6UL_Schematic_1v0.pdf, Dialog Semiconductor

[9] Schematic, DA9061_iMX6ULL_Schematic_1v0.pdf, Dialog Semiconductor

[10] The Linux Kernel Archives, https://kernel.org/ (DA9061 Software Driver) [Accessed 30/3/2016]

 

# 3 Introduction

The NXP® i.MX 6UL™ and i.MX 6ULL™ processors require dedicated power management for a stable and reliable system. The Dialog DA9061 PMIC provides a convenient and flexible solution that meets the processor power requirements. Although system power consumptions vary due to the differing demands of peripherals, processor, and so on, the DA9061 has sufficient headroom to meet the power requirements of most i.MX 6UL/6ULL systems. The features of DA9061 enable significant power saving, such as dynamic voltage control (DVC) which intelligently manages voltage changes. The DA9061 significantly reduces system cost and size compared to an equivalent discrete solution.

This document provides details of integrating the DA9061 into an i.MX 6UL or 6ULL system. General guidance can be found in the NXP references listed in Section 2.

# 4 i.MX 6UL/6ULL Power Requirements

All power domains of an i.MX 6 processor require precise power management to ensure reliable system operation. The main domains are:

VDD_SOC_IN supplies the internal peripherals and the internal ARM™ cores

VDD_HIGH_IN supplies PLLs, DDR pre-drivers, PHY and miscellaneous circuitry

VDD_SNVS_IN supplies the SNVS regulator for the RTC and SNVS (secure non-volatile storage)

Additional supplies may be required for DDR memory, peripherals, I/O interfaces, USB, and so on. The power management system must also comply with the processor power-up and power-down sequence requirements.

## 4.1 i.MX 6UL/6ULL Power Rails

Table 1 summarizes the supply rails of the NXP i.MX 6UL processor and the corresponding regulator outputs from the DA9061.

To optimize systems without a coin cell, VDD_SNVS_IN and VDD_HIGH_IN are tied together and supplied by LDO2 at 3.0 V. These rails are powered up first in the sequence.

**Table 1: i.MX 6UL/6ULL to DA9061 Power Rail Mapping**

| i.MX 6UL/ULL Rail or System Rail | DA9061 Regulator | Voltage (V) | Sequence Slot | Notes |
|---|---|---|---|---|
| VDD_HIGH_IN, VDD_SNVS_IN | LDO2 | 3.0/3.3 | 1 | Switchable via GPIO3 between 3.0 V and 3.3 V |
| VDD_SOC_IN | Buck1 | 1.40 | 2 | Default for Run Mode with VDD_SOC LDO enabled.<br>DVC to 1.2V for 6ULL Low Power RUN Mode<br>DVC to 1.0V for SUSPEND Mode |
| NVCC_DRAM (VDDQ_DDR) | Buck3 | 1.5/1.35 | 3 | Switchable via GPIO2 to support DDR3 and DDR3L |
| NVCC<x> | Buck2 | 3.3 | 4 | The NVCC_<x> digital I/O supply grouping is application specific |
| Peripherals | LDO3 | 1.8 | 5 | General purpose rail, for example, supply for RGMII I/O group |
| Peripherals | LDO4 | 1.2 | 6 | General purpose rail |
| Peripherals | LDO1 | 2.5 | 7 | General purpose rail |

The above mapping is illustrated in the interconnect block diagram of Figure 1.

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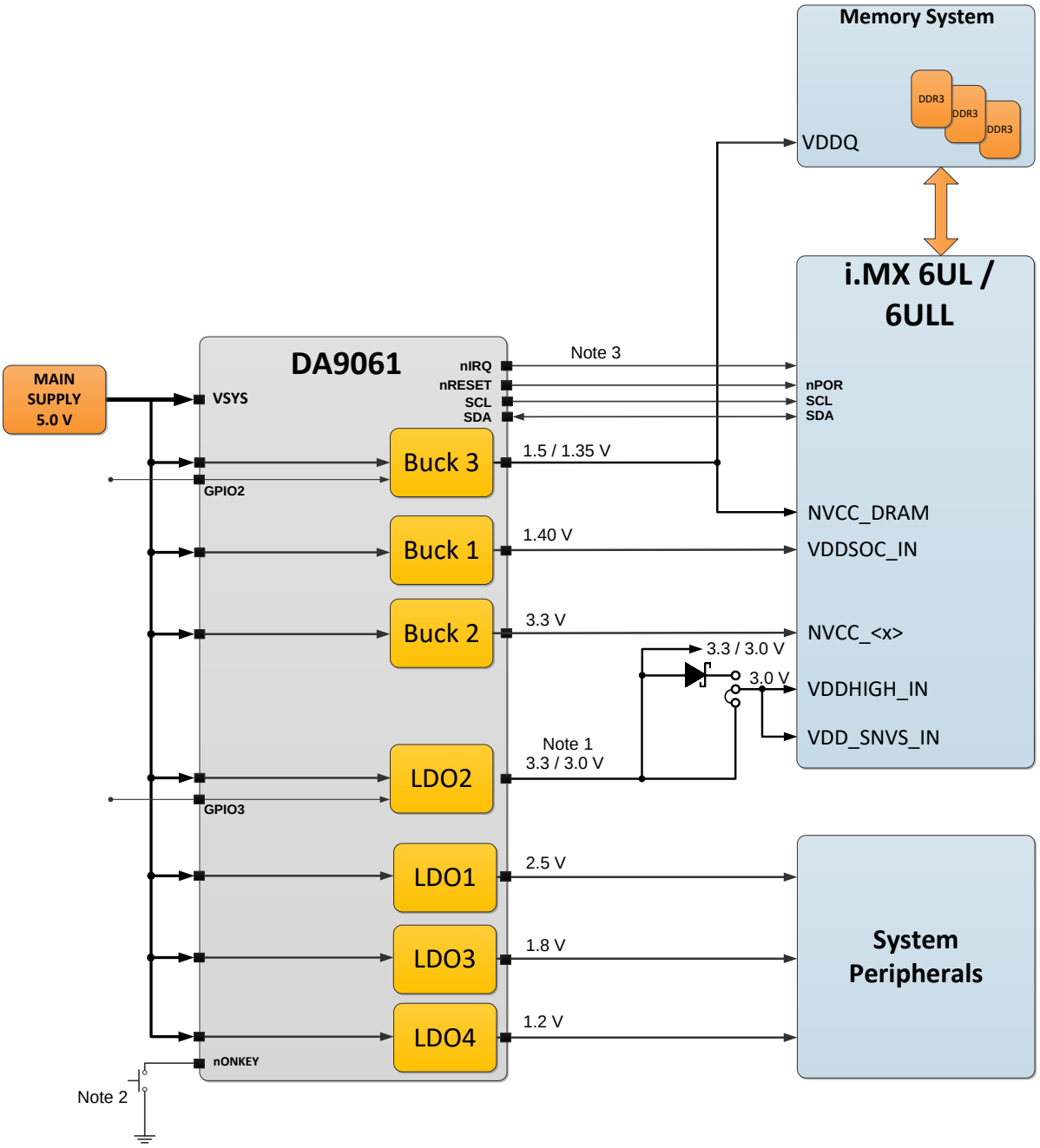


**Figure 1: DA9061 Connections to i.MX 6UL/6ULL**

**Note 1** LDO2 is switchable between 3.0 V and 3.3 V based on GPIO3 level. Since no battery is used, VDD_SNVS_IN is shorted to VDDHIGH_IN, as described in [1] and [2] Section 4.2.1. If LDO2 is set to 3.3 V (for example to drive a system peripheral), then the diode is required to reduce the voltage on VDDHIGH_IN/VDD_SNVS_IN.

**Note 2** DA9061-66 has the autoboot function enabled in OTP. The DA9061-67 has autoboot disabled and is therefore suited for systems requiring an ONKEY wake-up.

**Note 3** Pull-up resistors for open-drain lines are not shown.

The voltage for VDD_SOC_IN has been set in OTP as 1.40 V. For PCB layouts that have significant ohmic drops along these supply rails, the losses can be compensated for by increasing the level, to 1.44 V for example. This is achieved by an $I^2C$ software write to DA9061 control VBUCK1_A immediately after system power-up.

## 4.2 Power-Up Sequence

The sequence used by the DA9061 standard variants, DA9061-66 and DA9061-67, conforms to the requirements described in the i.MX 6UL/6ULL datasheets [1], [2] and reference manuals [3], [4], with specific details highlighted in Table 2.

**Table 2: i.MX 6UL/6ULL Sequencer Requirements**

| Requirements in i.MX 6UL/6ULL Datasheets [1], [2] and Reference Manuals [3], [4] | DA9061 Configuration Notes |
|---|---|
| VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply. | VDD_SNVS_IN must be supplied by a coin cell or shorted to VDD_HIGH_IN. In either case, VDD_SNVS should be turned on before any other supply. LDO2 is sequenced in Slot 1 to support this. |
| If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on. | No resulting requirement for DA9061. |
| If the external SRC_POR_B signal is used to control the processor POR, SRC_POR_B must remain low (asserted) until the VDD_ARM_CAP and VDD_SOC_CAP supplies are stable. | For 6UL/6ULL, VDD_SOC_IN is shorted and the delay for the POR_B pin is required. The delay is provided by the DA9061 sequencer delay for nRESET (register RESET at address 0x99). |
| If the external SRC_POR_B signal is not used (always held high or left unconnected), the processor defaults to the internal POR function (where the PMU controls generation of the POR based on the power supplies). If the internal POR function is used, the following power supply requirements must be met:<br>● VDD_ARM_IN and VDD_SOC_IN may be supplied from the same source, or, VDD_SOC_IN can be supplied before VDD_ARM_IN with a maximum delay of 1 ms.<br>● VDD_ARM_CAP must not exceed VDD_SOC_CAP by more than +50 mV. | The DA9061 reference design does use POR_B, so this is irrelevant. (VDD_ARM_IN is internally supplied from VDD_SOC_IN.) |
| NOTE: The SRC_POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the SRC_POR_B input, the internal POR module takes control. See the i.MX 6UL/6ULL reference manuals for further details and to ensure that all necessary requirements are being met. | The DA9061 design uses POR_B with a delay, as mentioned above.<br>POR_B is asserted by the DA9061 immediately when system power is supplied. It is released after all sequenced supplies reach their final stable voltages. Other system components may also assert POR_B, as illustrated in the schematic [8] as wdog2_WDOG. |
| NOTE: Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies). | No resulting requirement for DA9061. |
| NOTE: USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time. | No resulting requirement for DA9061. |

Figure 2 shows the power-up sequence generated by the DA9061-66, which meets the i.MX 6UL/6ULL start-up requirements.

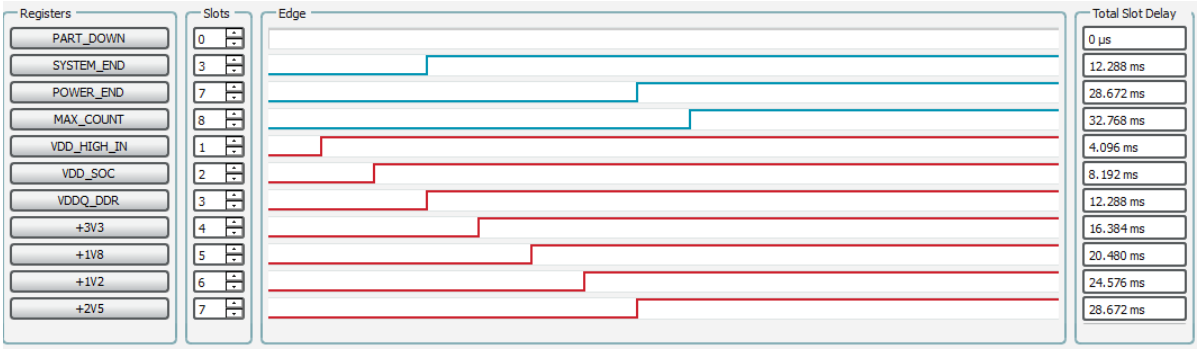


**Figure 2: DA9061 Power-Up Sequence**

### 4.3 Power-Down Sequence

There are no requirements specific to power-down. Restrictions for other supplies are discussed in [1], [2].

### 4.4 I²C Interface

An I²C interface between the i.MX 6 and the DA9061 device allows software, including the operating system kernel, to access the internal PMIC registers for control and monitoring. The slave address of the DA9061 is 0xB0.

### 4.5 Recommended External Components

For a list of recommended external components, please refer to the schematic [8], [9] and the DA9061 datasheet [7]. The recommended values of inductors and capacitors must be used at the output of all bucks and LDOs to guarantee the closed-loop stability and optimum efficiency of the supplies.

## 5 Scalable Power Management Solutions

Some systems require more regulators than available from the DA9061. This is frequently due to the demands of the peripherals. In these circumstances, other Dialog PMICs in the same family (for example, DA9062, DA9063, and DA9063L) are likely to provide suitable solutions. The DA9062 is pin-compatible with the DA9061 and provides additional features often required by i.MX 6 systems such as a real-time clock (RTC), a dual-phase (5 A) buck configuration, DDR memory termination (DA9062 VTT supply), and VTTR memory reference voltage.

## 6 Software Driver

After the DA9061 has started the i.MX 6 system, software can read and write to the PMIC via the I²C bus. This can be used for further PMIC configuration, such as the GPIOs, interrupt servicing, DVC, watchdog keep-alive writes, and so on. Dialog drivers for Linux™ are available in the Linux kernel from https://kernel.org/ [10] or, if interim assistance is required, from a Dialog Sales representative.

# 7 Development Support Tools and PMIC Configuration Files

To assist with hardware and software development, Dialog provides the following:

- DA9061 evaluation kit

This contains motherboard and daughterboard for hardware evaluation and software development. It also includes the SmartCanvas™ GUI software.

- SmartCanvas GUI

This PC-driven software provides easy access to a device under test (DUT). The GUI is used to exercise the DUT using the $I^2C$ interface. Control or measurement of analog and digital pins is supported. SmartCanvas supports the Dialog PMIC OTP configuration file format – .ini files.

- OTP configuration .ini files

These files define the configuration of the DA9061 at boot and define the different variants such as the -66 and -67. The following ini files are available from the Dialog Support Site:

  - DA9061-66_IMX6UL_AUTOBOOT_0v1_1B54.ini (autoboot enabled)
  - DA9061-67_IMX6UL_NO_AUTOBOOT_0v1_BD9B.ini (autoboot disabled)

These files are opened using the SmartCanvas GUI. They are applicable to both the 6UL and 6ULL processors.

- Design schematic [8] with details of PMIC to processor interconnections
- Linux software driver, see Section 6

# 8 Device Identification and Ordering

DA9061-66 has the autoboot feature enabled in OTP. The DA9061-67 has autoboot disabled and is therefore suited for systems requiring an ONKEY wake-up. If the DA9061-66 and DA9061-67 prove unsuitable for your target i.MX 6UL/6ULL design, please contact a Dialog sales representative to discuss custom variants (minimum order quantities apply for custom variants.)

**Table 3: Product Part Numbers**

| Part Number | Description (Note 1) |
|---|---|
| DA9061-66AMx | Autoboot. Industrial grade |
| DA9061-66AMx-A | Autoboot. Automotive AEC-Q100 Grade 2 |
| DA9061-67AMx | Non-autoboot. Industrial grade |
| DA9061-67Mx-A | Non-autoboot. Automotive AEC-Q100 Grade 2 |

**Note 1** See the DA9061 datasheet [7] for further information regarding part ordering. All parts are available in tray (x = 1) or Tape & Reel (x = 2).

## Revision History

| Revision | Date | Description |
|---|---|---|
| 1.1 | 25-Feb-2022 | File was rebranded with new logo, copyright and disclaimer |
| 1.0 | 20-Nov-2017 | First release. |

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## Status Definitions

| Status | Definition |
|---|---|
| DRAFT | The content of this document is under review and subject to formal approval, which may result in modifications or additions. |
| APPROVED or unmarked | The content of this document has been approved for publication. |

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