Digital Phase-Lock-Loop (DPLL) Evaluation
SLG47011V

Abstract

This application note describes how to implement a general Digital Phase-Loop-Lock (DPLL) using the Renesas SLG47011V.

A DPLL, as shown in Figure 1, is used to synchronize and generate stable and adjustable clock signals. A frequency divider (F_divider) is used to scale up the input frequency f_in, which is then sent to a Phase-Detector which compares the phase of the output signal f_out / M with the phase of the input reference frequency f_ref. A Digital Filter then filters the phase error (ΔPhase) to a digitally controlled oscillator (DCO) which generates the corresponding frequency f_out.

The SLG47011 is comprised of the adequate and specific digital macrocells needed to synthesize a DPLL according to this model. Each specific function in this basic DPLL structure is implemented by the macrocells available in the SLG47011 to implement the DPLL's functionality.

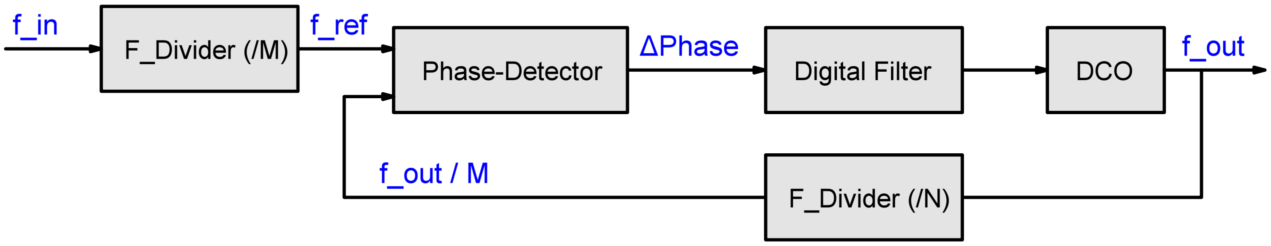

Figure 1. Basic Digital PLL Structure Diagram.

Contents

1. Terms and Definitions

CNT/DLY	Counter and Delay
DPLL	Digital Phase-Loop-Lock
DCO	Digital-Controlled Oscillator
LUT	Look Up Table
MCC	Memory Counter Control
NCO	Numerical Clock Oscillator
LUT	Look Up Table
I2C	Inter-Integrated Circuit
PGA	Programmable Gain Amplifier
I2C	Inter-Integrated Circuit
SOC	State of Charge

2. References

For related documents and software, please visit:

AnalogPAK | Renesas

Download our free Go Configure Software hub [1] to open the [2] design files and view the proposed circuit design. Use the AnalogPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes.

[1] Go Configure Software Hub | Renesas

[2] AN-CM-428 Digital Phase-Lock-Loop (DPLL) Evaluation.app, ANalogPAK Design File, Renesas Electronics

[3] SLG47011 - AnalogPAK Programmable Mixed-Signal IC | Renesas, AnalogPAK Development tools, Renesas Electronics

[4] Application notes library, Renesas Electronics

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3. Introduction

The SLG47011V is comprised of a diverse collection of digital and analog marcocells for analog front end (AFE) applications. In particular, the SLG47011's 14-bit SAR ADC and 4-channel PGA (see Figure 2) are used to perform AFE signal capturing. The PGA is capable of operating in several configurations (such as single-ended mode and differential mode) and the reference voltages used by the PGA and ADC can be configured independently as needed. The ADC supports resolutions ranging from 8 bits to 14 bits. Moreover, the SLG47011 offers four Buffer blocks in which averaging and over-sampling functions can be used to process ADC data. These digital macrocells can achieve the extended functionality needed for a DPLL used in AFE applications.

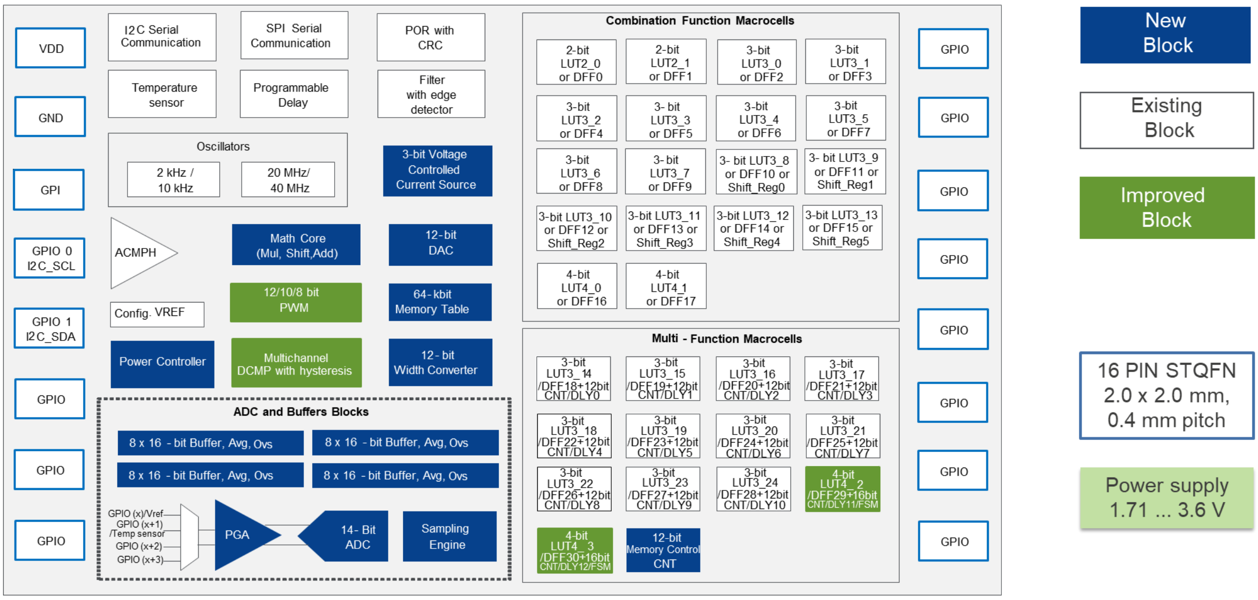


Figure 2. SLG47011 Block Diagram

4. Design

Figure 3 shows the final DPLL AnalogPAK design, which is comprised of several blocks providing the required functions listed:

1. Input (Divided) Frequency: A SHR macrocell is used to reduce input frequency F_IN.
2. Phase Detector: This is a simple phase detector consisting of a few basic macrocells.
3. MCC Clock Source (F_{MCC}) to Toggle a U/P Counter: This block is used for setting the required loop bandwidth.
4. Damping-Compensator to the U/P Counter: The block is used to decrease the damping to the U/P Counter.
5. U/P Counter: The counter acts as an accumulator to track the duration of UP and Down signals.
6. NCO (Numerical): For DCO synthesis, the Memory Table provides the specific numerical processing that gives the corresponding data equivalent to the frequency value. The next stage is a counter (CNT9) to generate the frequency F_OUT.
7. Feedback Divided Frequency: A SHR macrocell is used to reduce output frequency.
8. Boost Response: Used to monitor both the input and output frequency for boosting of the response of the U/P counter.
9. NCO Data Monitor: In this case, the Mathcore and DAC are integrated to present the Memory Table data directly.

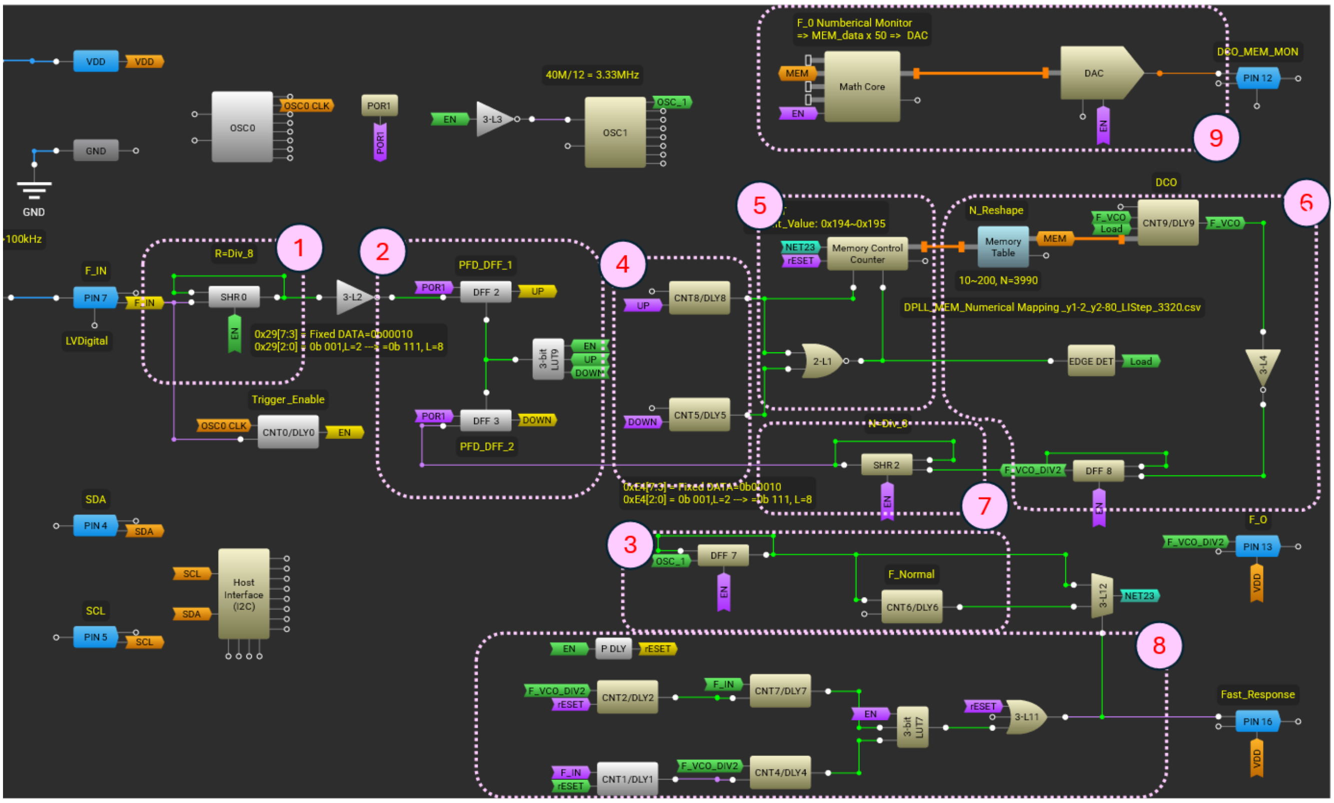


Figure 3. DPLL GP Design.

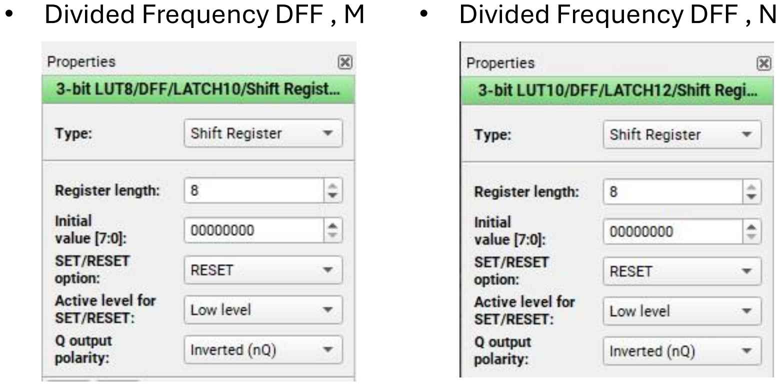
In this design, we use the input frequency condition range:

Minimum F_IN frequency = 300 kHz

Maximum F_OUT frequency =1.5 MHz

To generate a different output frequency, we can change the "N/M" divider ratio between the Divided Frequency blocks. The register length of both of the Input & Feedback Divided Frequency DFFs can be assigned with the required ratio. Figure 4 shows the configuration used.

In this design, the M and N values are set to '8' in both divided frequency DFF macrocells.



- Divided Frequency DFF , M

Properties

3-bit LUT8/DFF/LATCH10/Shift Regist...

Type: Shift Register

Register length: 8

Initial value [7:0]: 00000000

SET/RESET option: RESET

Active level for SET/RESET: Low level

Q output polarity: Inverted (nQ)

- Divided Frequency DFF , N

Properties

3-bit LUT10/DFF/LATCH12/Shift Regi...

Type: Shift Register

Register length: 8

Initial value [7:0]: 00000000

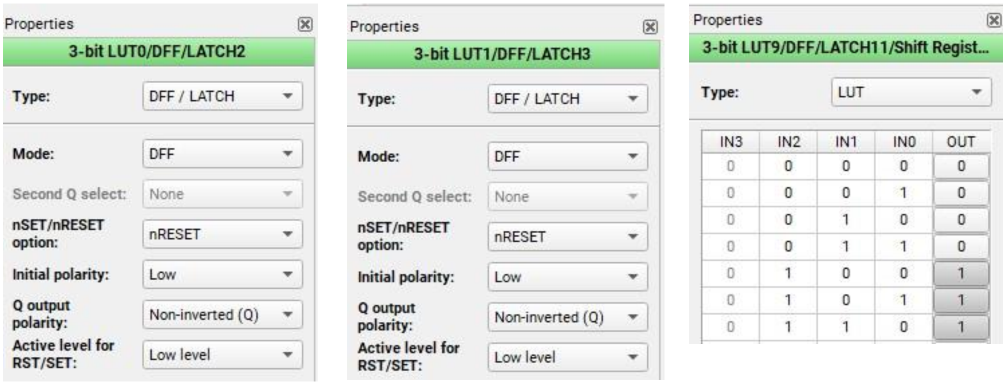
SET/RESET option: RESET

Active level for SET/RESET: Low level

Q output polarity: Inverted (nQ)

Figure 4. Dual SHR Configuration of the Frequency Divider Ratio.

The **Phase Detector** is the simplest logic circuit in the design. Figure 5 shows the configuration used. It outputs the phase difference between the input and the feedback frequency signal. The PLL adjusts the output frequency by the phase variation.



Properties

3-bit LUT0/DFF/LATCH2

Type: DFF / LATCH

Mode: DFF

Second Q select: None

nSET/nRESET option: nRESET

Initial polarity: Low

Q output polarity: Non-inverted (Q)

Active level for RST/SET: Low level

Properties

3-bit LUT1/DFF/LATCH3

Type: DFF / LATCH

Mode: DFF

Second Q select: None

nSET/nRESET option: nRESET

Initial polarity: Low

Q output polarity: Non-inverted (Q)

Active level for RST/SET: Low level

Properties

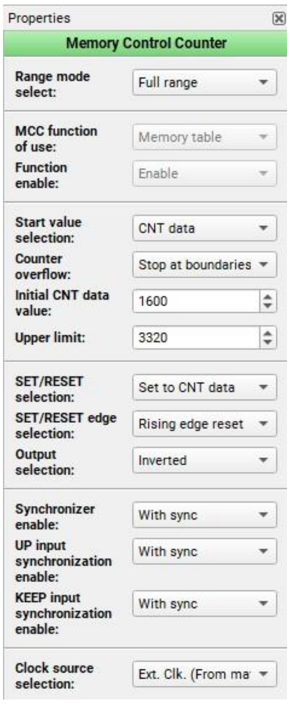
3-bit LUT9/DFF/LATCH11/Shift Regist...

Type: LUT

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1

Figure 5. Configuration of the Phase Detector.

Figure 6 shows the **U/P counter** configuration of the Memory Control Counter macrocell. The U/P counter tracks the phase variation to PLL. The upper limit of the Memory Control Counter macrocell is equivalent to the data size of the Memory Table. The counter overflow should be configured with the “Stop at boundaries” selection.



Properties

Memory Control Counter

Range mode select: Full range

MCC function of use: Memory table

Function enable: Enable

Start value selection: CNT data

Counter overflow: Stop at boundaries

Initial CNT data value: 1600

Upper limit: 3320

SET/RESET selection: Set to CNT data

SET/RESET edge selection: Rising edge reset

Output selection: Inverted

Synchronizer enable: With sync

UP input synchronization enable: With sync

KEEP input synchronization enable: With sync

Clock source selection: Ext. Clk. (From ma

Figure 6. Configuration of the U/P Counter (Memory Control Counter macrocell).

Theoretically, the control loop bandwidth should be less than 1/10th of the minimum frequency < 30 kHz.

The frequency source (F_{MCC}) of the MCC macrocell is given by the loop bandwidth formula:

$$Loop\_Bandwidth = \frac{F_{MCC}}{Min(\{DIV_{IN}, DIV_{Feedback}\})} \quad \text{(Equation 1)}$$

where DIV_{IN} and $DIV_{Feedback}$ represent the parameter of the frequency divider.

The calculated F_{MCC} (ideal value) can then be obtained which is < 240 kHz.

Using the appropriate configuration and Equation 2, the F_{MCC} in this design is given as 83 kHz.

$$F_{MCC} = \frac{OSC\_40MHz}{OSC_{DIV} \times CNT_{DATA}} \quad \text{(Equation 2)}$$

where OSC_{DIV} = 24 and CNT_{DATA} = 19 (from the CNT6 macorcell)

Properties

12-bit CNT6/DLY6 (MF6)

Multi-function mode: CNT/DLY

Mode: Reset counter

Counter data: 19

(Range: 1 - 4095)

Output period (typical): N/D Formula

Edge mode select: Rising

DLY IN init. value: Bypass the initial

Output polarity: Non-inverted (OUT

Up signal SYNC: None

Keep signal SYNC: None

Mode signal SYNC: Bypass

Connections

Clock source: Ext. Clk. (From ma

Clock divider: N/D

Clock frequency: N/D

Properties

3-bit LUT5/DFF/LATCH7

Type: DFF / LATCH

Mode: DFF

Second Q select: None

nSET/nRESET option: nRESET

Initial polarity: Low

Q output polarity: Inverted (nQ)

Active level for RST/SET: Low level

Figure 7. Configuration of the MCC Clock Source.

The Memory Table macrocell data in the NCO block needs to be assigned with specific data by the Numerical Mapping process. In this design, Figure 8 shows the Numerical Mapping NCO frequency curve plot.

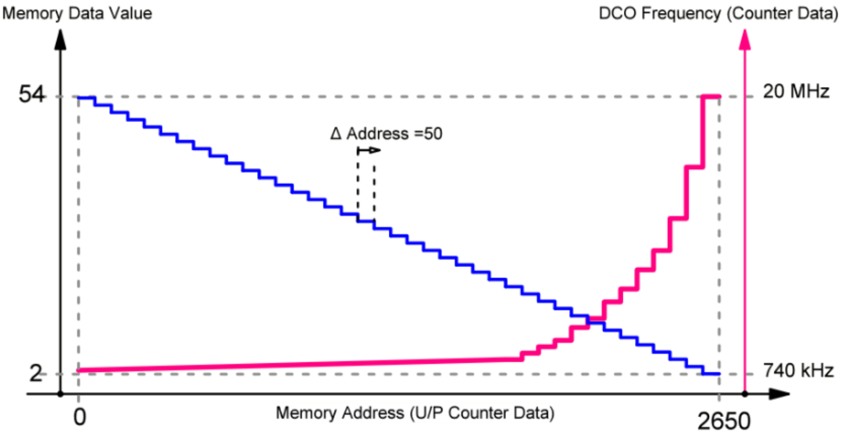
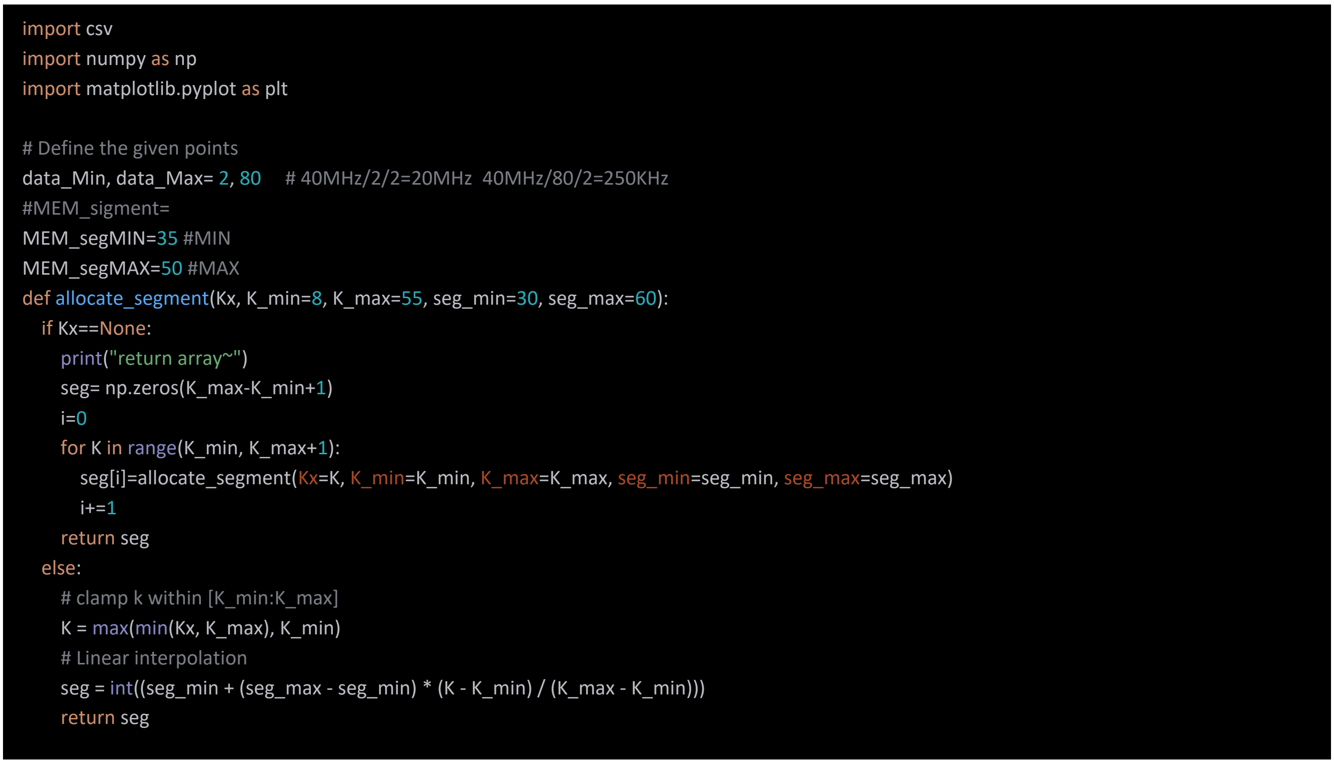


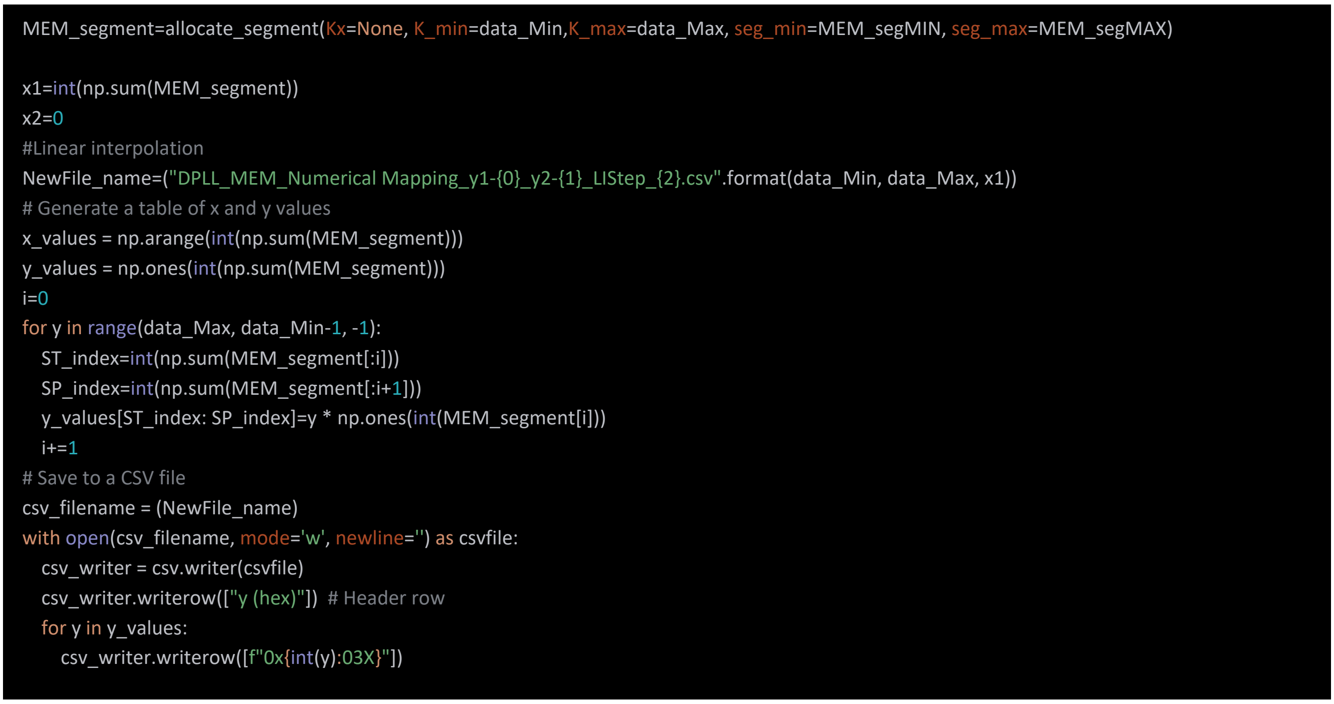
Figure 8. Memory Table Numerical Mapping NCO Frequency.

The following python script can be used to generate the required CSV file to fill the content of the Memory Table. In the Memory Table's data design, the corresponding allowed frequency ranges from 250 kHz to 10 MHz.



```
import csv
import numpy as np
import matplotlib.pyplot as plt

# Define the given points
data_Min, data_Max= 2, 80    # 40MHz/2/2=20MHz  40MHz/80/2=250KHz
#MEM_sigment=
MEM_segMIN=35 #MIN
MEM_segMAX=50 #MAX
def allocate_segment(Kx, K_min=8, K_max=55, seg_min=30, seg_max=60):
    if Kx==None:
        print("return array~")
        seg= np.zeros(K_max-K_min+1)
        i=0
        for K in range(K_min, K_max+1):
            seg[i]=allocate_segment(Kx=K, K_min=K_min, K_max=K_max, seg_min=seg_min, seg_max=seg_max)
            i+=1
        return seg
    else:
        # clamp k within [K_min:K_max]
        K = max(min(Kx, K_max), K_min)
        # Linear interpolation
        seg = int((seg_min + (seg_max - seg_min) * (K - K_min) / (K_max - K_min)))
        return seg
```



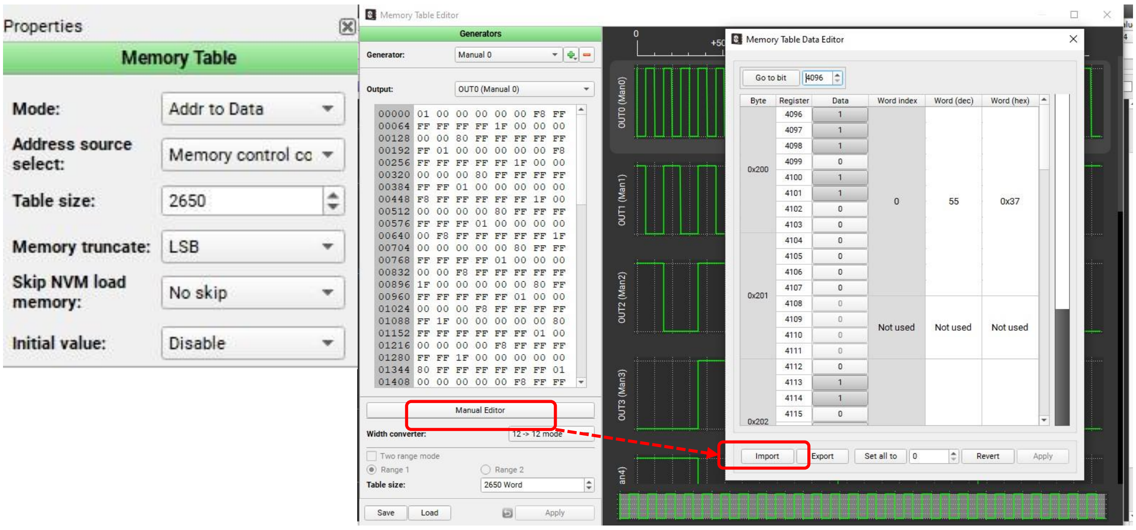
```
MEM_segment=allocate_segment(Kx=None, K_min=data_Min,K_max=data_Max, seg_min=MEM_segMIN, seg_max=MEM_segMAX)

x1=int(np.sum(MEM_segment))
x2=0
#Linear interpolation
NewFile_name=("DPLL_MEM_Numerical Mapping_y1-{0}_y2-{1}_LIStep_{2}.csv".format(data_Min, data_Max, x1))
# Generate a table of x and y values
x_values = np.arange(int(np.sum(MEM_segment)))
y_values = np.ones(int(np.sum(MEM_segment)))
i=0
for y in range(data_Max, data_Min-1, -1):
    ST_index=int(np.sum(MEM_segment[:i]))
    SP_index=int(np.sum(MEM_segment[:i+1]))
    y_values[ST_index: SP_index]=y * np.ones(int(MEM_segment[i]))
    i+=1
# Save to a CSV file
csv_filename = (NewFile_name)
with open(csv_filename, mode='w', newline='') as csvfile:
    csv_writer = csv.writer(csvfile)
    csv_writer.writerow(["y (hex)"])  # Header row
    for y in y_values:
        csv_writer.writerow([f"0x{int(y):03X}"])
```

```python
print(f"Table saved to {csv_filename}")
# Plot the x-y relationship
plt.figure(figsize=(10, 6))
plt.plot(x_values, y_values, label="MEM data(CSV)", color='blue', marker='o', markersize=4, linewidth=1)
plt.title('Numerical Mapping to Memory Table')
plt.xlabel('x (NCO/MEM_Reg#)')
plt.ylabel('y (NCO/MEM_Data)')
plt.grid(True)
plt.legend()
plt.tight_layout()
plt.show()
```

Python Script: Numerical Mapping_MEM_gen_r01.py

The Memory Table configuration is shown in Figure 9. The Data Editor in the Go Configure software can load the entire numerical data set from the generated csv file.



Properties

Memory Table

Mode: Addr to Data

Address source select: Memory control co

Table size: 2650

Memory truncate: LSB

Skip NVM load memory: No skip

Initial value: Disable

Memory Table Editor

Generators

Generator: Manual 0

Output: OUT0 (Manual 0)

```
00000 01 00 00 00 00 00 F8 FF
00064 FF FF FF FF 1F 00 00 00
00128 00 00 80 FF FF FF FF FF
00192 FF 01 00 00 00 00 00 F8
00256 FF FF FF FF FF 1F 00 00
00320 00 00 00 80 FF FF FF FF
00384 FF FF 01 00 00 00 00 00
00448 F8 FF FF FF FF FF 1F 00
00512 00 00 00 00 80 FF FF FF
00576 FF FF FF 01 00 00 00 00
00640 00 F8 FF FF FF FF FF 1F
00704 00 00 00 00 00 80 FF FF
00768 FF FF FF FF 01 00 00 00
00832 00 00 F8 FF FF FF FF FF
00896 1F 00 00 00 00 00 80 FF
00960 FF FF FF FF FF 01 00 00
01024 00 00 00 F8 FF FF FF FF
01088 FF 1F 00 00 00 00 00 80
01152 FF FF FF FF FF FF 01 00
01216 00 00 00 00 F8 FF FF FF
01280 FF FF 1F 00 00 00 00 00
01344 80 FF FF FF FF FF FF 01
01408 00 00 00 00 00 F8 FF FF
```

Width converter: 12 -> 12 mode

☐ Two range mode

● Range 1 ○ Range 2

Table size: 2650 Word

Memory Table Data Editor

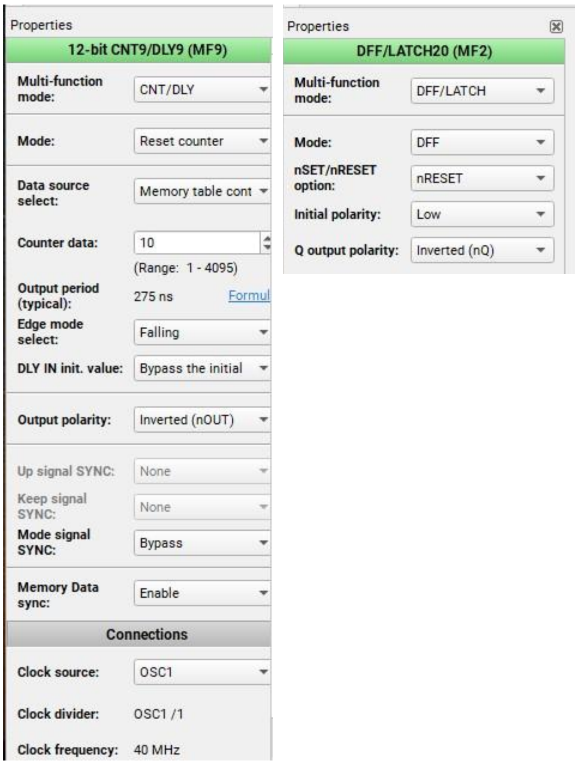
Go to bit: 4096

Byte	Register	Data	Word index	Word (dec)	Word (hex)
0x200	4096	1	0	55	0x37
	4097	1			
	4098	1			
	4099	0			
	4100	1			
	4101	1			
	4102	0			
	4103	0			
0x201	4104	0			
	4105	0			
	4106	0			
	4107	0			
	4108	0	Not used	Not used	Not used
	4109	0			
	4110	0			
	4111	0			
0x202	4112	0			
	4113	1			
	4114	1			
	4115	0			

Set all to: 0

Figure 9. Memory Table configuration

After completing the data loading process, the configuration of the other macrocells in the NCO block are shown in Figure 10. The counter converts the memory data to the corresponding doubling of the frequency signal. Finally, the DFF block obtains the required output frequency F_OUT.



Properties

12-bit CNT9/DLY9 (MF9)

Multi-function mode: CNT/DLY
Mode: Reset counter
Data source select: Memory table cont
Counter data: 10
(Range: 1 - 4095)
Output period (typical): 275 ns
Edge mode select: Falling
DLY IN init. value: Bypass the initial
Output polarity: Inverted (nOUT)
Up signal SYNC: None
Keep signal SYNC: None
Mode signal SYNC: Bypass
Memory Data sync: Enable

Connections

Clock source: OSC1
Clock divider: OSC1 /1
Clock frequency: 40 MHz

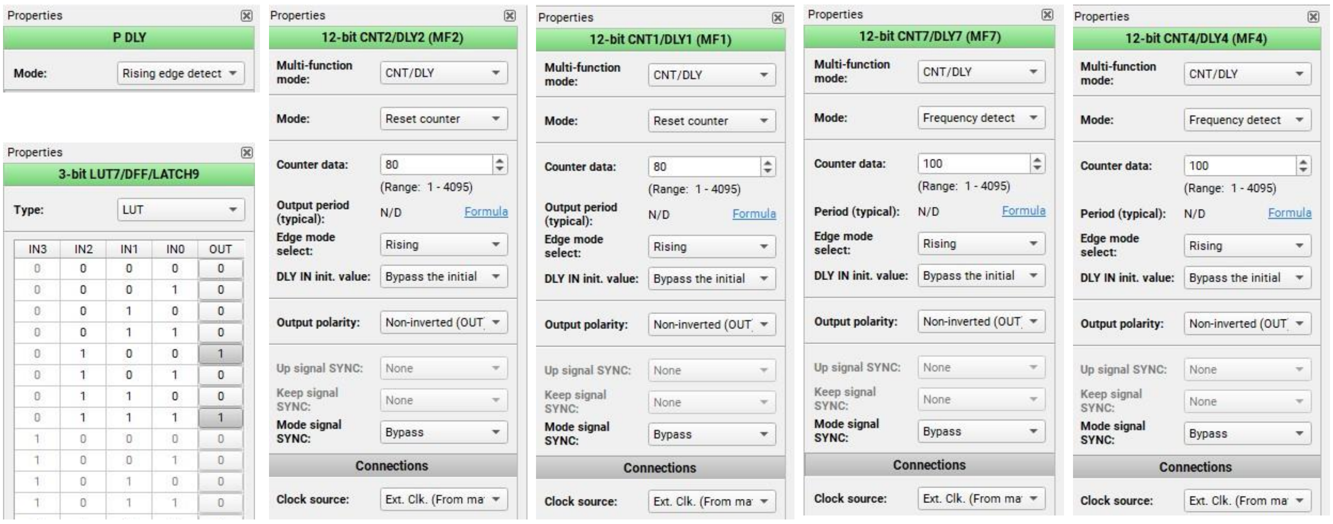
Properties

DFF/LATCH20 (MF2)

Multi-function mode: DFF/LATCH
Mode: DFF
nSET/nRESET option: nRESET
Initial polarity: Low
Q output polarity: Inverted (nQ)

Figure 10. Dual SHR Configuration for Frequency Divider Ratio.

The Boost Response block ensures that the initial activity occurs with a fast response. The P-DLY macrocell provides the detection of the rising edge to distinguish the initial activity status. The CNT macrocell provides the boosting response to the U/P counter in the DPLL loop. The configuration for the elements in this block are shown in Figure 11.



Properties

P DLY

Mode: Rising edge detect

Properties

3-bit LUT7/DFF/LATCH9

Type: LUT

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0

Properties

12-bit CNT2/DLY2 (MF2)

Multi-function mode: CNT/DLY
Mode: Reset counter
Counter data: 80
(Range: 1 - 4095)
Output period (typical): N/D
Edge mode select: Rising
DLY IN init. value: Bypass the initial
Output polarity: Non-inverted (OUT
Up signal SYNC: None
Keep signal SYNC: None
Mode signal SYNC: Bypass

Connections

Clock source: Ext. Clk. (From ma

Properties

12-bit CNT1/DLY1 (MF1)

Multi-function mode: CNT/DLY
Mode: Reset counter
Counter data: 80
(Range: 1 - 4095)
Output period (typical): N/D
Edge mode select: Rising
DLY IN init. value: Bypass the initial
Output polarity: Non-inverted (OUT
Up signal SYNC: None
Keep signal SYNC: None
Mode signal SYNC: Bypass

Connections

Clock source: Ext. Clk. (From ma

Properties

12-bit CNT7/DLY7 (MF7)

Multi-function mode: CNT/DLY
Mode: Frequency detect
Counter data: 100
(Range: 1 - 4095)
Period (typical): N/D
Edge mode select: Rising
DLY IN init. value: Bypass the initial
Output polarity: Non-inverted (OUT
Up signal SYNC: None
Keep signal SYNC: None
Mode signal SYNC: Bypass

Connections

Clock source: Ext. Clk. (From ma

Properties

12-bit CNT4/DLY4 (MF4)

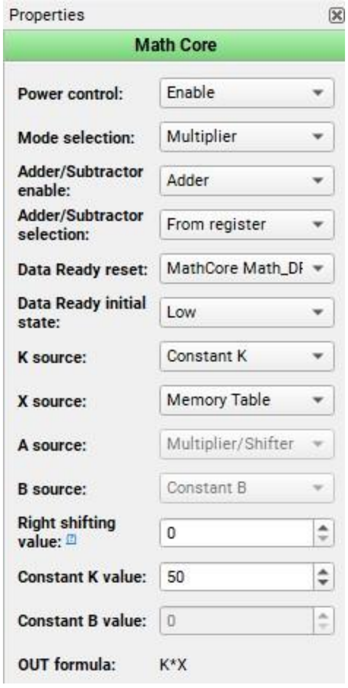
Multi-function mode: CNT/DLY
Mode: Frequency detect
Counter data: 100
(Range: 1 - 4095)
Period (typical): N/D
Edge mode select: Rising
DLY IN init. value: Bypass the initial
Output polarity: Non-inverted (OUT
Up signal SYNC: None
Keep signal SYNC: None
Mode signal SYNC: Bypass

Connections

Clock source: Ext. Clk. (From ma

Figure 11. Boost Response block configuration.

The NCO data monitor is used to monitor the variation of NCO data directly. The DAC outputs the corresponding analog signal to indicate NCO data.



Properties

Math Core

Power control: Enable

Mode selection: Multiplier

Adder/Subtractor enable: Adder

Adder/Subtractor selection: From register

Data Ready reset: MathCore Math_DF

Data Ready initial state: Low

K source: Constant K

X source: Memory Table

A source: Multiplier/Shifter

B source: Constant B

Right shifting value: 0

Constant K value: 50

Constant B value: 0

OUT formula: K*X

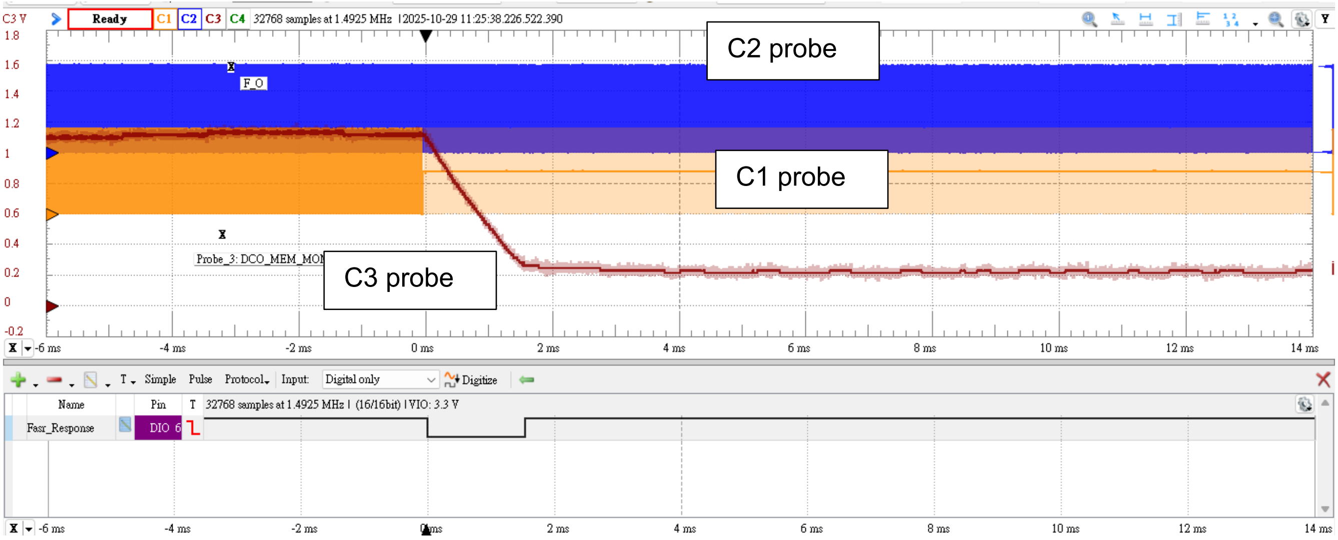
Figure 12. NCO Data Monitor block configuration.

5. Design Verification

Transition Response measurement:

- C1 probe: F_IN (PIN7) is the Input Frequency: F_min (300 kHz) is changed to F_max (1500 kHz)
- C2 probe: F_Out (PIN13) reflects the output frequency
- C3 probe: NCO_MON (PIN12) is the NCO Data Monitor
- D0 GPO: The internal multiplexer for Fast Response. Low status toggles fast MCC clock

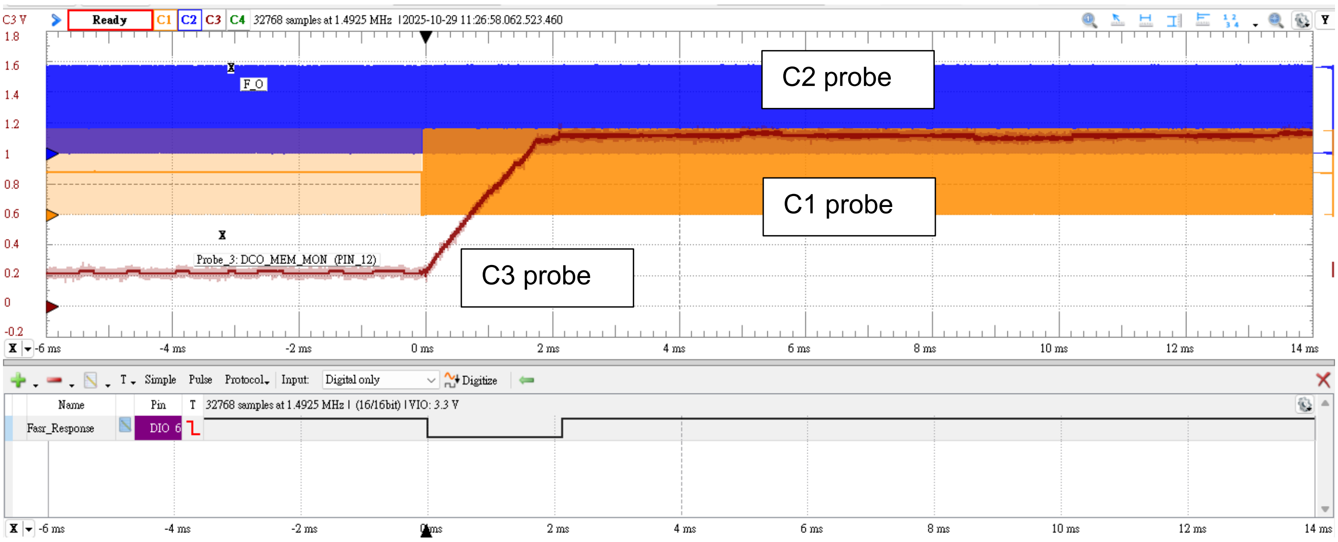
The transition response is around 2 ms.



Transition Response measurement:

- C1 probe: F_IN (PIN7) is the Input Frequency: F_max (1500 kHz) is changed to F_min (300 kHz)
- C2 probe: F_Out (PIN13) reflects the output frequency
- C3 probe: NCO_MON (PIN12) is the NCO Data Monitor
- D0 GPO: The internal multiplexer for Fast Response. Low status toggles fast MCC clock

The transition response is around 2 ms.



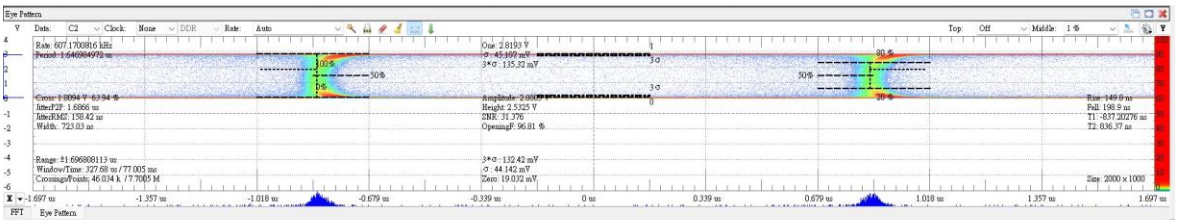
Jitter measurement without reducing bandwidth:

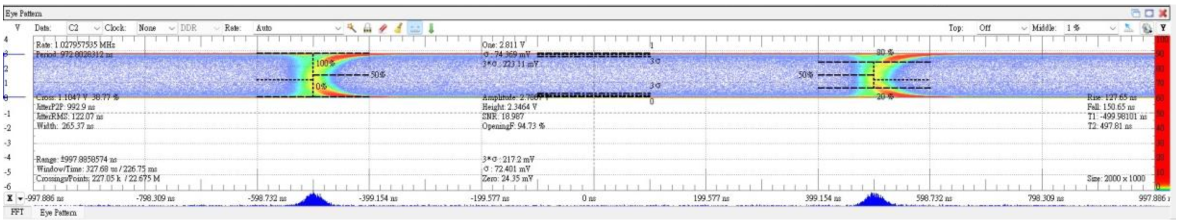
The input frequency F_IN is given 300 kHz, 500 kHz, and 700 kHz, separately.

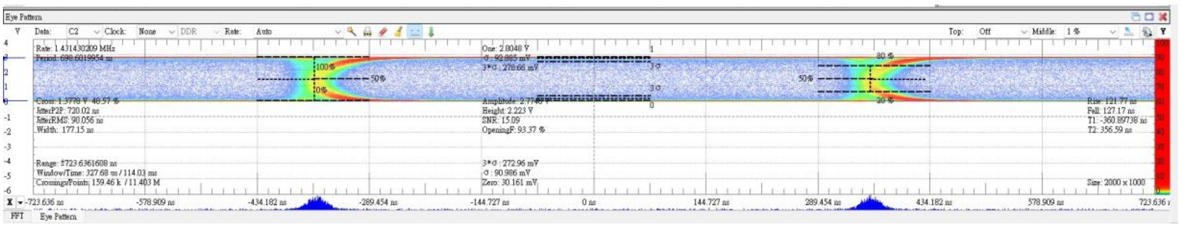
Without reducing bandwidth, the counter data of the internal counter CNT6 is still 19.

The Eye diagram of the output frequency (Probe C2 probe) can be obtained.

1. The F_OUT Jitter_RMS = 160 ns @ F_IN = 300 kHz: The output SNR = 31 dB
2. The F_OUT Jitter_RMS = 122 ns @ F_IN = 500 kHz: The output SNR = 19 dB
3. The F_OUT Jitter_RMS = 90 ns @ F_IN = 700 kHz: The output SNR = 15 dB







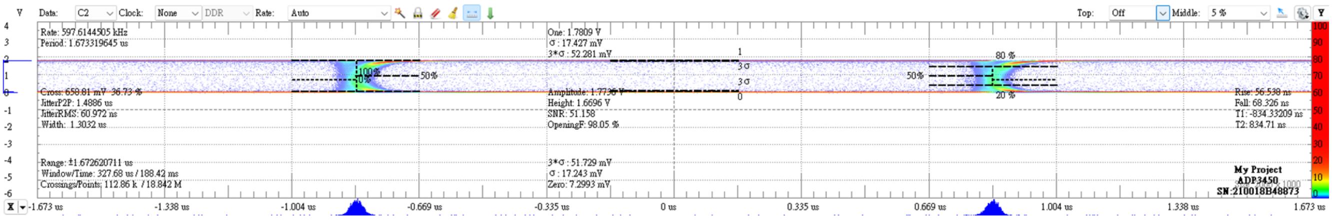
Jitter measurement while reducing bandwidth:

The input frequency F_IN is given 300 kHz, 500 kHz, and 700 kHz, separately.

The counter data of the internal counter CNT6 is changed from 19 to 259. SNR can be improved significantly.

The Eye diagram of the output frequency (Probe C2 probe) can be obtained.

1. The F_OUT Jitter_RMS = 60 ns @ F_IN = 300 kHz: The output SNR = 51 dB
2. The F_OUT Jitter_RMS = 48 ns @ F_IN = 500 kHz: The output SNR = 39.8 dB
3. The F_OUT Jitter_RMS = 63 ns @ F_IN = 700 kHz: The output SNR = 20 dB



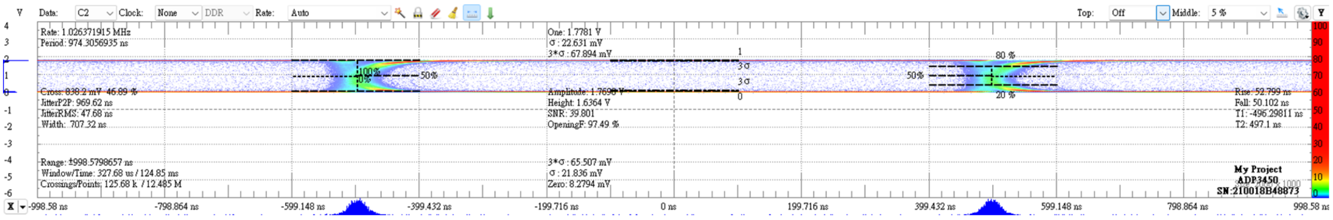
Data: C2
Clock: None
DDR
Rate: Auto
Top: Off
Middle: 5 %

Rate: 597.6144505 kHz
Period: 1.673319645 us
Cross: 658.81 mV 36.73 %
JitterP2P: 1.4886 us
JitterRMS: 60.972 ns
Width: 1.3032 us
Range: ±1.672620711 us
Window/Time: 327.68 us / 188.42 ms
Crossings/Points: 112.86 k / 18.842 M

One: 1.7809 V
σ : 17.427 mV
3*σ : 52.281 mV
Amplitude: 1.7736 V
Height: 1.6696 V
SNR: 51.158
OpeningF: 98.05 %
3*σ : 51.729 mV
σ : 17.243 mV
Zero: 7.2993 mV

Rise: 56.538 ns
Fall: 68.326 ns
T1: -834.33209 ns
T2: 834.71 ns

My Project
ADP3450
SN:210018B48873



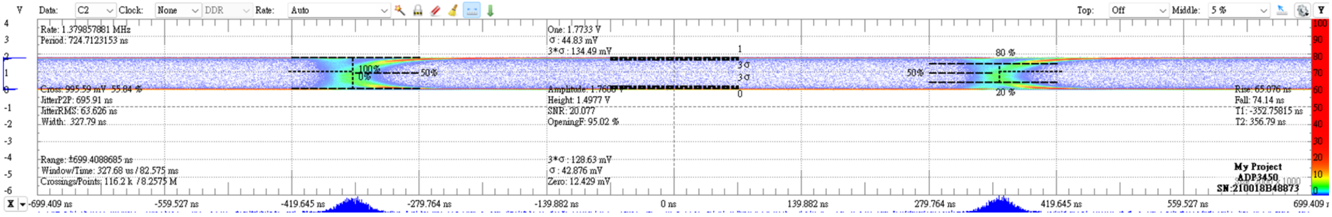
Data: C2
Clock: None
DDR
Rate: Auto
Top: Off
Middle: 5 %

Rate: 1.026371915 MHz
Period: 974.3056935 ns
Cross: 838.2 mV 46.89 %
JitterP2P: 969.62 ns
JitterRMS: 47.68 ns
Width: 707.32 ns
Range: ±998.5798657 ns
Window/Time: 327.68 us / 124.85 ms
Crossings/Points: 125.68 k / 12.485 M

One: 1.7781 V
σ : 22.631 mV
3*σ : 67.894 mV
Amplitude: 1.7698 V
Height: 1.6364 V
SNR: 39.801
OpeningF: 97.49 %
3*σ : 65.507 mV
σ : 21.836 mV
Zero: 8.2794 mV

Rise: 52.799 ns
Fall: 50.102 ns
T1: -496.29811 ns
T2: 497.1 ns

My Project
ADP3450
SN:210018B48873



Data: C2
Clock: None
DDR
Rate: Auto
Top: Off
Middle: 5 %

Rate: 1.379857881 MHz
Period: 724.7123153 ns
Cross: 995.59 mV 55.84 %
JitterP2P: 695.91 ns
JitterRMS: 63.626 ns
Width: 327.79 ns
Range: ±699.4088685 ns
Window/Time: 327.68 us / 82.575 ms
Crossings/Points: 116.2 k / 8.2575 M

One: 1.7733 V
σ : 44.83 mV
3*σ : 134.49 mV
Amplitude: 1.7608 V
Height: 1.4977 V
SNR: 20.077
OpeningF: 95.02 %
3*σ : 128.63 mV
σ : 42.876 mV
Zero: 12.429 mV

Rise: 65.076 ns
Fall: 74.14 ns
T1: -352.75815 ns
T2: 356.79 ns

My Project
ADP3450
SN:210018B48873

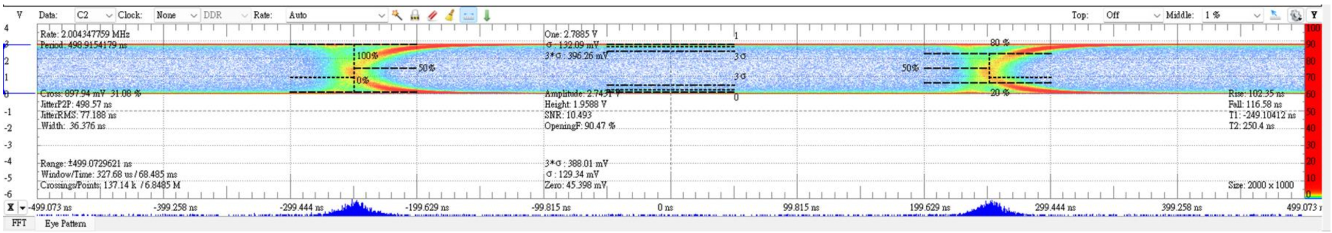
Jitter measurement without reducing bandwidth:

The input frequency F_IN is given 1 MHz, 1.25 MHz, and 1.5 MHz, separately.

Without reducing bandwidth, the counter data of the internal counter CNT6 is still 19.

The Eye diagram of the output frequency (Probe C2 probe) can be obtained.

1. The F_OUT Jitter_RMS = 77 ns @ F_IN = 1 MHz: The output SNR = 10.5 dB
2. The F_OUT Jitter_RMS = 53 ns @ F_IN = 1.25 MHz: The output SNR = 10.6 dB
3. The F_OUT Jitter_RMS = 95 ns @ F_IN = 1.5 MHz: The output SNR = 6.4 dB

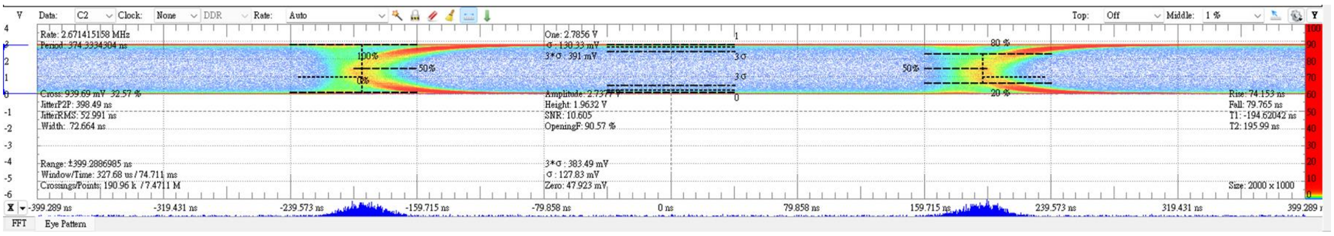


Data: C2 Clock: None DDR Rate: Auto Top: Off Middle: 1 %

Rate: 2.004347759 MHz
Period: 498.9154179 ns
Cross: 897.94 mV 31.08 %
JitterP2P: 498.57 ns
JitterRMS: 77.188 ns
Width: 36.376 ns
Range: ±499.0729621 ns
Window/Time: 327.68 us / 68.485 ms
Crossings/Points: 137.14 k / 6.8485 M

One: 2.7885 V
σ : 132.09 mV
3*σ : 396.26 mV
Amplitude: 2.7431 V
Height: 1.9588 V
SNR: 10.493
OpeningF: 90.47 %
3*σ : 388.01 mV
σ : 129.34 mV
Zero: 45.398 mV

Rise: 102.35 ns
Fall: 116.58 ns
T1: -249.10412 ns
T2: 250.4 ns
Size: 2000 x 1000

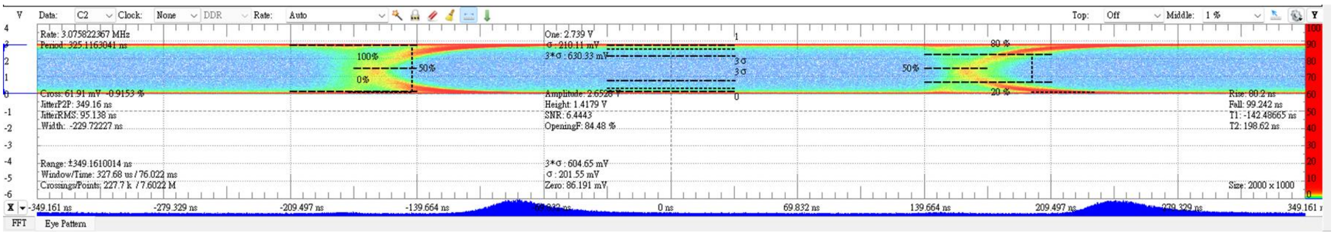


Data: C2 Clock: None DDR Rate: Auto Top: Off Middle: 1 %

Rate: 2.671415158 MHz
Period: 374.3334304 ns
Cross: 939.69 mV 32.57 %
JitterP2P: 398.49 ns
JitterRMS: 52.991 ns
Width: 72.664 ns
Range: ±399.2886985 ns
Window/Time: 327.68 us / 74.711 ms
Crossings/Points: 190.96 k / 7.4711 M

One: 2.7856 V
σ : 130.33 mV
3*σ : 391 mV
Amplitude: 2.7377 V
Height: 1.9632 V
SNR: 10.605
OpeningF: 90.57 %
3*σ : 383.49 mV
σ : 127.83 mV
Zero: 47.923 mV

Rise: 74.153 ns
Fall: 79.765 ns
T1: -194.62042 ns
T2: 195.99 ns
Size: 2000 x 1000



Data: C2 Clock: None DDR Rate: Auto Top: Off Middle: 1 %

Rate: 3.075822367 MHz
Period: 325.1163041 ns
Cross: 61.91 mV -0.9153 %
JitterP2P: 349.16 ns
JitterRMS: 95.138 ns
Width: -229.72227 ns
Range: ±349.1610014 ns
Window/Time: 327.68 us / 76.022 ms
Crossings/Points: 227.7 k / 7.6022 M

One: 2.739 V
σ : 210.11 mV
3*σ : 630.33 mV
Amplitude: 2.6528 V
Height: 1.4179 V
SNR: 6.4443
OpeningF: 84.48 %
3*σ : 604.65 mV
σ : 201.55 mV
Zero: 86.191 mV

Rise: 80.2 ns
Fall: 99.242 ns
T1: -142.48665 ns
T2: 198.62 ns
Size: 2000 x 1000

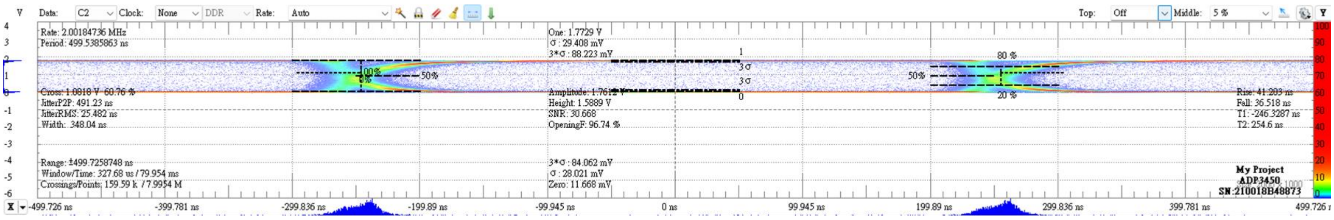
Jitter measurement while reducing bandwidth:

The input frequency F_IN is given 1 MHz, 1.25 MHz and 1.5 MHz, separately.

The counter data of the internal counter CNT6 is changed from 19 to 259. SNR can be improved significantly.

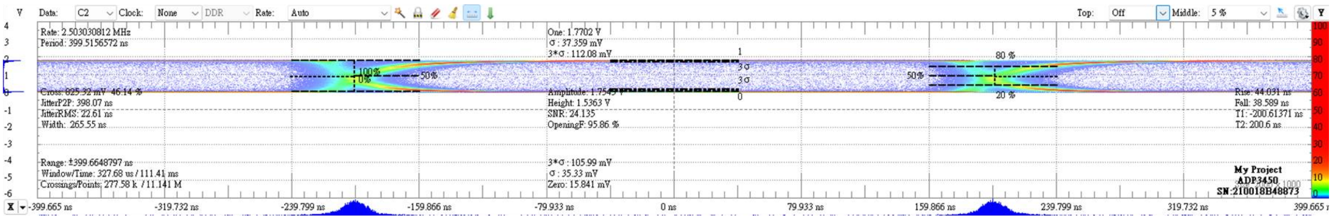
The Eye diagram of the output frequency (Probe C2 probe) can be obtained.

1. The F_OUT Jitter_RMS = 25.4 ns @ F_IN = 1 MHz: The output SNR = 30.6 dB
2. The F_OUT Jitter_RMS = 22.6 ns @ F_IN = 1.25 MHz: The output SNR = 24 dB
3. The F_OUT Jitter_RMS = 16.9 ns @ F_IN = 1.5 MHz: The output SNR = 25.8 dB



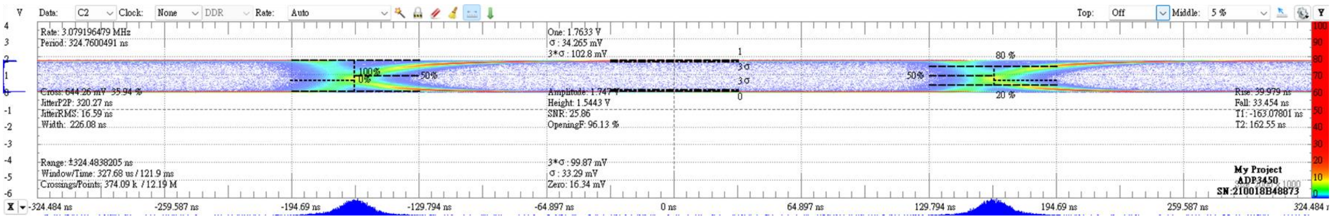
Data: C2 Clock: None DDR Rate: Auto Top: Off Middle: 5 %

Rate: 2.00184736 MHz
Period: 499.5385863 ns
Cross: 1.0818 V 60.76 %
JitterP2P: 491.23 ns
JitterRMS: 25.482 ns
Width: 348.04 ns
Range: ±499.7258748 ns
Window/Time: 327.68 us / 79.954 ms
Crossings/Points: 159.59 k / 7.9954 M
One: 1.7729 V
σ : 29.408 mV
3*σ : 88.223 mV
Amplitude: 1.7612 V
Height: 1.5889 V
SNR: 30.668
OpeningF: 96.74 %
3*σ : 84.062 mV
σ : 28.021 mV
Zero: 11.668 mV
Rise: 41.203 ns
Fall: 36.518 ns
T1: -246.3287 ns
T2: 254.6 ns



Data: C2 Clock: None DDR Rate: Auto Top: Off Middle: 5 %

Rate: 2.503030812 MHz
Period: 399.5156572 ns
Cross: 825.32 mV 46.14 %
JitterP2P: 398.07 ns
JitterRMS: 22.61 ns
Width: 265.55 ns
Range: ±399.6648797 ns
Window/Time: 327.68 us / 111.41 ms
Crossings/Points: 277.58 k / 11.141 M
One: 1.7702 V
σ : 37.359 mV
3*σ : 112.08 mV
Amplitude: 1.7545 V
Height: 1.5363 V
SNR: 24.135
OpeningF: 95.86 %
3*σ : 105.99 mV
σ : 35.33 mV
Zero: 15.841 mV
Rise: 44.031 ns
Fall: 38.589 ns
T1: -200.61371 ns
T2: 200.6 ns



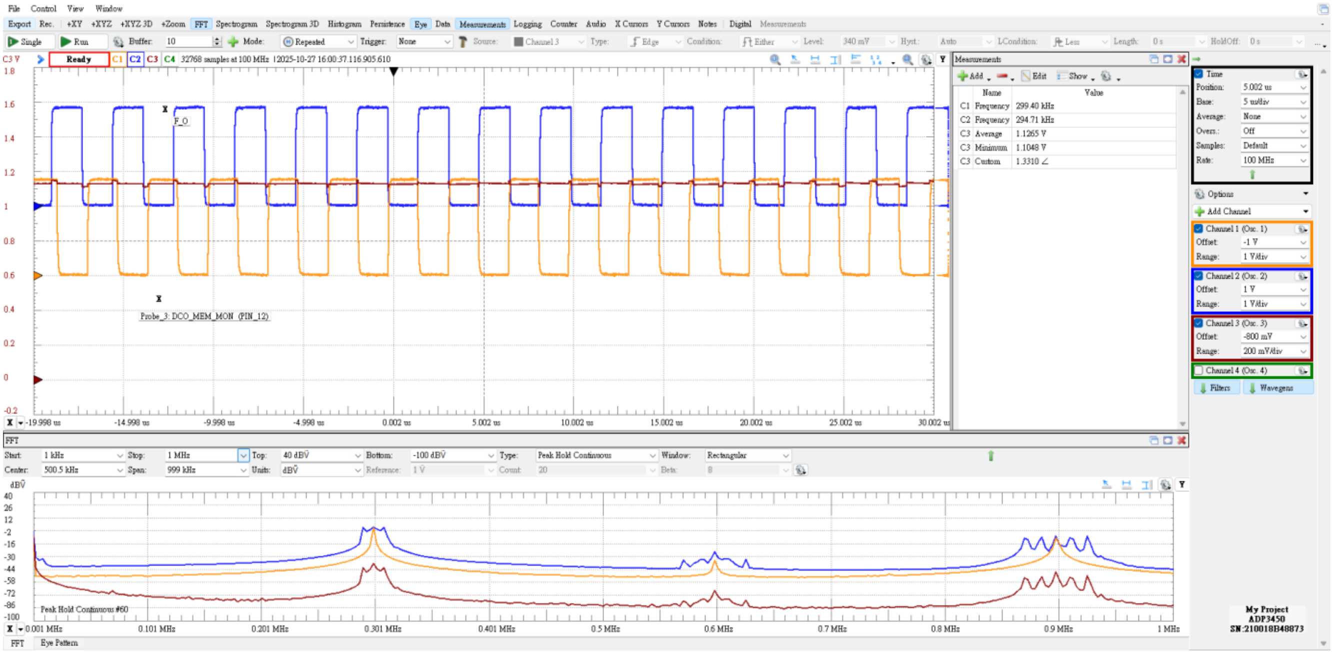
Data: C2 Clock: None DDR Rate: Auto Top: Off Middle: 5 %

Rate: 3.079196479 MHz
Period: 324.7600491 ns
Cross: 644.26 mV 35.94 %
JitterP2P: 320.27 ns
JitterRMS: 16.59 ns
Width: 226.08 ns
Range: ±324.4838205 ns
Window/Time: 327.68 us / 121.9 ms
Crossings/Points: 374.09 k / 12.19 M
One: 1.7633 V
σ : 34.265 mV
3*σ : 102.8 mV
Amplitude: 1.747 V
Height: 1.5443 V
SNR: 25.86
OpeningF: 96.13 %
3*σ : 99.87 mV
σ : 33.29 mV
Zero: 16.34 mV
Rise: 39.979 ns
Fall: 33.454 ns
T1: -163.07801 ns
T2: 162.55 ns

FFT measurement, @F_IN = 300 kHz

- C1 probe: F_IN (PIN7) is given input frequency 300 kHz
- C2 probe: F_Out (PIN13) reflects the output frequency
- Spectrum Analysis (FFT) result shows the comparison.

The spread spectrum of F_OUT is observed from 290 kHz to 308 kHz.



32768 samples at 100 MHz | 2025-10-27 16:00:37.116.905.610

Buffer: 10
Trigger: None
Source: Channel 3
Type: Edge
Level: 340 mV
LCondition: Less
Length: 0 s
HoldOff: 0 s

Name		Value
C1	Frequency	299.40 kHz
C2	Frequency	294.71 kHz
C3	Average	1.1265 V
C3	Minimum	1.1048 V
C3	Custom	1.3310 ∠

Time
Position: 5.002 us
Base: 5 us/div
Average: None
Overs.: Off
Samples: Default
Rate: 100 MHz

☑ Channel 1 (Osc. 1)
Offset: -1 V
Range: 1 V/div

☑ Channel 2 (Osc. 2)
Offset: 1 V
Range: 1 V/div

☑ Channel 3 (Osc. 3)
Offset: -800 mV
Range: 200 mV/div

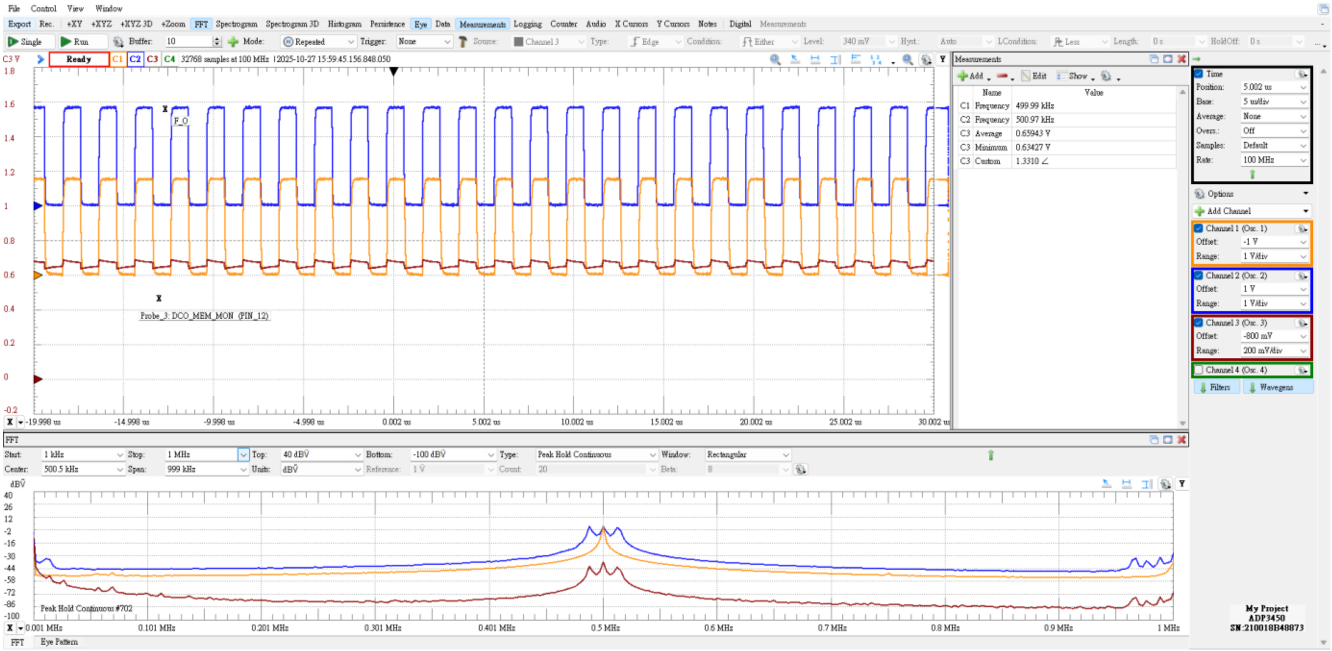
☐ Channel 4 (Osc. 4)

Start: 1 kHz
Stop: 1 MHz
Top: 40 dBV
Bottom: -100 dBV
Type: Peak Hold Continuous
Window: Rectangular
Center: 500.5 kHz
Span: 999 kHz
Units: dBV
Reference: 1 V
Count: 20
Beta: 8

FFT measurement, @F_IN = 500 kHz

- C1 probe: F_IN (PIN7) is given input frequency 500 kHz
- C2 probe: F_Out (PIN13) reflects the output frequency
- Spectrum Analysis (FFT) result shows the comparison.

The spread spectrum of F_OUT is observed from 488 kHz to 512 kHz.



32768 samples at 100 MHz | 2025-10-27 15:59:45.156.848.050

Buffer: 10
Mode: Repeated
Trigger: None
Source: Channel 3
Type: Edge
Level: 340 mV
LCondition: Less
Length: 0 s
HoldOff: 0 s

Name		Value
C1	Frequency	499.99 kHz
C2	Frequency	500.97 kHz
C3	Average	0.65943 V
C3	Minimum	0.63427 V
C3	Custom	1.3310 ∠

Time
Position: 5.002 us
Base: 5 us/div
Average: None
Overs.: Off
Samples: Default
Rate: 100 MHz

☑ Channel 1 (Osc. 1)
Offset: -1 V
Range: 1 V/div

☑ Channel 2 (Osc. 2)
Offset: 1 V
Range: 1 V/div

☑ Channel 3 (Osc. 3)
Offset: -800 mV
Range: 200 mV/div

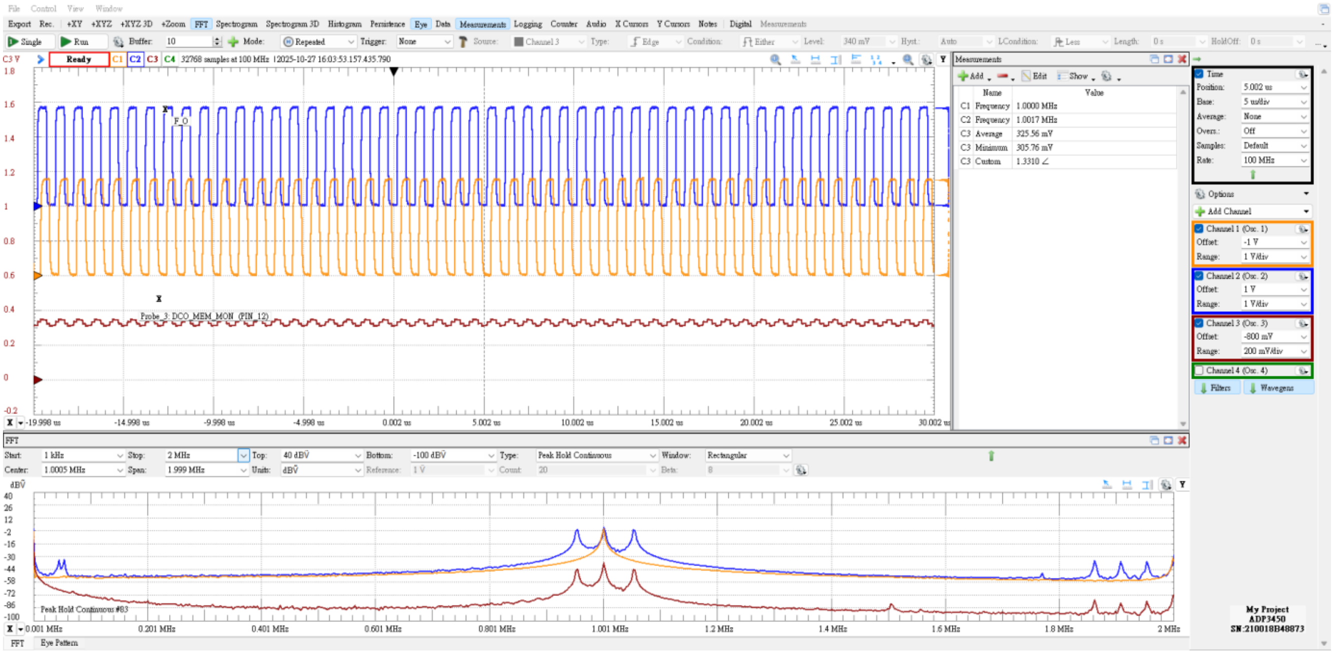
☐ Channel 4 (Osc. 4)

Start: 1 kHz
Stop: 1 MHz
Top: 40 dBV
Bottom: -100 dBV
Type: Peak Hold Continuous
Window: Rectangular
Center: 500.5 kHz
Span: 999 kHz
Units: dBV
Reference: 1 V
Count: 20
Beta: 8

FFT measurement, @F_IN= 1 MHz

- C1 probe: F_IN (PIN7) is given input frequency 1 MHz
- C2 probe: F_Out (PIN13) reflects the output frequency
- Spectrum Analysis (FFT) Result shows the comparison.

The spread spectrum of F_OUT is observed from 953 kHz to 1050 kHz.



Measurements

	Name	Value
C1	Frequency	1.0000 MHz
C2	Frequency	1.0017 MHz
C3	Average	325.56 mV
C3	Minimum	305.76 mV
C3	Custom	1.3310 ∠

☑ Time
Position: 5.002 us
Base: 5 us/div
Average: None
Overs.: Off
Samples: Default
Rate: 100 MHz

☑ Channel 1 (Osc. 1)
Offset: -1 V
Range: 1 V/div

☑ Channel 2 (Osc. 2)
Offset: 1 V
Range: 1 V/div

☑ Channel 3 (Osc. 3)
Offset: -800 mV
Range: 200 mV/div

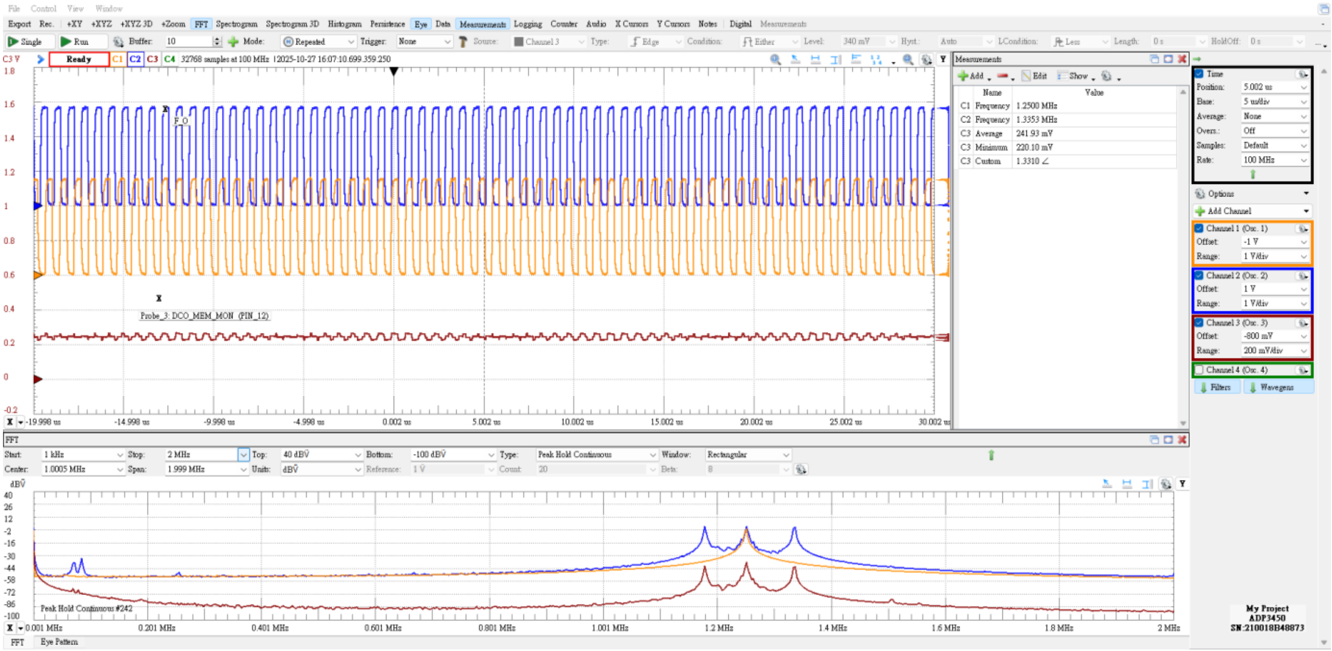
☐ Channel 4 (Osc. 4)

FFT
Start: 1 kHz
Stop: 2 MHz
Top: 40 dBV
Bottom: -100 dBV
Type: Peak Hold Continuous
Window: Rectangular
Center: 1.0005 MHz
Span: 1.999 MHz
Units: dBV
Reference: 1 V
Count: 20
Beta: 8

FFT measurement, @F_IN = 1.25 MHz:

- C1 probe: F_IN (PIN7) is given input frequency 1.25 MHz
- C2 probe: F_Out (PIN13) reflects the output frequency
- Spectrum Analysis (FFT) Result shows the comparison.

The spread spectrum of F_OUT is observed from 1178 kHz to 1336 kHz.



Measurements

	Name	Value
C1	Frequency	1.2500 MHz
C2	Frequency	1.3353 MHz
C3	Average	241.93 mV
C3	Minimum	220.10 mV
C3	Custom	1.3310 ∠

☑ Time
Position: 5.002 us
Base: 5 us/div
Average: None
Overs.: Off
Samples: Default
Rate: 100 MHz

☑ Channel 1 (Osc. 1)
Offset: -1 V
Range: 1 V/div

☑ Channel 2 (Osc. 2)
Offset: 1 V
Range: 1 V/div

☑ Channel 3 (Osc. 3)
Offset: -800 mV
Range: 200 mV/div

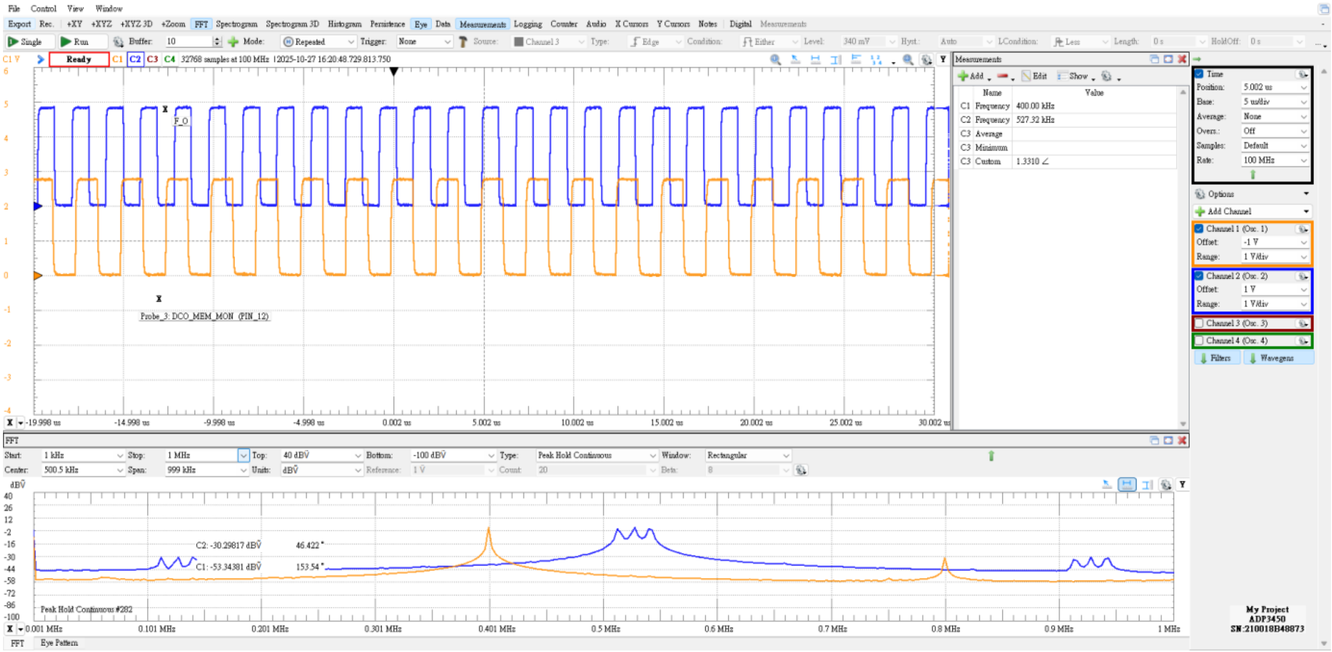
☐ Channel 4 (Osc. 4)

FFT
Start: 1 kHz
Stop: 2 MHz
Top: 40 dBV
Bottom: -100 dBV
Type: Peak Hold Continuous
Window: Rectangular
Center: 1.0005 MHz
Span: 1.999 MHz
Units: dBV
Reference: 1 V
Count: 20
Beta: 8

FFT measurement: @F_IN = 400 kHz; Integer-Ratio (N/M = 8/6) PLL, Disable Fast-Response Block

- C1 probe: F_IN (PIN7) is given input frequency 400 kHz, Input Frequency divider M = 6
- C2 probe: F_Out (PIN13) reflects the output frequency, Feedback Frequency divider N = 8
- Spectrum Analysis (FFT) Result shows the Integer-Ratio (**N**/**M** = 8/6) effect.

The spread spectrum of F_OUT is observed from 512 kHz to 540 kHz.



Ready C1 C2 C3 C4 32768 samples at 100 MHz |2025-10-27 16:20:48.729.813.750

Measurements

	Name	Value
C1	Frequency	400.00 kHz
C2	Frequency	527.32 kHz
C3	Average	
C3	Minimum	
C3	Custom	1.3310 ∠

Time: Position: 5.002 us; Base: 5 us/div; Average: None; Overs.: Off; Samples: Default; Rate: 100 MHz

Channel 1 (Osc. 1): Offset: -1 V; Range: 1 V/div

Channel 2 (Osc. 2): Offset: 1 V; Range: 1 V/div

FFT: Start: 1 kHz; Stop: 1 MHz; Top: 40 dBV̄; Bottom: -100 dBV̄; Type: Peak Hold Continuous; Window: Rectangular; Center: 500.5 kHz; Span: 999 kHz; Units: dBV̄; Reference: 1 V̄; Count: 20; Beta: 8

C2: -30.29817 dBV̄ 46.422 °

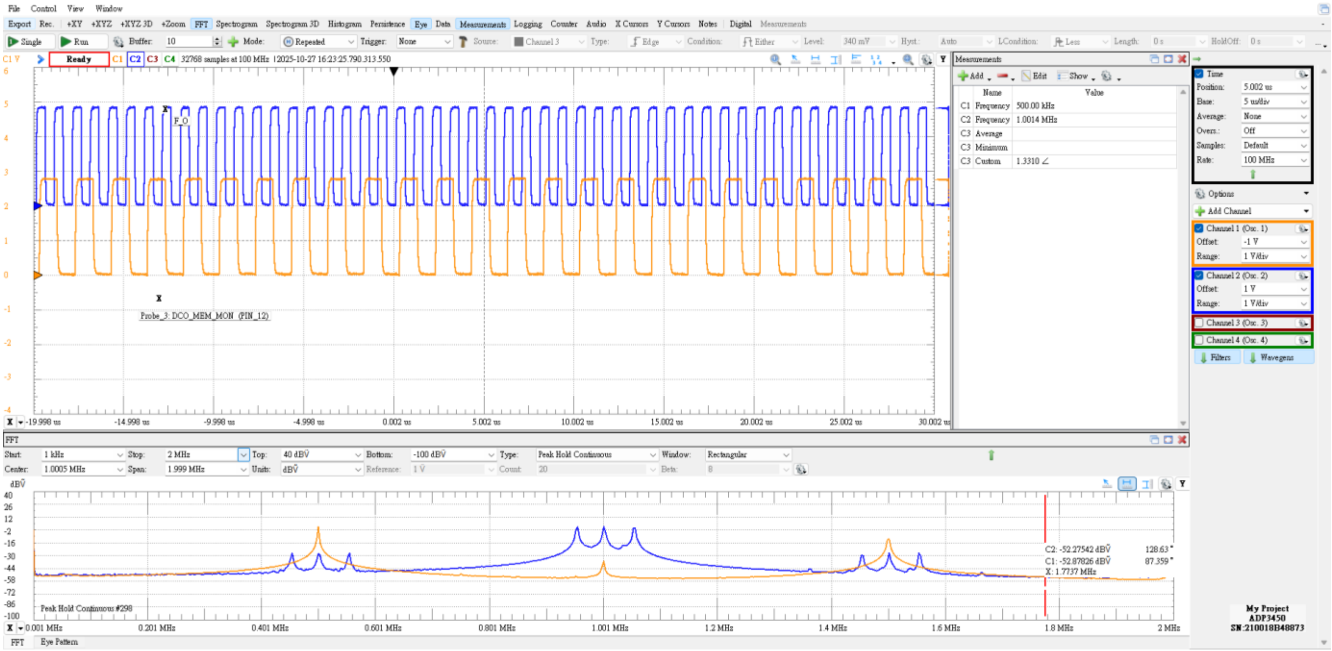
C1: -53.34381 dBV̄ 153.54 °

Peak Hold Continuous #282

FFT measurement: @F_IN = 500 kHz; Integer-Ratio (N/M = 8/4) PLL, Disable Fast-Response Block

- C1 probe: F_IN (PIN7) is given input frequency 400 kHz, Input Frequency divider M = 4
- C2 probe: F_Out (PIN13) reflects the output frequency, Feedback Frequency divider N = 8
- Spectrum Analysis (FFT) Result shows the Integer-Ratio (**N**/**M** = 8/4) effect.

The spread spectrum of F_OUT is observed from 955 kHz to 1059 kHz.



Ready C1 C2 C3 C4 32768 samples at 100 MHz |2025-10-27 16:23:25.790.313.550

Measurements

	Name	Value
C1	Frequency	500.00 kHz
C2	Frequency	1.0014 MHz
C3	Average	
C3	Minimum	
C3	Custom	1.3310 ∠

Time: Position: 5.002 us; Base: 5 us/div; Average: None; Overs.: Off; Samples: Default; Rate: 100 MHz

Channel 1 (Osc. 1): Offset: -1 V; Range: 1 V/div

Channel 2 (Osc. 2): Offset: 1 V; Range: 1 V/div

FFT: Start: 1 kHz; Stop: 2 MHz; Top: 40 dBV̄; Bottom: -100 dBV̄; Type: Peak Hold Continuous; Window: Rectangular; Center: 1.0005 MHz; Span: 1.999 MHz; Units: dBV̄; Reference: 1 V̄; Count: 20; Beta: 8

C2: -52.27542 dBV̄ 128.63 °

C1: -52.87826 dBV̄ 87.359 °

X: 1.7737 MHz

Peak Hold Continuous #298

6. Conclusion

The Renesas SLG47011V can be used to fulfill the requirements needed to implement a low bandwidth Digital PLL using its available internal digital macrocells. The results validate the flexibility of the design implementation.

However, there are several specific items or designs that require future considerations.

- Basic Jitter elimination: The results shows that jitter is significant with narrow variation of the NCO data. Therefore, using a higher internal oscillator (>> 40 MHz) can improve on the high jitter and low SNR.
- Boost Transition: The SLG47011V lacks an internal PI control macrocell which can improve overall response time and stability.
- Dual-Loop DPLL structure: It is possible that the control concept can be changed to allow the design to better reduce low-frequency reference jitter.
- Fractional-Ratio PLL: The current design only fulfills an Integer-Ratio PLL function. To support Fractional-Ratio control an accumulator and more macrocells are required.

7. Revision History

Revision	Date	Description
1.00	Feb 24, 2026	Initial version