Voltage, Current, Power, and Temperature Monitor
SLG47011

This application note describes how to use the SLG47011 to implement voltage, current, power, and temperature monitor. The application note comes complete with design files, which can be found in the References section.

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References

For related documents and software, please visit:

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Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-375 Voltage, Current, Power, and Temperature Monitor.aap, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

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1. Introduction

In the dynamic landscape of electronic systems, the need for a robust protection mechanism has become more imperative than ever. As devices and circuits continue to evolve in complexity and sophistication, susceptibility to potential hazards, such as overcurrent, overvoltage, overpower, and overtemperature events has increased significantly. Beyond mere safeguarding, the next step is to incorporate data logging capabilities. This combination not only protects electronic systems from harm but also empowers engineers with valuable insights into the performance and health of their applications.

To perform such tasks, an integrated circuit with three input channels of the Analog-to-Digital Converter (ADC) and an ability to compare measured data and log the results obtained is required. The SLG47011 from Renesas perfectly suits this challenge because it has a four-channel 14-bit ADC, a four-channel 16-bit digital comparator, and the capability to store data sets.

2. GreenPAK Design

Figure 1 shows an internal design of the monitor in the Go Configure software.

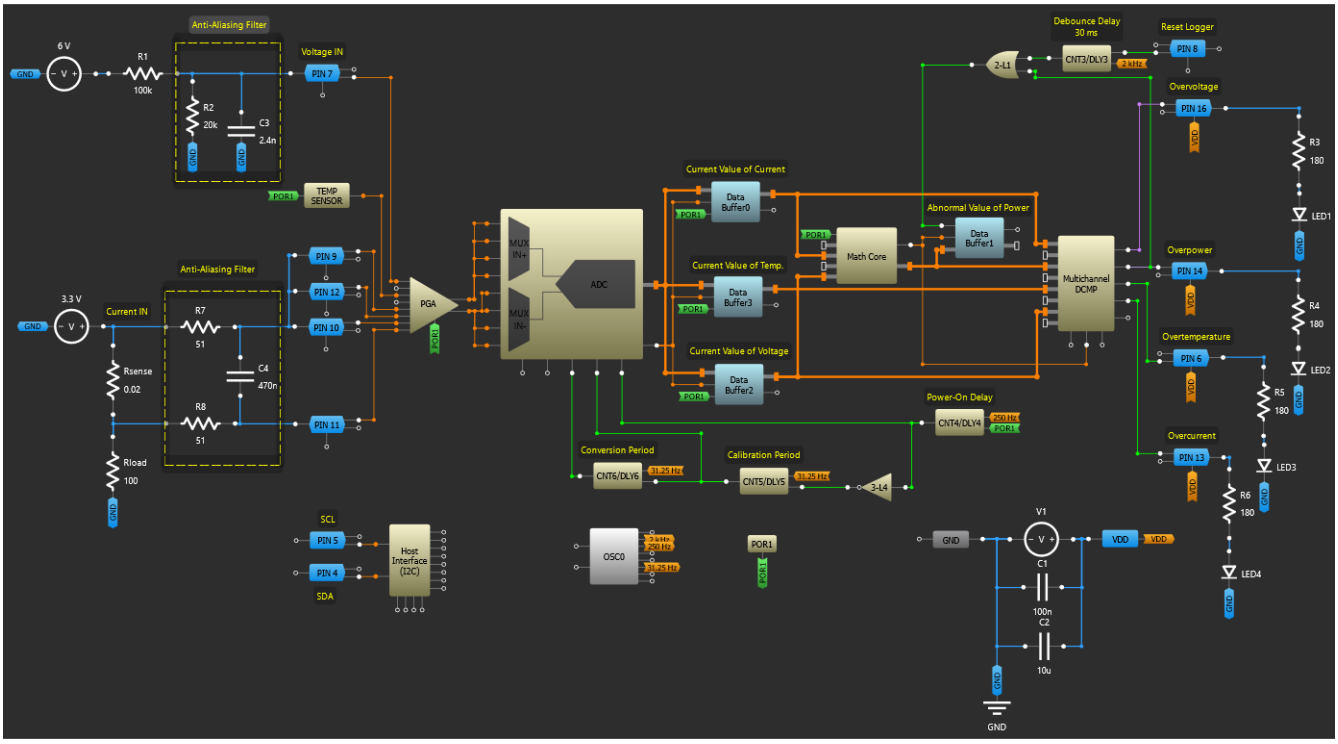


Figure 1. Go Configure Schematic of Monitor

The main function in this circuit is performed by the ADC, which processes three channels simultaneously with the help of the Sampling Engine block. Signals can be amplified through the PGA, which is used in this project for channel 2, designed to measure current. For channel 0 (voltage measurement) and channel 1 (temperature measurement), PGA is used in buffer mode. The Multichannel Digital Comparator sets the static threshold for each channel. When any of the measured values exceeds this threshold, a HIGH-level signal appears on the corresponding output. The Digital Comparator cannot directly take data from the ADC. For this purpose, Data Buffer 0, Data Buffer 2, and Data Buffer 3 are used to store the current values of the measurement.

An important block of the SLG47011 is the Mathematical Core (Math Core), which allows performing arithmetic operations on the measured values. In this case, the Math Core is used to multiply voltage and current values to obtain the power value.

Red LEDs are employed to indicate abnormal events. Depending on the event that occurred, the corresponding LED lights up.

2.1 Overvoltage Detection

If, for example, as given in the application note, there is a need to detect when the input voltage reaches 6 V, a divider must be used. Because this voltage exceeds the 1.62 V ADC reference voltage, a 5:1 divider is appropriate. The ADC input voltage for this overvoltage event, with this divider, is calculated as follows:

$$V_{IN} = 6 \frac{20}{20 + 100} = 1 \text{ V}$$

With the ADC Vref = 1.62 V, the digital comparator static threshold #3 value is set to:

$$TH3 = \frac{1}{1.62} 16384 = 10113$$

Figure 2 shows the overvoltage detection tested on the SLG47011.

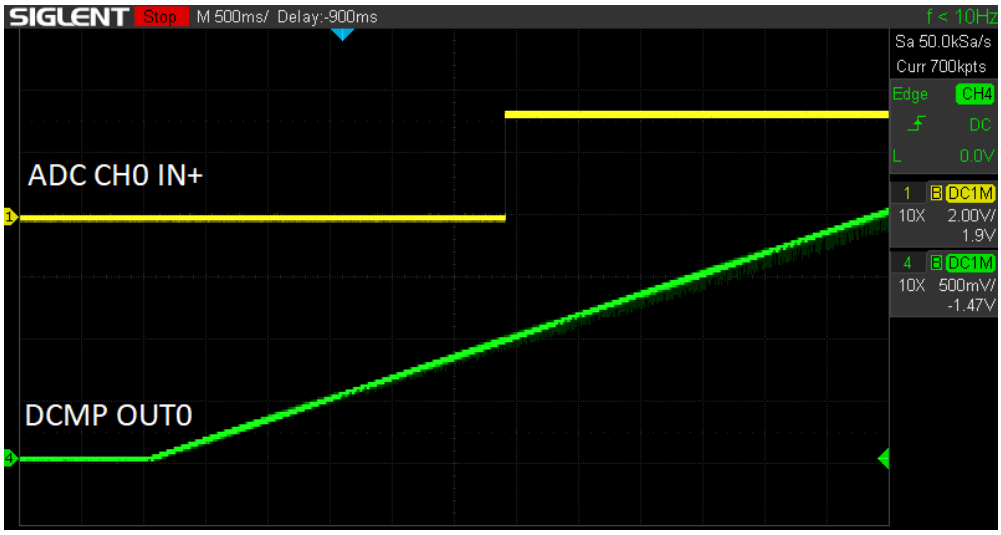


Figure 2. Waveform Illustrating Overvoltage Monitor

This solution is universal and allows for the selection of a divider and a comparator static threshold to set any voltage value at which the protection is triggered.

2.2 Overcurrent Detection

Overcurrent detection with a threshold equal to 5 A is considered as an example. For this purpose, a 0.02 Ω current sense resistor is used, on which, when a current of 5 A passes, 0.1 V drops. The PGA channel 3 is configured as a differential input with a differential amplifier with a gain of 4. For the differential mode, the gain is applied to the difference between IN+ and IN- with an offset of the ADC Vref/2, or at the ADC Vref = 1.62 V, the offset is equal to 1.62/2 = 0.81 V. Therefore, the digital comparator static threshold #0 value is:

$$TH0 = \frac{0.1 \times 4 + 0.81}{1.62} 16384 = 12237$$

Figure 3 shows the overcurrent detection tested on the SLG47011.

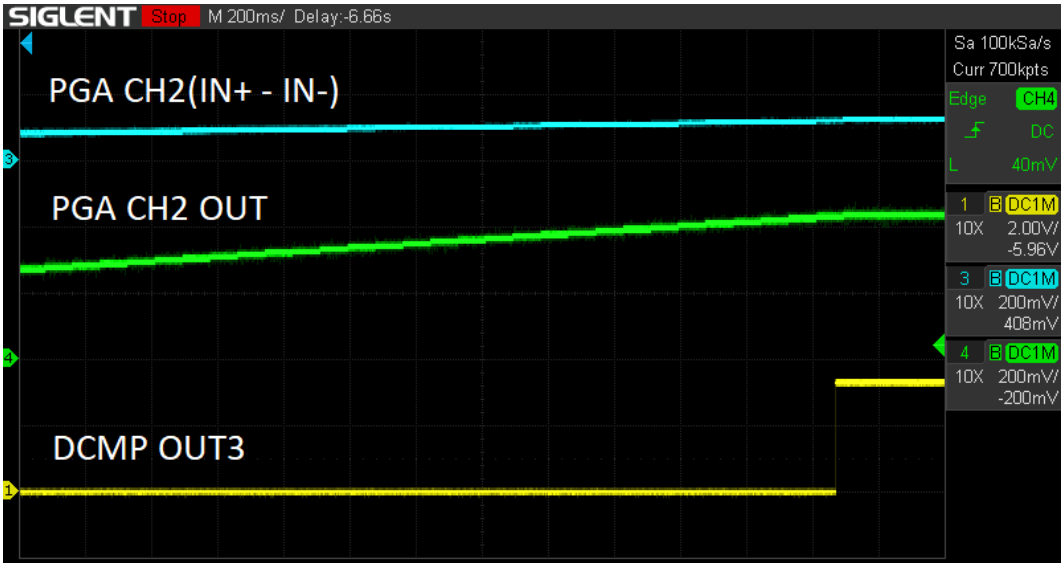


Figure 3. Waveform Illustrating Overcurrent Monitor

2.3 Overpower Detection

Sometimes it is not enough to measure only current and voltage. It is also desirable to know the power at these current and voltage values, because they may be within the permitted range, but high dissipation power can lead to failure. The Mathematical Core provides a 16-bit result to be compatible with the data bus width. Therefore, when multiplying the 16-bit current and 16-bit voltage values, a 32-bit value is obtained, causing an overflow. To provide a 16-bit result compatible with the data bus width, multiplication should be followed by a cyclic shift operation. The Math Core has a user-defined right-shifting value feature. In this example, a shift to the right by 10 positions is used. This shift value was chosen to accommodate the maximum expected value of the multiplication result.

Given that a current in Data Buffer 0 is stored with an offset of Vref/2, or 8192 in the code, when multiplying this current by a voltage value, the offset (midpoint) must be subtracted. This ensures that when there is no current and voltage at the input, the power value is also zero.

For example, set the power threshold to 25 W. This value can be obtained, for instance, at a current of 4.5 A (static threshold = 11832) and a voltage of 5.5 V (static threshold = 9270). Firstly, it is necessary to subtract the midpoint from the current value: 11832 – 8192 = 3640. To set the power threshold to 25 W, it is necessary to configure the static threshold #1 value of the digital comparator as (3640 x 9270) >> 10 = 32951.

Figure 4 shows the overpower detection tested on the SLG47011. As can be seen from the waveform, neither the voltage nor the current reaches their thresholds, but the power does reach the threshold of 25 W.



Figure 4. Waveform Illustrating Overpower Monitor

2.4 Overtemperature Detection

Because the SLG47011 has a built-in Analog Temperature Sensor, it can be used to detect overtemperature. Consider, for example, a desired threshold of 100 °C. According to the Analog Temperature Sensor specifications, the Temperature Sensor output voltage at 100 °C is 0.5625 V.

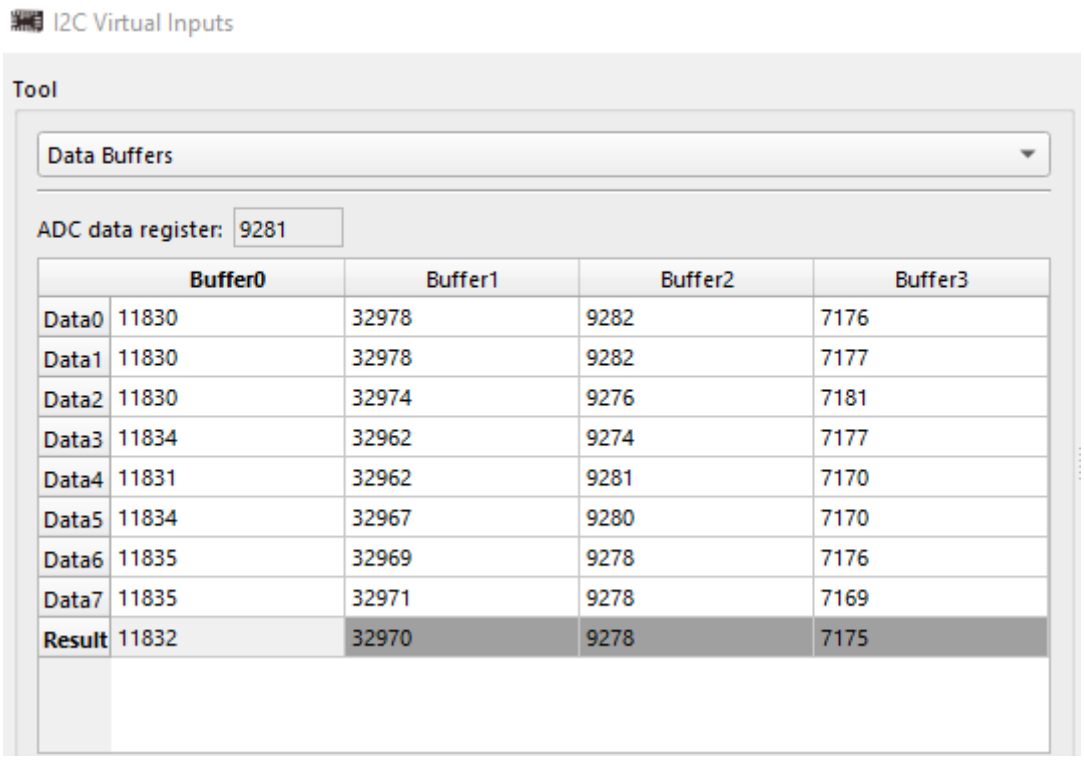
With the ADC Vref = 1.62 V, the digital comparator static threshold #2 value is:

$$TH2 = \frac{0.5625}{1.62}\ 16384 = 5688$$

During testing, the stored result in Data Buffer3, responsible for the sensor output, was read, and the value 0x1BF1 (7153) was obtained. This value is significantly below the threshold and is equivalent to approximately 0.707 V and 25 °C, respectively. Therefore, in this case, the OUT2 of the digital comparator has a LOW voltage, signifying the absence of the overtemperature. The flexibility of the SLG47011 allows for setting any threshold and detecting any temperature anomalies.

2.5 Data Logging

The SLG47011's Data Buffers can also be used for data logging. In this application note, Data Buffer 1 performs this function. At the moment of switching on and until the overpower occurs, it contains a zero value. However, when the overpower event happens, the HIGH-level signal from the comparator OUT1 is fed through the 2-bit LUT1 to the LOAD input of the buffer. With this signal, the buffer writes abnormal power values from the Math Core output. Users can read this buffer data via I^2C or SPI. Specifically, bytes 0x2224~0x2225, contain the result value of the buffer and based on these data, can judge the occurrence of the overpower event. If the read data value is above the static threshold value 32951, it indicates that the overpower has occurred. Figure 5 shows the Go Configure Tool for reading Virtual Inputs, namely, Data Buffers value during overpower.



	Buffer0	Buffer1	Buffer2	Buffer3
Data0	11830	32978	9282	7176
Data1	11830	32978	9282	7177
Data2	11830	32974	9276	7181
Data3	11834	32962	9274	7177
Data4	11831	32962	9281	7170
Data5	11834	32967	9280	7170
Data6	11835	32969	9278	7176
Data7	11835	32971	9278	7169
Result	11832	32970	9278	7175

Figure 5. Data Buffers Value during Overpower in Go Configure Tool

When the user reads the buffer and sees that an abnormal event has occurred, they can reset this value using the button “Reset Logger.” To filter out switch bouncing, a Delay macrocell DLY4 is used.

Thanks to the versatility of the SLG47011, it is possible to log current, voltage, or temperature instead of the power given in this design.

2.6 Anti-Aliasing Filters

Low-pass filtering is essential to eliminate any frequency components (harmonics) within the analog signal that surpass the Nyquist frequency. When frequency components in the analog signal exceed the Nyquist frequency, an undesired phenomenon called aliasing occurs. Resistor R2 and capacitor C3 form a filter with a cutoff frequency equal to $f_{-3dB} = 1/(2\pi R_2 C_3) = 3.3\ \text{kHz}$ and are intended to prevent aliasing when voltage is measured. Resistors R7, R8, and capacitor C4 form a filter for current measurement channel with a cutoff frequency equal to $f_{-3dB} = 1/(2\pi(R_7 + R_8)C_4) = 3.3\ \text{kHz}$.

2.7 PGA Offset Cancellation

The SLG47011 has built-in system calibration – specially designed customer calibration to simplify some differential mode measurements. In this design to eliminate PGA offset error for the current measurement channel the system calibration is used.

PGA channel 2 serves as the calibration channel. For this channel, the PGA settings must be configured the same as for channel 3, which is the main measurement channel. Additionally, it is recommended to short the inputs of the offset compensation channel and connect them with the same common-mode voltage as the measurement channel. Note that not all ADC channels have a calibration function. The compensation channel must either be channel 0 (for a pair of channel 0 and channel 1) or channel 2 (for a pair of channel 2 and channel 3). The compensation is activated by setting the System calibration register for the pair channel 0,1 or channel 2,3, and by applying a pulse to the ADC Calibration input.

To initiate the ADC calibration and conversion, it is necessary to provide a delay, which is achieved using a 100 ms delay (DLY4). CNT5 set calibration period and after 1 s starts calibration. CNT/DLY6 (One Shot) set conversion period.

2.8 Increasing Accuracy when Measuring Current

The above current measurement is quite accurate. However, this measurement does not take into account the sense resistor error and PGA gain error. With the SLG47011, it is possible to further improve the accuracy of current measurement by compensating for these errors. This makes it impossible to monitor power, as the Mathematical Core need to be used to compensate for the error. However, in this case, the current will be monitored with higher accuracy.

Because in this application note the current is measured in differential mode and the gain is applied to the difference between IN+ and IN- with an offset of the ADC Vref/2, before starting the compensation, subtracting the midpoint from the measured value is essential.

To implement the compensation, the real gain and sense resistor value must be measured by the user. Then, their errors must be calculated and added to determine a rational number, which is essentially a correction factor. The Math Core adjusts that error by multiplying the measured current value by constant K and right-shifting the result. Right-shifting by N bits is equivalent to division by 2^N. If K is set to 32768 (2^{15}) and the right-shifting value is set to 15, it is equivalent to multiplying the measured result by a factor of 1. So, no input data manipulation is being conducted. However, using this formula, by changing the K value, the input data can be trimmed to compensate for the PGA gain error and sense resistor error.

For example, if after measuring the real gain error and sense resistor value, a correction factor of 1.03 was determined, then the constant value K will be: 32768 × 1.03 = 33751. Then this constant K multiplies with the measured current value and shifts the result to the right by 15. The resulting value will contain the error-compensated current value.

3. Conclusions

This application note demonstrates the use of AnalogPAK SLG47011 as a monitor for current, voltage, power, and temperature. This is achieved by using the 4-channel 14-bit ADC, which allows the four signals to be monitored with high accuracy. The built-in calibration function allows for the implementation of PGA offset cancellation, which further improves measurement accuracy. The presence of the Mathematical Core allows for performing mathematical operations, which are used in this project to calculate power. Furthermore, the SLG47011 makes it possible to enable data logging, and all that in a miniature package of 2.0 mm x 2.0 mm.

4. Revision History

Revision	Date	Description
1.00	Sept 23, 2024	Initial release.

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