Application Note

Propagation Delay Considerations

AN-CM-283

Abstract

This application note illustrates the concept of propagation delay and how to estimate the propagation delay of different circuit blocks. It includes techniques that foster a more robust design implementation.

Contents

Figures

Terms and Definitions

Tpd	Propagation Delay
LUT	Look-Up Table
P DLY	Programmable Delay

1 References

[1] SLG46826, Datasheet, Renesas Electronics.

[2] AN-1046, Various Edge Detector Circuits, Application Note, Renesas Electronics.

2 Introduction

In digital electronics, the time needed to transmit a signal from one point (element) to another is called propagation delay (Tpd). The main factors that determine additional propagation delay of a signal through an integrated circuit are diode and transistor capacitances between the components of the ICs and inertia of the switching process in diode and transistors. This problem is exacerbated in synchronous systems, where the propagation of a signal through the IC is dependent upon the global clock frequency.

In practice, propagation delay is variable and depends on different factors including environment (for temperature) and electrical characteristics (for example supply voltage). GreenPAK, just like any other IC, has propagation delay resulting from its internal components like LUTs, DFFs, and others.

3 Propagation Delay Considerations in GreenPAK

The question of whether propagation delay is advantageous or detrimental is heavily dependent upon the specific circuit. On one hand, the signal delay caused by LUT propagation gives us the possibility to create helpful designs such as edge detectors in reset functions (see application note AN-1046), signal filters, or high frequency oscillators.

On the other hand, propagation can lead to undesirable and unpredictable logic combinations (often called “signal race”), which can negatively influence design functionality. Furthermore, Tpd limits the maximum frequency with which circuits can function. There are a lot of devices and applications that work on a minimum allowable switching frequency, like transmission protocols (I^2C, UART, SPI), Levels Shifters, and more. Depending upon the minimum propagation delay, certain applications may not be feasible.

We are going to consider this issue and give simple hints that can help to calculate propagation delay of different blocks and their combinational delay. We will also show problems that can be caused by propagation delay, along with the methods to avoid these problems.

To start, we must know where propagation delay timings can be found. To find a typical estimated propagation time for different blocks go to the datasheet. It is very easy to do it via GreenPAK designer. Choose the necessary IC (let’s say SLG46826). GreenPAK Designer automatically downloads the datasheet after clicking «Datasheet» in the «Help» window (see Figure 1).

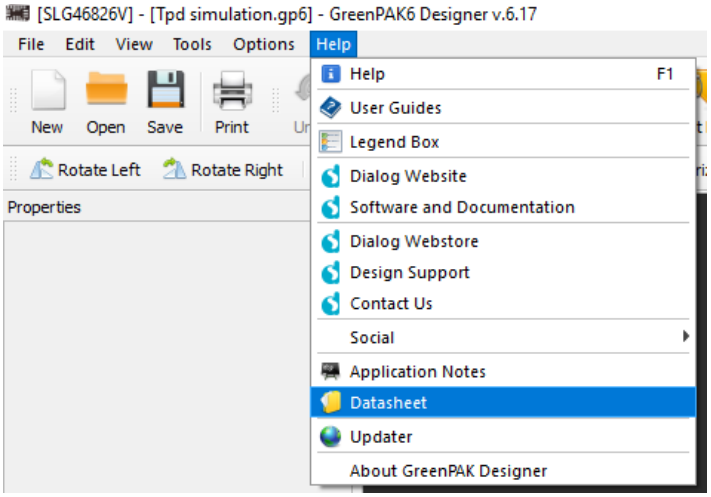

Figure 1 Opening Datasheet via Help Window

In the datasheet navigate to chapter 3.4 Timing Characteristics of propagation delay can be determined in Table 8 Typical Delay Estimated for Each Macrocell (**Note1:** Chapter and table number example is for the SLG46826 IC, it varies from chip to chip). Looking through the table, the datasheet of a certain block specifies the propagation delay variation for different voltage ranges at 25 ˚C (**Note 2:** All data shown are worst case and includes 6-sigma coverage factor).

3.4 TIMING CHARACTERISTICS

Table 8: Typical Delay Estimated for Each Macrocell at T = 25°C

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Multi-Function DFF Q	23	21	16	15	11	11	ns
tpd	Delay	Multi-Function DFF nQ	23	21	17	15	12	11	ns
tpd	Delay	Multi-Function DFF nRESET Q	--	29	--	21	--	15	ns
tpd	Delay	Multi-Function DFF nRESET nQ	31	--	22	--	16	--	ns
tpd	Delay	2-bit LUT	17	16	12	12	8	8	ns
tpd	Delay	3-bit LUT	17	17	12	12	8	9	ns
tpd	Delay	4-bit LUT	--	--	--	--	--	--	ns
tpd	Delay	Digital input to Low Voltage to PP 1X	35	222	24	150	16	96	ns
tpd	Delay	Digital input to with Schmitt Trigger to PP 1x	26	30	19	22	13	16	ns
tpd	Delay	Digital input to 1xPP	27	31	19	22	13	16	ns
tpd	Delay	Digital input to 2xPP	24	29	18	21	12	15	ns
tpd	Delay	Digital input to 1xNMOS	--	27	--	20	--	14	ns
tpd	Delay	Digital input to 2xNMOS	--	26	--	19	--	14	ns
tpd	Delay	Digital input to 1x3-State (Z to 0)	--	24	--	17	--	12	ns

Figure 2: Typical Delay Estimated for Macrocells in SLG46826

3.1 Estimating Propagation Delay for Different Blocks

Frequently, questions are asked: “what is the maximum frequency that GreenPAK can work with?” or “how do I estimate the delay of an input signal?”. To answer these questions, refer to the following Example 1 and Example 2.

Example 1

The datasheet of a certain block specifies that for 2-bit LUT (SLG46826), at the V_{DD} = 3.3 V rising edge delay, tpd (rising) = 12 ns, falling edge delay tpd (falling) = 12 ns. What is the maximum frequency that can go through the LUT?

$$t_{min} = t_{pd}(\text{rising}) + t_{pd}(\text{falling}) = 12\ \text{ns} + 12\ \text{ns} = 24\ \text{ns}$$

$$f_{max} = \frac{1}{t_{min}} = \frac{1}{24\ \text{ns}} = \frac{1}{24\times10^{-9}} = 41.66 \times 10^{6}\ \text{Hz} = 41.66\ \text{MHz}$$

As a result, the received frequency f_{max} = 41.66 MHz is the highest frequency that can pass through the 2 bit-LUT.

Example 2

Given: Logic circuit in Figure 3. Find: signal delay at the output pin (V_{DD} = 5 V).

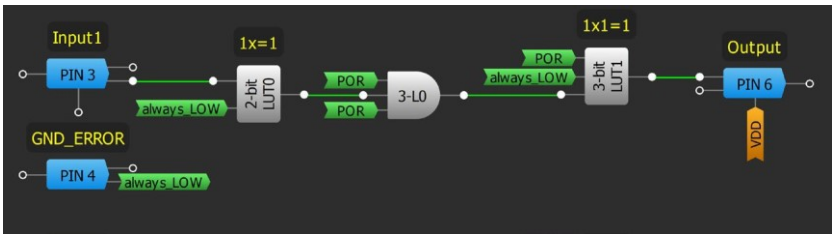

Figure 3: Example for Signal Delay

The solution includes two parts: rising edge delay and falling edge delay calculation.

$$t_{rising\_edge} = t_{pd}(rising_{DI_{to\ 1xPP}}) + t_{pd}(rising\_2bitLUT) + 2t_{pd}(rising\_3bitLUT) = 13\ ns + 8\ ns + 2 \cdot 8\ ns = 37\ ns$$

$$t_{falling\_edge} = t_{pd}(falling\_DI\_to\_1xPP) + t_{pd}(falling\_2bitLUT) + 2t_{pd}(falling\_3bitLUT) = 16\ ns + 8\ ns + 2 \cdot 9\ ns = 42\ ns$$

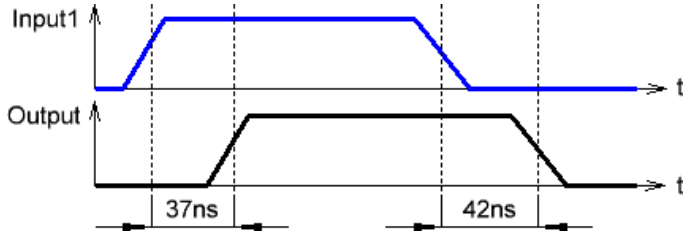

Figure 4: Serial Block Propagation Delay

Result: rising and falling edges of applied input signal are delayed 37 ns and 42 ns accordingly.

To fully understand potential issues related to Tpd, let's consider the simple logic circuit designed in SLG46826 (Figure 5). A signal that is applied to Input2 goes through an XOR block. The signal is fed into the XOR through IN0 directly, and with IN1 it passes via an AND-cell (Input1 is enable signal).

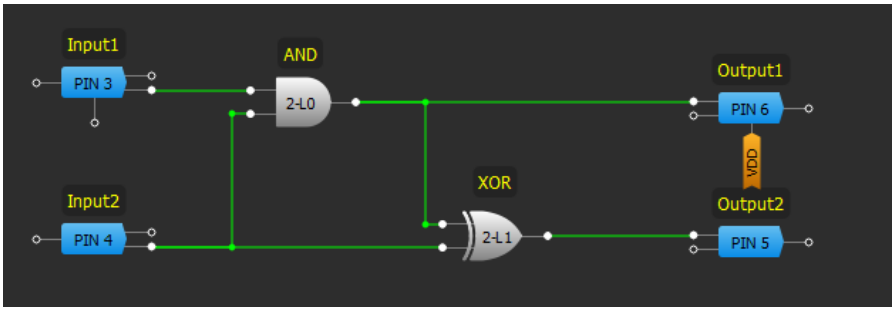

Figure 5: Design Example

So, how will propagation delay factor into this delay? When Input1 is Low, the XOR-gate works to buffer the Input2 signal. But, when it is High, XOR's IN1 will be applied with the signal from Input2, which will be delayed by AND cell propagation delay. This construction generates a short duration glitch on Output2 (Figure 6). Not good, especially for edge-dependent logic on the output.

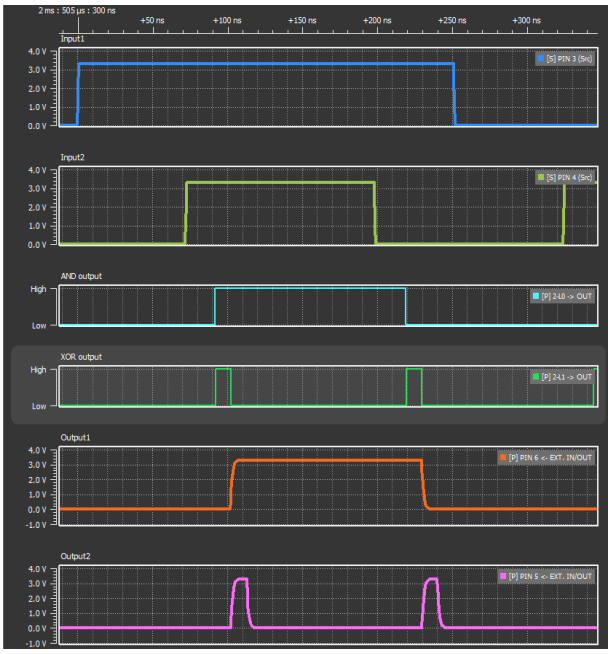

Figure 6: Design Example Simulation Result

The first and the easiest way to overcome glitches caused by this circuit scenario is to filter it using either P DLY block (configured as both edge delay) or FILTER (configured as filter) (see Figure 7). This method is reliable because of long delay time (up 834 ns for 4 cells P DLY, according to the datasheet). However, these specialized blocks may already be used for other functions or the input frequency is too high to use P DLY, so another method for filtering propagation glitches should be applied.

The second method is based upon providing the equivalent signal delay for the 2 XOR inputs. In order to implement this, a 2-bit LUT (2-bit LUT is an example, any other block can be used) is added between Input2 and the XOR's In0 (see Figure 8). The extra block equalizes the delays on XOR's inputs, which prevents that logic from creating short glitches on Output2 pin. **Note 3:** Because of the internal structure of LUT's, their inputs have different propagation delay times. The higher the input label number, the shorter the propagation delay it has. For example, IN1 has shorter propagation delay time than IN0.

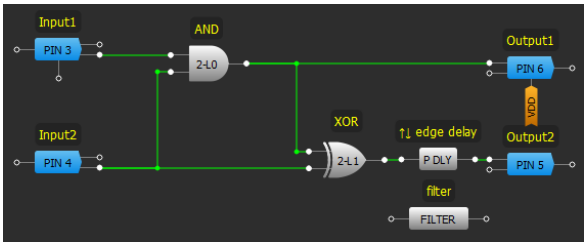

Figure 7: Filtering Glitches Dependent on Propagation Delay (Using P DLY (FILTER))

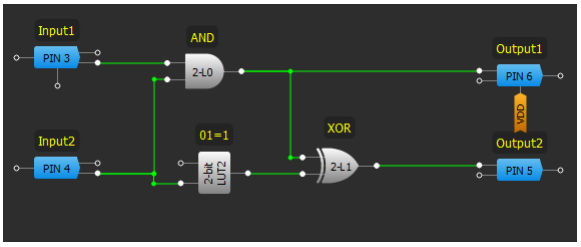

Figure 8: Filtering Glitches Dependent on Propagation Delay (Using LUT Buffer)

4 Conclusions

In this article, we considered the sensitivity of Tpd, and how to calculate total propagation delay time in GreenPAK designer. Two examples with maximum frequency and signal delay calculation were presented. Two different methods of filtering glitches caused by propagation delay were shown.

Revision History

Revision	Date	Description
1.0	13-Jun-2019	Initial version

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