Application Note

RTC Binary Counter – An Introduction

AN-CM-253

Abstract

This application note introduces the behavior of the GreenPAK™ Real-Time Counter (RTC) and outlines a couple of common design applications in which the RTC provides added configurability to circuit designers. The RTC macrocell serves as a 47-bit binary counter for lengthy timing applications but can also be modified to work as a 32-bit counter for creating shorter periodic signals. All register information and RTC specifications contained within this document reference the SLG46580/82/83 specifically, but the principles can be applied to other GreenPAK-based RTCs.

Contents

Figures

1   Terms and Definitions

ICs	Integrated circuits
LSBs	Least significant bits
RTC	Real-time counter

2   References

[1]   SLG46580/SLG46582/SLG46583, Datasheet, Renesas Electronics.

[2]   AN-CM-233, External Oscillator Solutions with GreenPAK, Application Note, Renesas Electronics.

Author: Craig Cary

3   Functionality Explanation

The RTC is comprised of the 15-bit and 32-bit counters shown in Figure 1 and Figure 2. By analyzing the datasheet's macrocell diagram in Figure 2, we can learn more about the configuration registers for this block as well as the associated matrix connections.
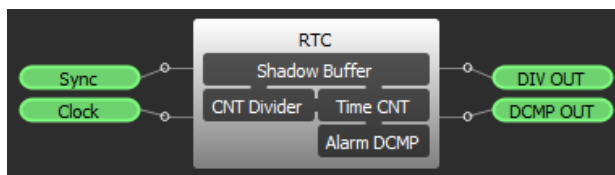

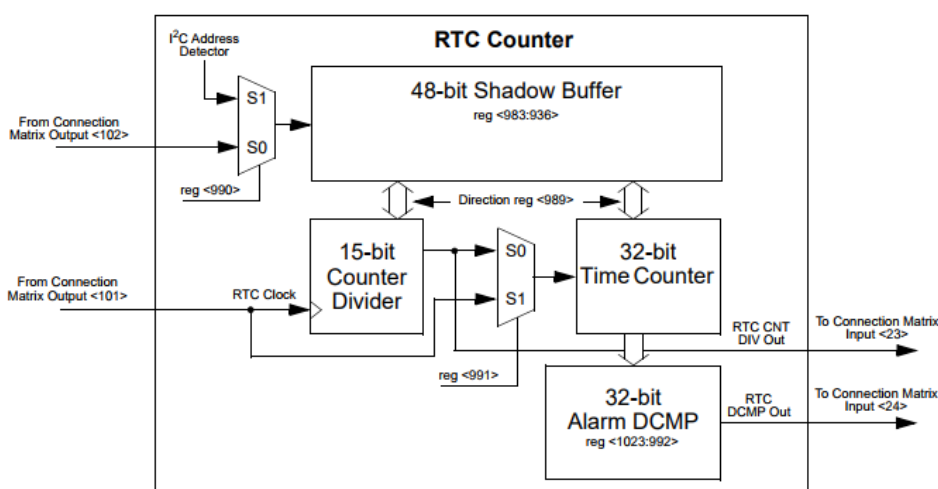**Figure 1: RTC Block Diagram - GreenPAK Designer**

Figure 2: RTC Counter Macrocell - SLG46580/82/83 Datasheet

This block's operation centers around the 32-bit time counter and the 32-bit alarm DCMP illustrated in Figure 2.The operation is simple: for every rising edge of its clock, the count value held within the time counter registers increments by one until it reaches 2^{32}-1. Upon reaching this value, the next clock signal causes the counter to "overflow" to zero and restart its count. When the registers of the time counter match the alarm DCMP registers, the "RTC DCMP Out" signal will go high. The RTC block operates in the 32-bit configuration as described above when the RTC's 32-bit counter is clocked, through mux selection, by the "RTC Clock" matrix output.
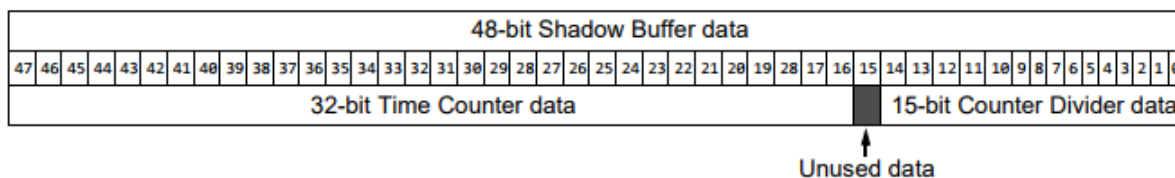
Please note that the RTC's clock input should have an active high pulse width exceeding 1 μs. Assuming a 50% duty cycle, this specification allows for input clock frequencies that are less than or equal to 500 kHz.

Looking back at Figure 2, we see the inclusion of another 15-bit counter within the RTC macrocell. This counter's output, when selected by the mux as the 32-bit time counter's clock, becomes the 15 least significant bits (LSBs) of a 47-bit counter configuration. The 15-bit counter overflows at 2^{15}-1 in the same way as previously described for the 32-bit counter. When the 15-bit counter overflows to "0", the 15-bit counter clocks the 32-bit counter and the RTC block outputs a "1" into the matrix through "RTC CNT DIV Out."

A key feature of the 15-bit counter is that it pairs well with a 32.768 kHz crystal oscillator. By selecting "32767" for the "Init. counter divider data" section of the RTC property window, the user can create 1-second pulses to clock the 32-bit time counter. This trivializes the process of creating arbitrary timing signals with the RTC block as you can simply calculate the desired delay in seconds and set the "Alarm DCMP value:" registers accordingly.

RTC Binary Counter – An Introduction

If you take another look at Figure 1 and Figure 2, you can see a matrix output named "SYNC" that connects to what we call the "Shadow Buffer." This 48-bit buffer can be used to both read from and write to the 15-bit and 32-bit counters. Figure 3 shows the register contents for this shadow buffer which are located at the I^{2}C addresses from 0x75 to 0x7A.

Figure 3: Shadow Buffer Register Contents

Register <989> controls the direction of the shadow buffer data transfer. When triggered by a rising edge of "SYNC," a digital "1" configures the RTC block to load the counter registers with the data stored inside the shadow buffer. Alternatively, a digital "0" in register <989> stores the current count value of each of the counters in the shadow buffer registers.

These register transfers are synchronized to one of two sources selected by register <990>: a rising edge on the "SYNC" matrix output as previously described or an I^{2}C trigger signal. A digital "0" selects the "SYNC" trigger and vice versa. The I^{2}C trigger signal is generated internally by reading (when register <989> is "0") or writing (when register <989> is "1") to any of the shadow buffer register addresses.

The shadow register guarantees a stable I^{2}C read from the RTC count registers when triggered via I^{2}C. If you were to perform an I^{2}C read on the counter registers directly, the register contents might increment during the read time, resulting in an incorrect I^{2}C read. By copying the register contents into the shadow buffer, the GreenPAK™ allows the RTC counters to continue operating while the user reads the shadow buffer registers.

For "SYNC" triggering and I^{2}C writing to the counter registers, we recommend stopping the RTC's clock to ensure correct data transfer. Please see the SLG46580/82/83 errata files for more information.

4   Integrating I^{2}C Reading & Writing with Periodic Signals

To create a periodic signal with the RTC block, the designer needs to configure the RTC block to reset each time the 32-bit count matches the alarm DCMP registers. When not using I^{2}C, resetting the counter requires the use of the "SYNC" input to transfer an initial count value from the shadow buffer to the 15-bit and 32-bit counters.

By feeding the "RTC DCMP OUT" signal to the "SYNC" input as shown in Figure 4, you can create the 5 second clock pulse shown in Figure 6. Please note that this signal is generated using an external 32.768kHz oscillator. This clock period can be modified for various applications by changing the external clock speed or the Alarm DCMP value displayed in Figure 5.
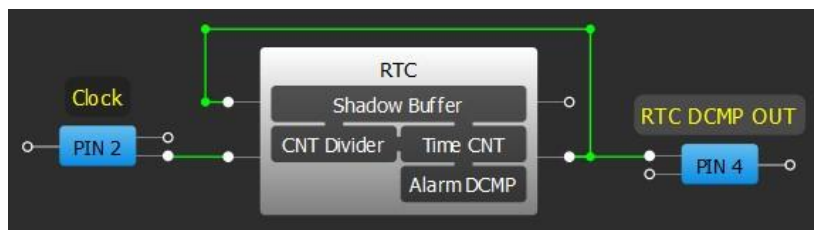
RTC Binary Counter – An Introduction

Figure 4: Five-Second Periodic Signal Design using the RTC

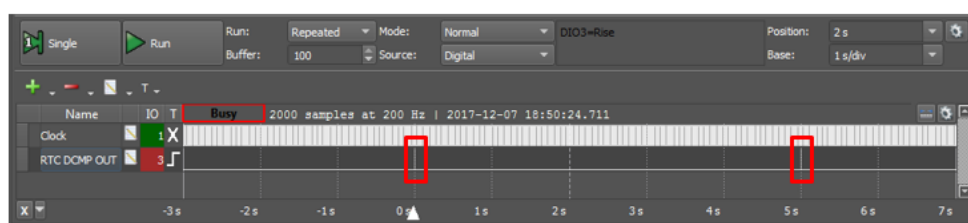**Figure 5: RTC Properties for
Five-Second Clock**

Figure 6: RTC Five-Second Clock Pulse

On occasion, a designer might want to perform an I²C read to check the current count of their periodic signal. This requires the user to follow a procedure as shown below:

- Follow the previously outlined procedure for generating periodic signals.
- Initialize read mode for the RTC block by changing reg <989> to "0".
- Change the trigger from "SYNC" to the I²C trigger by setting reg<990> to "1".
- Perform the I²C read of the desired addresses.
- Revert the trigger back to "SYNC" by setting reg <990> to "0".
- Reset the contents of the shadow buffer to the default values.
- Set the RTC block to write mode by changing reg <989> to "1".

Following these steps should enable you to read the register contents of the RTC while generating a periodic signal. It is important to note that the feedback mechanism is disrupted during I²C reads. If the time counter registers increment above the alarm DCMP registers during an I²C read, the "SYNC" input's rising edge won't trigger a counter reset. This behavior can be detected and rectified by analyzing the results of each I²C read. If any read is close to the alarm DCMP compare value and there isn't enough time to reset the device's settings back to its original periodic behavior, the software can manually generate the I²C commands to trigger the RTC reset.

5   Industry Application

The features explained in this application note can be customized for many different applications ranging from Bluetooth beacons to household electronics. You might have a temperature sensor, for example, that you want to wake up every hour to sample data. Similarly, you might want to put a Bluetooth beacon to sleep to conserve power. This block can periodically wake up the Bluetooth device to transmit its presence to nearby Bluetooth-compatible devices.

This block can also keep track of the life expectancy for various electronic devices. For example, many smoke detector and carbon monoxide alarms have a lifespan of about 10 years. This block provides designers with a simple, configurable, and low power timing solution for alerting homeowners of the need to replace their devices.

When clocked at 3.3V by a 32.768kHz oscillator, the use of the RTC block increases the SLG46580/82/83's current consumption by about 250nA. Please note that this value doesn't include the current consumption due to the clock source and GPIO switching, if applicable. For additional information regarding the creation of an external oscillator circuit using GreenPAK, please see AN-CM-233.

6   Conclusion

The RTC block provides a low power and cost-effective timing solution for designers to create both extended signals and short periodic alerts. When combined with the other GreenPAK logic elements, this block provides increased configurability to designers as they attempt to minimize current consumption, decrease PCB size, and reduce BOM costs for their applications.

Revision History

Revision	Date	Description
1.0	29-Aug-2018	*Initial Version*

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.