ClockMatrix / VersaClock 7

OCP NIC 3.0 Timing Synchronization: An Overview

Introduction

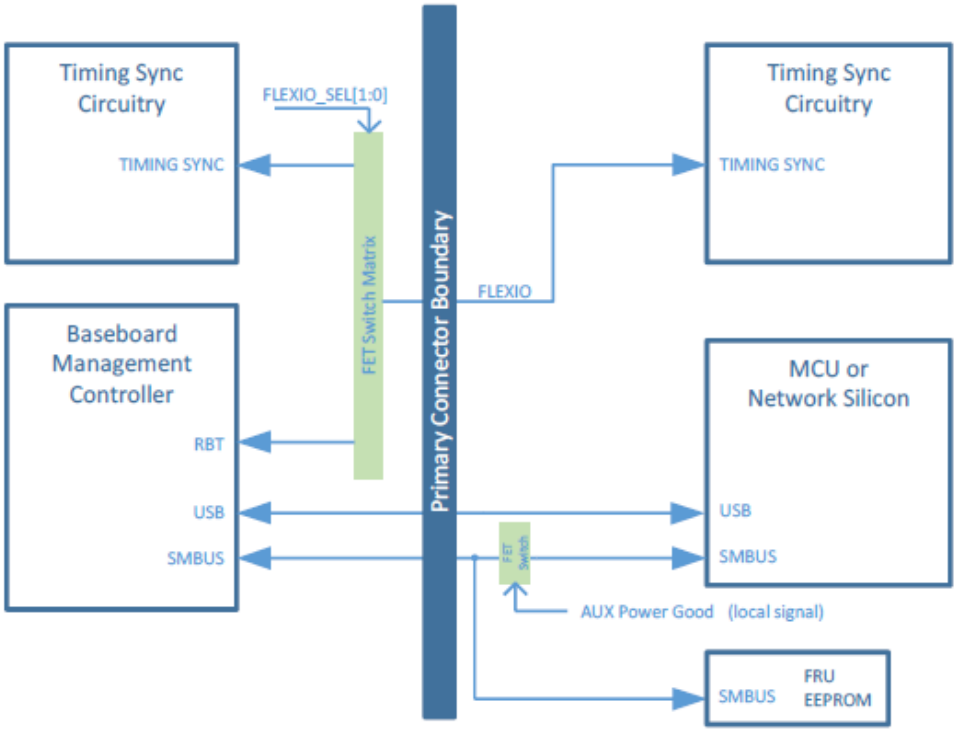
The OCP Timing Synchronization Card facilitates high-precision clocking to expand OCP infrastructure to support telecommunications and edge markets. It integrates network synchronization capabilities (supporting ITU-T and O-RAN) and adheres to Open Compute Project standards, ensuring interoperability, efficiency, and scalability. By leveraging Flex I/O and eliminating internal cabling, it provides an efficient interface between NIC and baseboard assemblies, addressing current challenges in timing synchronization.

Contents

1. What is the OCP Timing Synchronization Card?

The OCP Timing Synchronization Card is an innovative solution designed to integrate high-precision clocks into Open Compute Project (OCP) infrastructure. This innovation is pivotal for expanding the reach of OCP into telecommunications and edge markets where precise timing and synchronization are critical. It aligns with industry standards such as ITU-T and O-RAN for network synchronization and allows the future IEEE P3335 Standard for Architecture and Interfaces for Time Card to leverage and enhance this functionality.

OCP NIC 3.0 Standard makes use of Flex I/O pins, which repurposes RBT pins, to support discrete timing synchronization signals across the OCP NIC connector. This design choice eliminates the need for internal cabling between the NIC and baseboard assemblies, thereby streamlining integration and reducing complexity.



Source: OCP NIC 3.0 Design Specification, Figure 111 (Rel. 1.5.0)

Figure 1. OCP NIC 3.0 Block Diagram

By adhering to OCP standards, the timing synchronization card ensures interoperability, efficiency, and scalability across a variety of hardware platforms. This internal interface between the OCP NIC card and the baseboard not only simplifies assembly but also addresses the growing demand for seamless integration in data centers and edge computing environments.

2. Timing Synchronization Mode

Current timing synchronization NICs typically rely on external cables, such as 50-ohm coaxial cables, to propagate timing synchronization signals. While functional, this approach presents significant challenges. Propagating timing across multiple NICs within a single system, or even multi-systems, often proves cumbersome and error-prone.

The preferred alternative is a 10MHz signal embedded with a 1 Pulse Per Second (ePPS) signal. This configuration offers improved reliability and simplifies deployment. A secondary option involves a 10MHz signal with a separate 1PPS, providing flexibility for specific use cases. These advancements in synchronization methods reduce complexity and enhance the overall performance of timing-critical applications.

2.1 RX Frequency and Synchronization

The OCP NIC 3.0 Timing Synchronization mode incorporates several input features routed as 50-ohm single-ended nets:

- **TS[0:1]_RX_FREQ:** Typically receives a 10MHz reference clock with an embedded ePPS signal. The 10MHz carrier frequency maintains a 50% duty cycle, while the ePPS signal adheres to a 25% duty cycle. Alternatively, this pin may carry a 10MHz reference clock with a separate 1PPS signal on the TS_RX_SYNC pin.
- **TS[0:1]_RX_SYNC:** Usually receives a 1PPS signal when paired with the TS_RX_FREQ pin operating as a 10MHz reference clock. It can also function as a separate 10MHz frequency source. This pin operates at a 3.3V TTL logic level and, if unused, should be terminated with a 10kΩ resistor to ground.
- **TS[0:1]_GPI:** Driven high by the OCP NIC, this signal indicates potential issues such as Loss of Signal (network port disconnection) or Loss of Lock (timing signals unsynchronized with a primary clock). These signals operate at 3.3V and should also be terminated with a 10kΩ resistor to ground if unsupported by the baseboard.

These input configurations ensure that the timing synchronization signals are robust, precise, and adaptable to various operational scenarios.

2.2 TX Frequency and Synchronization

The OCP NIC 3.0 Timing Synchronization mode also features output capabilities routed as 50-ohm single-ended nets:

- **TS[0:1]_TX_FREQ:** Drives a 10MHz reference clock with an embedded ePPS signal. Similar to its RX counterpart, the carrier frequency and ePPS signal maintain 50% and 25% duty cycles, respectively. It can optionally carry a separate 1PPS signal on the TS_TX_SYNC pin.
- **TS[0:1]_TX_SYNC:** Typically drives a 1PPS signal when paired with the TS_TX_FREQ pin operating as a 10MHz reference clock. This pin can also serve as a standalone 10MHz frequency source. It operates at a 3.3V TTL logic level and requires termination with a 10kΩ resistor to ground if unused.
- **TS[0:1]_GPO:** While not supported in the current release, this pin is designated as an active-high output from the baseboard to the OCP NIC. For now, it is left as a no-connect on both the baseboard and NIC.

These output mechanisms complement the input features, ensuring seamless timing synchronization and signal propagation across systems.

3. OCP NIC 3.0 Clock Tree

The OCP NIC 3.0 clock tree is designed to prioritize backward compatibility and operational efficiency. Key features include:

- **Default State:** The TS_RX_FREQ and TS_RX_SYNC pins remain in a high-impedance (High-Z) state before being enabled by the baseboard. This precaution prevents potential issues when the NIC is plugged into baseboards that only support RBT functionality.
- **Backward Compatibility:** To ensure compatibility with legacy systems, the RBT_ARB_IN and RBT_ARB_OUT pins are tied together when operating in TSMode.

3.1 Using ClockMatrix

ClockMatrix natively supports ePPS clocks, making it a perfect fit for Time Synchronization mode on the NIC.

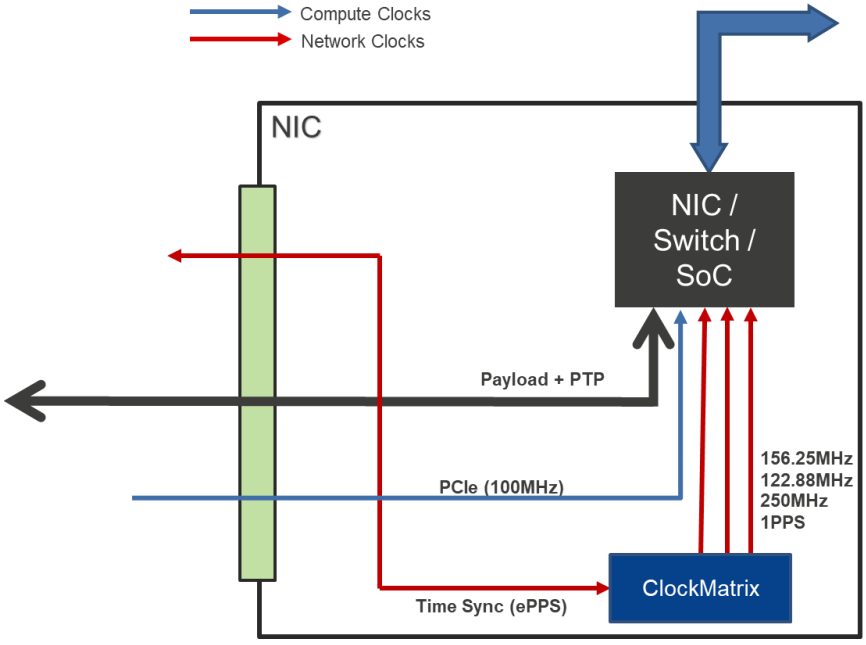


Figure 2. OCP NIC 3.0 with ClockMatrix

Along with supporting multiple clock input and output options for clocking, it also adheres to many synchronization standards and recommendations. Available Linux-based drivers based on the PTP Hardware Clock (PHC) subsystem allow for quick integration of software on the host, supporting open-source software such as Linux PTP (ptp4l).

3.2 Using VersaClock 7

The VersaClock 7 family introduced synchronization capabilities along with PCIe clocking.

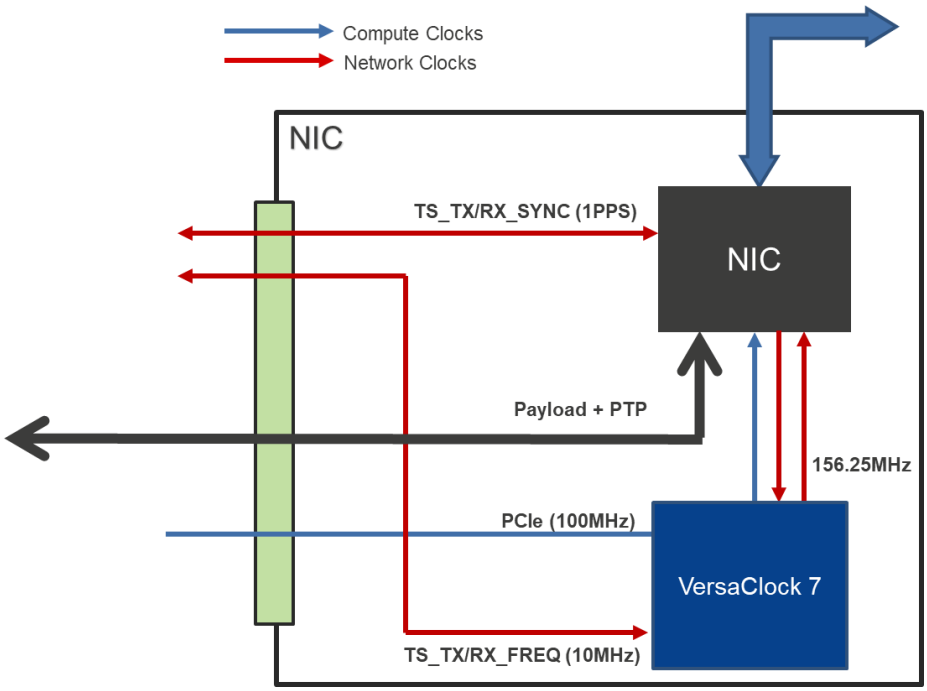


Figure 3. OCP NIC 3.0 with VersaClock 7

Along with supporting PCIe Gen6, it also adheres to many frequency synchronization standards and recommendations.

4. OCP Baseboard Clock Tree

The OCP baseboard clock tree works in tandem with the NIC 3.0 clock tree to provide a cohesive timing synchronization solution. It is optimized for efficient signal routing and minimal interference, ensuring that both factory and field deployments achieve the desired performance metrics.

By integrating seamlessly with the NIC, the baseboard clock tree eliminates the need for external cabling and simplifies the overall system architecture. This streamlined approach reduces installation time, minimizes errors, and enhances the scalability of OCP-based infrastructure.

Renesas' ClockMatrix devices natively support ePPS clocks, multiple clock inputs and outputs, and multiple synchronization channels; making them a perfect fit for Time Synchronization Mode on the Baseboard.

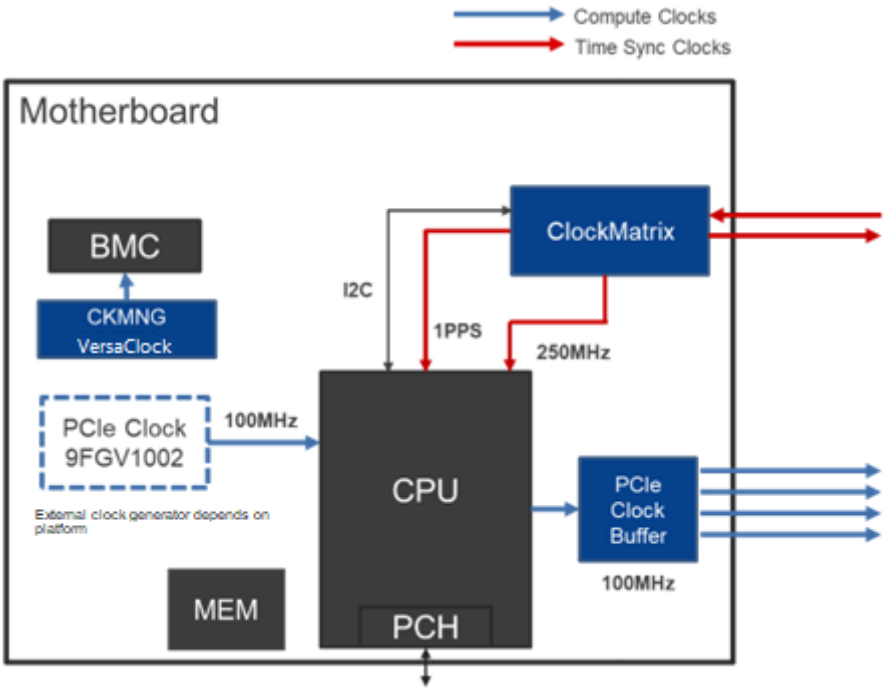


Figure 4. OCP Baseboard with Renesas Timing

5. Conclusion

The OCP NIC 3.0 Timing Synchronization Card represents a significant advancement in the field of timing synchronization. By adhering to OCP standards and leveraging innovative technologies such as Flex I/O, it addresses the unique challenges of telecommunications and edge markets. Its robust input and output configurations ensure precise timing signals, while the integration of the NIC and baseboard clock trees simplifies deployment and enhances scalability.

This groundbreaking solution paves the way for more efficient, interoperable, and scalable hardware platforms, reinforcing the OCP's commitment to open standards and collaborative innovation.

6. Revision History

Revision	Date	Description
1.01	Jan 16, 2025	Updated Figure 4.
1.00	Jan 15, 2025	Initial release.

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