

Renesas RA Family

Application Design using RA8 First Stage Bootloader

Introduction

The Renesas RA8 Series MCUs listed below make available a "First Stage Bootloader" (FSBL), which is masked in ROM and can execute after reset to verify the OEM firmware programmed in the on-chip flash in the single-chip operating mode. Due to its immutable nature, the FSBL provides a silicon-based Root of Trust (RoT).

In order to use the FSBL, the OEM firmware must be verified during production programming. The MCU's factory boot firmware provides this capability.

This application project provides a walk-through for how to establish the credentials used by the factory boot firmware and the FSBL to verify the OEM firmware. The application project then demonstrates the verification of the firmware using either technique available: Cyclic Redundancy Check 32 (CRC32) integrity verification or Elliptic Curve Cryptography (ECC) NIST P256 signature authentication combined with HMAC-SHA256 authentication.

Required Resources

Target Devices

Below are the Renesas MCU products to which the information within this document is applicable:

- RA8M1
- RA8D1
- RA8T1

Software and development tools

- e² studio IDE v2023-10
- Renesas Flexible Software Package (FSP) v5.1.0

The links to download the above software are available at <u>https://github.com/renesas/fsp</u>.

- SEGGER J-Link[®] USB driver v7.920 or later (<u>SEGGER J-Link</u>)
- Renesas Secure Key Management Tool v1.05 or later
- <u>Renesas Flash Programmer v3.13 or later</u>
- GNU Privacy Guard for Windows: <u>Gpg4win</u>
- <u>Renesas Device Lifecycle Management Server</u>

Hardware

- EK-RA8M1, Evaluation Kit for RA8M1 MCU Group (renesas.com/ra/ek-ra8m1)
- Workstation running Windows[®] 10 and the Tera Term console or similar application.
- One USB device cable (type-A male to micro-B male)



Prerequisites and Intended Audience

This application project assumes that you have experience using Renesas e² studio IDE. In addition, knowledge on application boot loading and cryptographic algorithms is desirable. Prior to exercising this application project, the user should install all the tools mentioned in the **Software and development tools** section and read the following sections in the RA8M1 Hardware User's Manual. This will provide a background for some discussions in this application project. Reading these sections will also provide convenience for the user to dig deeper and extend the learning from this application project.

- Section: Security Features
- Section: Option-Setting Memory
- Section: Flash Memory

Furthermore, the user should have the Renesas RA Secure Key Injection Application Project (R11AN0496) handy. The user will need to follow several sections in this application project to support the FSBL usage. A non-TrustZone[®] application is used for demonstration in this application project. Users who are interested in using the FSBL with TrustZone projects can preview section 4.1 to understand the updates needed.

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1. Introduction to the First Stage Bootloader

1.1 Overview

In a secure system, an application program must be executed only after confirming that it has not been altered, either maliciously or inadvertently. This confirmation, typically performed by a boot loader, can be a simple integrity check, or it can involve signature verification to ensure authenticity. However, it is important to note that the legitimacy of the boot loader itself must also be guaranteed.

When the FSBL is enabled, there are two options to verify the product firmware.

- Integrity check using CRC32. This check will be performed at initial MCU programming and prior to execution.
- Authenticity check. During initial MCU programming, the application is authenticated using ECDSA with the secp256r1 (NIST P256) ECC curve. Prior to execution, the application is authenticated using HMAC-SHA256 with the MCU's HUK.

The secure boot sequence is often implemented in stages, starting with an immutable entity to ensure a strong Root of Trust (RoT). The RA8 Series MCUs include an immutable First Stage Bootloader (FSBL), which provides this RoT as a starting point for a secure boot sequence. Typically, the FSBL validates the OEM's bootloader, which then validates the remainder OEM firmware, forming a "Chain of Trust" (refer to Figure 1 Case 2 for the authenticate path) for booting the system. Thus, the availability of the FSBL allows for securely updating the OEM bootloader.

The following is a high-level representation of the usage of the FSBL in an embedded system in MCU single chip mode.



Figure 1. Usage of the FSBL in a Single Chip Mode

Note that in the RA8 MCU Hardware User's Manual, the description is centered around the second use case where a Second Stage Bootloader exists. The Hardware UM uses "OEM_BL" to refer to both usages when it comes to operations related with FSBL. In this release of the application project, only the first usage is covered. To be consistent with the Hardware User's Manual, we will use "OEM_BL" to refer to OEM product firmware.

As shown in the image below, the FSBL registers are mapped into the **Data flash option setting memory** area. The programming of these registers can be handled by the Serial programming/ JTAG or SWD programming when using the IDEs (for example, e² studio). They are programmed via the boot access modes when using RFP to program the applications. As a result, the settings made in these FBSL registers will determine the MCU's operation state coming out of Reset and the decision of whether to jump directly into OEM_BL.





Figure 2. Data Flash Option Setting Memory Area RA8x1

The lockable data flash option setting memory area can be locked via the Renesas Flash Programming tool during production or other production programs. Be very cautious – after these areas are locked, they cannot be unlocked to reenable the configuration of these registers. Locking up these registers should be avoided during application development.



Figure 3. Using RFP to Lock the Lockable Data Flash Option Setting Registers



1.2 FSBL based Booting Options

When the FSBL is enabled, there are two schemes supported for the verification of OEM_BL.

- CRC32 boot: in this case, the application integrity is validated using CRC32.
- Secure boot: in this case, the application authenticity is validated upon programming using the secp256r1 ECC curve (NIST P256). The application authenticity is validated upon execution using HMAC-SHA256 with the MCU's Hardware Unique Key.

The FSBL configuration options can be selected via the RA Smart Configurator **BSP** tab. The configuration settings for the FSBL shown below demonstrate an example where **Secure boot with report measurement** is selected. Adjust these settings based on the security objectives of the OEM application being developed. Refer to the "Build Time Configurations" for your MCU in the RA Flexible Software Package Documentation > API Reference > BSP > MCU Board Support Package for more explanations of the various Stack properties.



Figure 4. FSBL Configurations

Applications targeting RA8 Series MCUs are not required to use the FSBL. The FSBL can be bypassed. This is configured by setting the **FSBLEN** property to **Disabled**. In this case, there is no verification of the application code during either programming or prior to execution. The MCU can be used in the same way as other RA MCUs that do not include an FSBL.

Since the FSBL will take some time to perform the verification, it may be acceptable to skip the verification process after certain types of resets. Configure the **FSBLSKIPSW** property to **Enabled** to skip the FSBL upon a software reset. Similarly, configure the **FSBLSKIPDS** property to **Enabled** to skip the FSBL upon reset from at Deep Software Standby Reset.

In both CRC and Secure boot use cases, it is possible to choose with or without "**report measurement**" option as shown in Figure 5. Verification Options Using FSBL.



FSBL Control 1 (FSBLCTRL1) FSBLEXMDFSBLEN Secure boot with report measurement FSBL Control 2 (FSBLCTRL2) CRC boot with report measurement PORTPN CRC boot with report measurement PORTGN Secure boot with report measurement		
FSBLEXMDFSBLEN Secure boot with report measurement V FSBL Control 2 (FSBLCTRL2) CRC boot without report PORTPN CRC boot with report measurement PORTGN Secure boot without report	 FSBL Control 1 (FSBLCTRL1) 	
FSBL Control 2 (FSBLCTRL2) CRC boot without report PORTPN CRC boot with report measurement Secure boot without report Secure boot without report Secure boot without report	FSBLEXMDFSBLEN	Secure boot with report measurement
PORTPN CRC boot with report measurement PORTGN Secure boot without report	 FSBL Control 2 (FSBLCTRL2) 	CRC boot without report
PORTGN Secure boot without report	PORTPN	CRC boot with report measurement
	PORTGN	Secure boot without report

Figure 5. Verification Options Using FSBL

If report measurement is selected, the information in Figure 6 is output to the memory address stored in the SAMR register, which is configured using the **FSBL Measurement Report Address** property under the BSP tab (refer to). The contents in the Measurement Report are generated to meet the requirements of the <u>ARM</u> <u>Platform Security Architecture Attestation API</u>. The latest version of the ARM PSA Certified Attestation API manual from this link has explanations on the usage of these entities.



Figure 6. Content and Location of the Measurement Report

For CRC boot, the Signer ID will output the calculated CRC 8 times. Each CRC32 is 4 bytes, and the Signer ID is 32 bytes. Using **CRC boot with report measurement** is a rare use case.

Upon a failed boot, the high level is output to the port set by the FSBLCTRL2 register (refer to Figure 4) and the MCU goes to CPU Sleep mode. For example, in Figure 4, Pin 107 is selected as the pin to output a high level when the secure boot fails. This pin controls the red LED on board, which will be turned on with a failed boot sequence.

1.2.1 OEM_BL Verification Overview During Production Programming

During production programming, the OEM_BL is validated by the MCU boot firmware using ECDSA. The RA8 MCU offers access to the MCU boot mode through JTAG, SCI and USB interfaces. For details of the boot mode, refer to section **Details of Operating Modes** in the Hardware User's Manual.

After establishing communication with the boot firmware (for example, through RFP), the boot firmware injects the hash of the OEM_ROOT_PK to unmapped flash area as the RoT of the system. Once the OEM_BL is programmed to the MCU, the boot firmware then reads the **Image Version** number in the code certificate. If the **Image Version** is a higher version than previously programmed, the boot firmware calculates the hash of the OEM_ROOT_PK (which is stored in the key certificate) and compare with the Hash of OEM_ROOT_PK that is programmed to the MCU. If the hash of the OEM_ROOT_PK matches, the OEM_BL_PK in the code certificate is verified by comparing the calculated hash of the OEM_BL_PK to the hash residing in the key certificate. Once the OEM_BL_PK is verified, it will be used by the boot firmware to verify the OEM_BL using the signature in the code certificate. If the OEM_BL is validated, the boot firmware increments the anti-rollback counter up to the Image Version written in the code certificate and calculates the OEM_BL_digest are then programmed to the MCU.





Figure 7. OEM_BL Validation Flow in Production Programming Mode



1.2.2 OEM_BL Verification During Single-Chip Operation

In single chip mode, the OEM_BL is validated by the FSBL using HMAC-SHA256. Assume the OEM_BL production programming is successful. When **Secure boot** is enabled, the immutable FSBL in ROM is executed after MCU reset. The FSBL calculates the HMAC value (the OEM_BL_digest) of the OEM_BL plus the code certificate and compares it to the expected OEM_BL_digest, which is stored in the code flash during production programming. If the OEM_BL_digest matches, the FSBL jumps to the OEM_BL. If not, then FSBL will transition the CPU to a sleep mode and optionally output a level 'high' to a port pin of user's choice.

When CRC boot is selected, the FSBL calculates the CRC of the OEM_BL and compares it to the expected CRC value, which is located in the code certificate. If the CRC values match, the FSBL jumps to the OEM_BL.



Figure 8. OEM_BL Validation in Single-Chip Mode

1.2.3 Advantages of Using HMAC-SHA256 in Single-Chip Mode

The HMAC-SHA256 provides advantages based on the RA8 MCU hardware features:

- Security is maintained because the HMAC "shared secret" (the MCU's HUK) is never exposed outside the MCU.
- The HUK is MCU unique and provides anti-cloning protection.
- The operation is significantly faster than verifying a digital signature.
- The HMAC-SHA256 operation is Quantum-resistant.



1.3 Details of the Credentials Used in Authenticity Checking

This section describes the chain of trust of the system based on ECDSA and HMAC-SHA256 operations.

The chain of trust of the system is established with the following components.



Figure 9. Chain of Trust

The following sections describe the format and content of the various credentials described in Figure 9 and their usage during production programming and prior to production firmware execution.

1.3.1 Root of Trust

Two sets of secp256r1 ECC Key Pairs must be generated when using the Secure boot:

- OEM_ROOT_PK: the public part of the OEM Root Key pair
- OEM_ROOT_SK: the private (secret) part of the OEM Root Key pair
- OEM_BL_PK: the public part of the OEM_BL Key pair
- OEM_BL_SK: the private (secret) part of the OEM_BL Key pair

The SHA256 hash of the OEM_ROOT_PK is stored in the lockable data flash area (HOEMRTPK) as the Root of Trust (RoT) using the secure key injection process described in section "Secure Key Injection" in the Hardware User's Manual for your RA8 MCUs. The injection of the Root of Trust is done during the production programming of the application.

1.3.2 Key Certificate

The key certificate plays a critical role during production programming for HMAC boot enabled applications. Below is some important information about the creation and usage of the key certificate.

- The key certificate is signed by OEM_ROOT_SK.
- The OEM_ROOT_PK is included in the signed key certificate and is verified by the HOEMRTPK.
- The hash of the OEM_BL_PK is included in the key certificate. It will be used by the boot firmware to verify the OEM_BL_PK.
- The key certificate is discarded after the OEM_BL PK is validated.





Figure 10. Key Certificate to Verify the OEM_BL_PK

1.3.3 Code Certificate

The code certificate plays a critical role during MCU production programming as well as during MCU single chip operating mode.

- The code certificate is signed by OEM_BL_SK.
- The OEM_BL_PK is included in the code certificate. It is verified by its hash, which was stored in the key certificate. The OEM_BL_PK will then be used to verify the OEM_BL's signature, included in the code certificate.
- The code certificate contains credentials used for the FSBL verification process during single-chip operation mode. It must be programmed into flash memory (code or data flash) after the OEM_BL is programmed.
- The application **Image Version** number is part of the code certificate when using Secure boot. The valid Image Version is 1 to 64, which implies the application can be updated 64 times when FSBL with Secure boot is enabled. The FSBL implements an anti-rollback scheme. Therefore, to update to a new application image, the next new image must have a version number higher than the previous application image. For more details on the operation and explanation of the usage of the "Image Version" number, please refer to the **Anti-Rollback Counter** Section of the Hardware User's Manual.
- The code certificate location in flash must be specified in the SACC0 register or SACC1 register. SACC0 register specifies the start address of the code certificate when the lower bank is Bank 0 in dual bank mode or when the startup area is the default block (block 0) in linear mode. The SACC1 register specifies the start address of the code certificate when the lower bank is Bank 1 in dual bank mode or when the startup area is the alternate block (block 1) in linear mode. Configuration of SACCx registers is handled by the RA Smart Configurator and the FSP Board Support Package (BSP). Figure 4 provides an example configuration for the Code Certificate programming location. Be sure to adapt it as required for your specific application.
- For FSBL signature authentication, the TLV EXPECTED_CRC field is not used. The structure of the Code Certificate, however, remains unchanged.
- After successful validation of the OEM_BL during production programming, the HMAC-SHA256 digest (OEM_BL_digest) of the OEM_BL plus the code certificate is then calculated by the boot firmware using the MCU's HUK. The boot firmware will program the OEM_BL_digest in the memory area immediately following the Code Certificate.



Field		Size [byte]	Description
TLV EXPECTED_MAC	Type & Length	4	Fixed value 0x30184008
	Value	32	Unique OEM_BL_digest in each MCU

Figure 11. Details of the OEM_BL_digest



Figure 12. Code Certificate to Verify the OEM_BL using HMAC Boot



1.3.4 Summary of the Usage of the Credentials in Production Programing, Secure Boot

During the firmware application programming stage, the following items will be programmed on to the MCU:

- Hash of OEM_BOOT_PK
- OEM_BL (application image)
- Code Certificate
- OEM_BL_digest

The following figure summarizes the overall workflow using SKMT and RFP during production programming using Secure boot. A step-by-step walk-through of using SKMT and RFP is provided in section 2.



Figure 13. Summary of Credential Usage during Production Programming for Secure Boot

1.4 Details of the Credentials Used in Integrity Checking

Validation using CRC is relatively simple. The differences from the **Secure boot** process described above are:

- The OEM Root Public Key (OEM_ROOT_PK) is not used. Therefore, there is no requirement for creating an OEM_ROOT key pair nor injecting the OEM_ROOT_PK to create the OEM_ROOT_PK's hash (HOEMRTPK).
- The Key Certificate is not used, and the OEM_BL is not signed. Therefore, there is no requirement to create an OEM_BL key pair.
- There is no anti-rollback policy enforced. Therefore, the anti-rollback counter (ARC_OEMBLn) and the Image Version field in the Code Certificate are not used.
- During production programming, the boot firmware calculates the CRC32 of the OEM_BL. If the calculated CRC32 value matches the value in the code certificate, the boot firmware programs the code certificate at the location specified by the SACC0/1 register.
- During single chip operation mode, the FSBL calculates the CRC32 of the OEM_BL compares it to the CRC in the code certificate. If the CRC values match, the FSBL jumps to the OEM_BL.

1.4.1 Code Certificate

The code certificate of the CRC boot includes the following components. The TLV ECCPUBKEY and TLV_EXPECTED_SIG fields do not exist in the Code Certificate. The Image Version field is not used during booting.





Figure 14. Code Certificate to Verify the OEM_BL using CRC Boot

1.4.2 Summary of the Usage of the Credentials in Production Programing, CRC boot

During the firmware application programming stage, the following items will be programmed on to the MCU:

- The OEM_BL (application image)
- The Code Certificate

The following figure summarizes the overall workflow using SKMT and RFP during production programming using CRC boot. A step-by-step walk-through of using SKMT and RFP is provided in section 3.



Figure 15. Summary of Credential Usage during Production Programming for CRC Boot



1.5 Using the FSBL with Renesas Secure Factory Programming

Renesas RA8 Series MCUs support programming an encrypted firmware image with Secure Factory Programming, enabling secure firmware programming in a non-secure environment. Renesas Secure Factory Programming can be implemented with or without FSBL. When FSBL is used with secure factory programming, the application must have FSBL configured. FSBL must be activated after the encrypted image is written into the MCU and before issuing a reset. To erase the device and turn off FSBL after secure factory programming, the MCU Initialize Device command should be performed (for example using the RFP as shown in Figure 23). For more details on the Secure Factory Programming, refer to the **Secure Factory Programming** section in the Hardware User's Manual.

2. Authenticated Production Programming and HMAC-SHA256 Boot Demonstration

This section provides a walk-through of generating the credentials for the authenticated production programming and HMAC boot. A simple blinky project is used to demonstrate this process. The procedure for injecting the Root of Trust has a lot in common to the secure key injection process described in R11AN0496. This application note will refer to sections in R11AN0496 whenever appropriate.

2.1 Prepare two Sets of ECC secp256r1 Key Pairs

As explained in the previous sections, two sets of ECC secp256r1 key pairs are needed to generate the chain of trust of the system. In this application project, using OpenSSL to generate the key pairs is demonstrated. Additionally, this writeup demonstrated using the NIST CAVP ECDSA test vectors to create the chain of trust.

2.1.1 Using OpenSSL to Generate the ECC Key Pairs

For Linux, get the OpenSSL from here: <u>https://www.openssl.org/source/</u>. For Windows, get the OpenSSL from here: <u>https://slproweb.com/products/Win32OpenSSL.html</u>.

After downloading OpenSSL, install it and navigate to the \bin folder from a command prompt.

The following command generates a pair of OEM Root Key Pair:

C:\Program Files\OpenSSL-Win64\bin>openssl ecparam -name prime256v1 -genkey -noout - out c:\RA8_FSBL\openssl_keys\oem_root_private_key.pem

The following command generates the public key for the OEM Root Key Pair.

C:\Program Files\OpenSSL-Win64\bin>openssl ec -in c:\RA8_FSBL\openssl_keys\oem_root_private_key.pem -pubout -out c:\RA8_FSBL\openssl keys\oem root public key.pem

read EC key

writing EC key

The same commands can be used to generates a pair of OEM_BL Key Pair:

C:\Program Files\OpenSSL-Win64\bin>openssl ecparam -name prime256v1 -genkey -noout - out c:\RA8_FSBL\openssl_keys\oem_bl_private_key.pem

The following command generates the public key for the OEM_BL Key Pair.

C:\Program Files\OpenSSL-Win64\bin>openssl ec -in c:\RA8_FSBL\openssl_keys\oem_bl_private_key.pem -pubout -out c:\RA8_FSBL\openssl keys\oem bl public key.pem

read EC key

writing EC key

2.1.2 Download NIST CAVP Test Vectors as ECC Key Pairs

The following NIST Cryptographic Algorithm Validation Program (CAVP) test vectors are used in this application project to demonstrate booting with HMAC with FSBL is used.

The CAVP NIST test vectors can be downloaded from the following link. The ECDSA vectors are what we will use.

Cryptographic Algorithm Validation Program | CSRC (nist.gov)



IESt Vector	3		
Use of these test vec	tors does not replace validation ob	tained through the CAVP.	
The test vectors linke 186-2 and FIPS 186-4	d below can be used to informally ve) using the validation systems <u>listed a</u>	rify the correctness of digital signature algo <u>Ibove</u> .	orithm implementations (in FIPS
Response files (.rsp) exactly.	: the test vectors are properly format	ted in response (.rsp) files. Vendor respons	e files must match this format
Intermediate results	s files (.txt) : files with intermediate re	esults (.txt) are supplied to help with debug	ging.
See the README file i	n each zip file for details.		
	Publication	Algorithm Test Vectors	
	FIPS 186-4	DSA ECDSA RSA	



After downloading the zip file 186-4ecdsatestvectors.zip, unzip it and find the following vectors in the plaintext file KeyPair.rsp.

ECC P256 secp256r1 key pair for the OEM Root Key Pair

The following vector is used for the OEM Root Key Pair. It is used in section 2.2 to generate the wrapped OEM Root Public Key. It is also used in section 2.4 to generate the key certificate.

d = c9806898a0334916c860748880a541f093b579a9b1f32934d86c363c39800357

Qx = d0720dc691aa80096ba32fed1cb97c2b620690d06de0317b8618d5ce65eb728f

Qy = 9681b517b1cda17d0d83d335d9c4a8a9a9b0b1b3c7106d8f3c72bc5093dc275f

ECC P256 secp256r1 key pair for the OEM APP (BL) Key Pair

The following vector is used for the OEM APP (BL) Key Pair. It is used in section 2.4 to generate the code certificate.

d = 710735c8388f48c684a97bd66751cc5f5a122d6b9a96a2dbe73662f78217446d

Qx = f6836a8add91cb182d8d258dda6680690eb724a66dc3bb60d2322565c39e4ab9

Qy = 1f837aa32864870cb8e8d0ac2ff31f824e7beddc4bb7ad72c173ad974b289dc2

2.2 Generate the Root of Trust

As explained earlier, the hash of the OEM_ROOT_PK is the Root of Trust of the system and will be injected during a successful application programing when FSBL is enabled.

The OEM_ROOT_PK needs to be wrapped using the Renesas DLM server prior to injection to the MCU using RFP. Prior to wrapping the OEM Root Public Key, go through the process of Wrapping the User Factory Programming Key using the Renesas Key Wrap Service. The security considerations and the process of the UFPK wrapping is not repeated in this write up, reference the following sections in R11AN0496 to learn the usage background and establish the PGP encrypted communication with the Renesas DLM Server.

- Reference section Create PGP Key Pair to generate customer PGP Key Pair.
- Reference section Registration with DLM Server to register with the DLM Server.
- Reference section **Exchange User and Renesas PGP Public Keys** to establish encrypted communication with the DLM Server.

2.2.1 Generate the Wrapped User Factory Programming Key

After finishing the operations based on the above sections in R11AN0496, the next step is to reference section **Wrapping the UFPK** in R11AN0496 to generate W-UFPK. However, there are some critical steps to update during this process. Please read through the section **Wrapping the UFPK** first prior to reading the rest of this section to identify where to update the operations in order to generate the Wrapped UFPK for



OEM Root Public Key injection purpose. Afterwards, identify where to update the following operations in that flow and follow R11AN0496 to generate the W-UFPK.

- For a given input plaintext UPFK, the output of DLM server (W-UFPK) will vary based on the selected mode for the security engine. I.e.: Compatibility mode or Protected Mode. To be consistent with the option selected on the DLM Server when wrapping the OEM Root Key (which uses the MCU Protected Mode), choose the RA Family, RSIP-E51A Security Functions and Protected Mode option under the Overview page when using SKMT to generate the UFPK.
 - It is important to note that R11AN0496 uses RSIP Compatibility mode which implies selection of RA Family, RSIP-E51A Compatibility Mode in SKMT. Please pay attention to changing to the protected mode needed for FSBL usage.



Figure 17. Choose RSIP-E51A Security Functions and Protected Mode

• For the same reason, when using the DLM Sever to wrap the UFPK, it is critical to choose the following RA8 item under the **DLM and Protected Mode** rather than the Compatibility Mode entry.



Figure 18. Select RA8D1/RA8M1 MCU Group DLM and Protected Mode



• The other steps for generating the Wrapped UFPK are identical to what is described in the R11AN0496.

The rest of this application project assumes that the following UFPK and W-UFPK have already been created:

ra8x1_ufpk.key: the UFPK
ra8x1_ufpk.key enc.key: the DLM Wrapped W-UFPK

Once the UFPK and W-UFPK are generated, wrapping the OEM Root Public Key should be done in a similar way to the ECC Public Key wrapping process as described in the section **Wrap an Initial ECC Public Key with the UFPK** of R11AN0496.

2.2.2 Generate the Wrapped OEM Root Public Key using OpenSSL and the SKMT CLI Interface

Once the Secure Key Management Tool (SKMT) is installed, open a command line window and navigate to the \cli folder and use the following command to generate the Wrapped OEM Root Public Key. This key can be presented to the MCU using the secure key injection process using RFP.

UFPK: 000102030405060708090A0B0C0D0E0F000102030405060708090A0B0C0D0E0F

W-UFPK: 00000000A7BF7EB27054D78E07C504291520678AA7BF7EB27054D78E07C504291520678A

IV: 55AA55AA55AA55AA55AA55AA55AA55AA

Encrypted key: E71776A79F2BFF879CE3A434C5D0AEFBA934214518114AA89E7CAD10BD45D25623CE6710EC929971BAD200814 B6D633A670447B51347EA24EC7908C9C66AA933F7DD64E2DBDB1B831CED6E3B1347C69B

Note that this example <code>oem_root_pk_cli.rkey</code> does not match the example project included in this application project. So, do not use this key in the example boot processes described in this application project.

2.2.3 Generate the Wrapped OEM Root Public Key using the SKMT GUI Interface

In this section, the OEM Root Public Key pair provided in section 2.1.2 will be used to generate the wrapped OEM Root Public Key.

Launch SKMT, under the Overview page, choose RA Family, RSIP-E51A Security Functions and Protected Mode as shown Figure 17. Navigate to the Wrap Key tab in the SKMT, select the Key Type as OEM Root public and then provide the Wrapping Key (UFPK and W-UFPK).

Overview Generate	UFPK Generate	(UK Wrap K	TSIP UPDATE	FSBL D	OTF S	FP	
Keys n	nust be wrapped by	the UFPK fo	r secure injection o	by the KU	K for sec	ure updat	e.
Key Type Key Dat	a						
O DLM/AL	AL2_KEY \sim	⊖ AES	128 bits	\sim		24	
⊖кик		⊖ RSA	2048 bits, public	~		S	
OEM Root publ	lic	OECC	secp256r1, public	\sim			
		OHMAC	SHA256-HMAC	\sim			
Wrapping Key							
UFPK UFPK Fil	e: C:\RA8_FSB	L\ufpk\ra8x1	_ufpk.key				Browse.
W-UFPK	File : C:\RA8_FSB	L\ufpk\ra8x1	_ufpk.key_enc.key				Browse.

Figure 19. Wrap the OEM Root Public Key



Under the **Key Data** tab, provide the OEM Root Public Key.



Figure 20. Provide the OEM Root Public Key

Now select **RFP** as the output type, select the output location, name the file, and then click **Generate File** to generate the Wrapped OEM Root Public Key.

The View	Help			
Overview	Generate UFPK	K Generate KUK Wrap Key TSIP UPDATE F	SBL DOTF SFP	
	Keys must b	e wrapped by the UFPK for secure injection or	by the KUK for secure update.	
Кеу Туре	e Key Data			
○ File			В	rowse
Raw	Qx :	d0720dc691aa80096ba32fed1cb97c2b62069	0d06de0317b8618d5ce65eb728f	Û.
	Qy:	9681b517b1cda17d0d83d335d9c4a8a9a9b0	b1b3c7106d8f3c72bc5093dc275f	0
ORand	lom - Output Fil	e	В	rowse
Mana				
		C\R48_ESBL\ufpk\ra8x1_ufpk_key		TOWER
U	W-LIEPK File	C:\RA8 FSBL\ufpk\ra8x1 ufpk.kev enc.kev		rowse
ОКИК	KLIK File :			rowse
-				
OUse s Output Format : Address	rate random val pecified value (1 t RFP : 10000	I6 hex bytes, big endian format) 0011223344: File : C:\RA8_FSBL\K2\oem_ Key name :	root_key.rkey B	rowse
		Generate file		
Dutput File UFPK, 0001 W-UFPK: 00 V: 043CB6E Encrypted I 85861E82D1	2 C:\RA8_FSBL\k 02000105000700 0000002A8434C BD0A073FF5F38E key: D3997B72BA882 06007328288201	(2) oem_root_key.rkey 0000A0B0C0D0E0F00042030405060708090A0B0 CA97D0313279389DD8F15523DB2A8434CA97D03 80F87710671A3 1AA5B64947B40A375F7A77B9ACA071C94B2F93 D6727CFF95642BA6380371C177A48812D3ED15	C0D0E0F 813279389DD8F15523DB 803F5A4018DD4EA4556B3DEE7A1 1294831	FB26176

Figure 21. Generate the Wrapped OEM Root Public Key

This Wrapped OEM Root Public Key (oem_root_key.rkey) is provided to you to enable convenient evaluation of the system. It can be used if this same Root Public Key is used in the key and code certificate generation.



2.3 Prepare a Blinky Application with FSBL Enabled with HMAC-SHA256 Boot

Typically, to use FSBL enabled boot, the OEM_BL should be developed first with FSBL disabled. After the OEM_BL is fully tested, the FSBL can be enabled.

The included blinky example project <code>blinky_hmac_boot_ra8m1</code> is created by following section of "Create a New Project for Blinky" from the FSP User's Manual with no RTOS support for RA8M1. By default, setting up the Trust Zone boundary is enabled in the Debug configuration setting. The FSBL property is configured based on the configuration in . For the convenience of debugging the application, FSBL skip is enabled upon software reset or exit from Deep Software Standby mode. In addition, the project configures **P107** as **Output Initial Low** so it can be turned on to high by the FSBL upon a boot failure. Note that although the e2studio example project has the FSBL enabled, the FSBL will not be enabled after the application image is downloaded by e2studio. The FSBL will only be effective after the next power cycle.

For an MCU which has the FSBL already enabled in an early operation, run the **MCU Initialize** command to use the boot firmware to erase the existing FSBL and Trust Zone settings which resides in the option-setting memory. This can be achieved using the **Renesas Device Partition Manager** (RDPM) (which is natively installed with e2studio) or **Renesas Flash Programming** (RFP).

Once **e2studio** is launched, the RDPM can be activated by selecting **Run -> Renesas Debug Tools -> Renesas Device Partition Manager**. On EK-RA8M1, the default jumper setting has SCI boot mode enabled and the SCI signals are routed to the Debug interface, either SCI or SWD interface can be selected when working with RDPM. In the following screenshot, the SCI interface is selected.

Renesas Device Partition Manager		_	
Device Family: Renesas RA 🖂			
Action			
Read current device information	Change debug state		
Set TrustZone secure / non-secure boundaries	Initialize device back to factory default		
Target MCU connection: J-L	Link ~		
Connection Type: SC	а ~		
Emulator Connection: Ser	rial No 🗸 🗸		
Serial No/IP Address:			
Debugger supply voltage (V): 0	\sim		
Connection Speed (bps for SCI, Hz for SWD): 960	00 ~		
Debug state to change to: See	cure Software Development \sim		
Memory partition sizes			
Use Renesas Partition Data file			
			Browse
Code Flash Secure (KB)	32		
Code Flash NSC (KB)			
Data Flash Secure (KB)	0		
SRAM Secure (KB)	8		
SRAM NSC (KB)			
Command line tool:			
C:\Users\a5099044\.eclipse\com.renesas.platform	m_865760450\DebugComp\RA\DevicePartitionManager	RenesasDevicePartitionManagerCmd.exe	Browse
Display errors in : English			^
Connecting			
Loading library : SUCCESSFUL! Establishing connection : SUCCES	SSFUL!		
Checking the device's TrustZone type : SUC CONNECTED.	CCESSFUL!		
Initializing device and rolling back Protection Lev	vel to PL2		
SUCCESSFUL!			
Disconnecting			
Connection : SUCCESSFUL!			
END SUMMARY			
			~
<			>
0	Import	Export Run	Close
	import		

Figure 22. Using RDPM to Initialize the MCU



Figure 23 shows the command to choose to use RFP to Initialize Device.

Operation completed.

Figure 23. Using RFP to Initialize the MCU

After Initializing the Device, follow the below steps to build and run the included example project.

Import blinky_hmac_boot_ra8m1 to a workspace, open the configuration.xml file and click Generate Project Content. Connect J-Link OB USB on J10 to the development's USB connection using a Micro USB cable, build and run the included blinky project (blinky_hmac_boot_ra8m1) to verify its functionality.

- The compilation result will be used in the section 2.4 for the creation of the code certificate.
- The three LEDs should be blinking.

arm-none-	-eabi-size	eform	nat=berkel	ey "blinky_hmac_boot_ra8m1.elf"
text 11576	data 92	bss 2220	dec 13888	<pre>hex filename 3640 blinky_hmac_boot_ra8m1.elf</pre>
16:53:29	Build Fir	nished.	0 errors,	0 warnings. (took 396ms)



Open Tera Term application and configure the Baud Rate to 115200.

Tera Term: Serial port se	etup and connection		×
Port:	СОМ6 ~	New setting	ונ
Speed: Data:	115200 V	Cancel	
Parity:	none v		
Stop bits:	1 bit \sim	Help	
Flow control:	none ~		
Trans O	smit delay msec/char 0	msec/line	
Device Friendly Device Instance Device Manufac Provider Name: Driver Date: 6-6 Driver Version:	/ Name: JLink CDC UAR 2 ID: USB\VID_1366&PI cturer: SEGGER : SEGGER :-2019 1.34.0.44950	T Port (COM6) D_1024&MI_00\6&2B18	
<		>	

Figure 25. Configure the Tera Term

Click **New setting** and observe the following output on the terminal. Notice the output for the FSBL register settings, the boot measurement report and the HMAC digest. Refer to the register definition in the Hardware UM, the code certificate content (Figure 12) to understand the meaning of the output. Since the FSBL is not enabled yet, the version num oem bl field will be 0s and the digest area will be 0xFFs.





Figure 26. J-Link Console Output for HMAC Boot

When a Power-ON Reset is issued to the MCU, the FSBL will be activated and the blinky will not be booted anymore because the Root of Trust and code certificate are not yet programmed to the MCU. For a successful boot-up of the application, inject the OEM_ROOT_PK and present the key certificate and code certificate before a POR is issued. This process is explained in the subsequent sections. Section 2.6 provided details on booting an application with FSBL enabled.

2.4 Acquire the MCU OEM_BL Anti-Rollback Counter Value

As explained in section 1.3.3, the code certificate for HMAC boot should include a field for **Image Version** which ranges from 1 to 64. This Image Version number is permanently stored in a pair of option-setting memory registers called Anti-Rollback Counter for OEM_BL (refer to Figure 2) for the location of this register.

Base ad	dress: 0x2703 0000		
Offect ed	drees: 0x2700_0000	- 0. 1)	
Oliset au	JIESS. 0X076 + 0X004 × 11 (11	- 0, 1)	
Bit po	sition: 31		0
Bi	it field:	ARC_OEMBL[32 × n + 31 : 32 × n]	
Value after	reset:	User setting ^{*1}	
Bit	Symbol	Function	R/W
Bit 31:0	Symbol ARC_OEMBL[32*n	Function Anti-Rollback Counter for OEM_BL Application	R/W R/W

Figure 27. Anti-Rollback Counter for OEMBL

Note that the Image Version number is not the value stored in these two registers, but an interpreted value. Reference section **52.12.5 Anti-Rollback Counter** for the operational details of this counter. Only boot firmware can write to this counter during production programming. Essentially, every successful application update increments the counter by setting one addition bit to 1. As an example, if the device has been updated 3 times, a number 7 (which is b 0111) will be stored in these two counters. These two 32-bit counters can be used for 64 application updates.



Renesas RA Family

The application project includes a J-Link script that reads out this register value. Unzip read_arc_oembl_jlink_script.zip and double click on ra8m1.bat to read out the value in these two registers. Figure 28 shows an example output of running the J-Link script. Note that in this example, the register 0x27030878 (ARC_OEMBL0) holds a value of 0xFFFFFFFF and register 0x2703087C (ARC_OEMBL1) holds a value of 0x00000001. There are a total of 33 bits set to 1 for the ARC_OEMBL0 and ARC_OEMBL1 registers. Therefore, the next Image Version user can select should be equal or higher than 34 but equal or lower than 64.

SEGGER J-Link Commander V7.920 (Compiled Nov 8 2023 15:47:59) DLL version V7.920, compiled Nov 8 2023 15:46:12 J-Link Command File read successfully. Processing script file J-Link/device R7FA8M1AH J-Link/device R7FA8M1AH J-Link connection not established yet but required for command. Connecting to J-Link via USB0.K. Firmware: J-Link OB-RA4M2 compiled Oct 30 2023 12:13:20 Hardware version: V1.00 J-Link uptime (since boot): 0d 10h 07m 36s S/N: 1082859018 USB speed mode: Full speed (12 MBit/s) VTref=3.300V	
DLL version V7.926, compiled Nov 8 2023 15:46:12 J-Link Command File read successfully. J-Link>device R7FA8M1AH J-Link>device R7FA8M1AH J-Link connection not established yet but required for command. Connecting to J-Link Via USBO.K. Firmware: J-Link OB-RA4M2 compiled Oct 30 2023 12:13:20 Hardware version: V1.00 J-Link Uptime (since boot): 0d 10h 07m 36s S/N: 1082859018 USB speed mode: Full speed (12 MBit/s) VTref=3.300V	
J-Link Command File read successfully. Processing script file J-Link>device R7FA8M1AH J-Link connection not established yet but required for command. Connecting to J-Link via USBO.K. Firmware: J-Link OB-RA4M2 compiled Oct 30 2023 12:13:20 Hardware version: V1.00 J-Link uptime (since boot): 0d 10h 07m 36s S/N: 1082859018 USB speed mode: Full speed (12 MBit/s) VTrefe3.300V	
J-Link Command File Yead Successfully. Processing script file J-Link>device R7FA8M1AH J-Link connection not established yet but required for command. Connecting to J-Link Via USBO.K. Firmware: J-Link OB-RA4M2 compiled Oct 30 2023 12:13:20 Hardware version: V1.00 J-Link uptime (since boot): 0d 10h 07m 36s S/N: 1082859018 USB speed mode: Full speed (12 MBit/s) VTref=3:300V	
J-Link>device R7FA8M1AH J-Link>device R7FA8M1AH J-Link connection not established yet but required for command. Connecting to J-Link OB-RA4M2 compiled Oct 30 2023 12:13:20 Hardware version: V1.00 J-Link uptime (since boot): 0d 10h 07m 36s S/N: 1082859018 USB speed mode: Full speed (12 MBit/s) VTref=3:300V	
J-LINK connection not established yet but required for command. Connecting to J-Link Via USBO.K. Firmware: J-Link OB-RA4M2 compiled Oct 30 2023 12:13:20 Hardware version: V1.00 J-Link uptime (since boot): 0d 10h 07m 36s S/N: 1082859018 USB speed mode: Full speed (12 MBit/s) VTref=3.300V	
Firmware: J-Link OB-RA4M2 compiled Oct 30 2023 12:13:20 Hardware version: V1.00 J-Link uptime (since boot): 0d 10h 07m 36s S/N: 1082859018 USB speed mode: Full speed (12 MBit/s) VTref=3.300V	
Hardware version: V1.00 J-Link uptime (since boot): 0d 10h 07m 36s S/N: 1082859018 USB speed mode: Full speed (12 MBit/s) VTref=3:300V	
S/N: 1082859018 USB speed mode: Full speed (12 MBit/s) VTref=3.300V	
USB speed mode: Full speed (12 MBit/s) VTref=3.300V	
J-Link>speed 12000	
Selecting 12000 kHz as target interface speed	
Selecting SWD as current target interface.	
J-Link>Mem32 0x27030878 1 Target connection not established yet but required for command.	
Device "R7FA8M1AH" selected.	
Connecting to target via SWD ConfigTargetSettings() start	
Configuring FlashDLNoRWWThreshold=0x200 in order to make sure that option bytes programming is done via read-modi	ify-write
ConfigTargetSettings() end - Took 147us InitTarget() start	
Identifying target device	
SWD selected. Executing JTAG -> SWD switching sequence Initializing DAP	
DAP initialized successfully.	
Determining TrustZone configuration Secure Debug: Enabled (SSD)	
Determining currently configured transfer type by reading the AHB-AP CSW register.	
> Correct transfer type configured. Done. TnitTarget() end - Took 5.72ms	
Found SW-DP with ID 0x6BA02477	
DPIDR: 0x6BA02477 ConeSight SoC-400 or earlier	
Scanning AP map to find all available APs	
AP[2]: Stopped AP scan as end of AP map has been reached	
AP[1]: APB-AP (IDR: 0x54770002)	
Iterating through AP map to find AHB-AP to use	
AP[0]: CHE HOHN AP[0]: AHB-AP ROM base: 0xE00FE000	
CPUID register: 0x410FD232. Implementer code: 0x41 (ARM) Feature set: Mainline	
Cache: L1 I/D-cache present	
Found Cortex-M85 r0p2, Little endian. EPUnit: 8 code (RP) slots and 0 literal slots	
Security extension: implemented	
Secure debug: enabled	
ROMTD1[0] @ E00FE000	
[0][0]: E00FF000 CID B105100D PID 000BB4D4 ROM Table	
[1][0]: E000E000 CID B105900D PID 000BBD23 DEVARCH 47702A04 DEVTYPE 00 ???	
[1][1]: E0001000 CID B105900D PID 000BBD23 DEVARCH 47711A02 DEVTYPE 00 DWT	
[1][2]: E0000000 CID B105900D PID 000BBD23 DEVARCH 47701A03 DEVTYPE 00 FPB [1][3]: E0000000 CID B105900D PID 000BBD23 DEVARCH 47701A01 DEVTYPE 43 ITM	
[1][5]: E0041000 CID B105900D PID 002BBD23 DEVARCH 47754A13 DEVTYPE 13 ETM	
[1][7]: E0003000 CID B105900D PID 000BBD23 DEVARCH 4/700A06 DEVTYPE 16 ??? [1][7]: E0042000 CID B105900D PID 000BBD23 DEVARCH 47701A14 DEVTYPE 14 CSS600-CTI	
[0][1]: E0040000 CID B105900D PID 000BBD23 DEVARCH 00000000 DEVTYPE 11 TPIU	
I-Cache LI: 16 KB, 256 Sets, 32 Bytes/Line, 2-Way D-Cache LI: 16 KB, 128 Sets, 32 Bytes/Line, 4-Way	
Memory zones:	
Zone: "Default" Description: Default access mode Cortex-M85 identified.	
27030878 = FFFFFFF	
J-Link>Mem32 0x2703087C 1 2703087C = 00000001	
J-Link>rx 100	
Reset delay: 100 ms Reset ture MORMM : Resets core & reminterals via SYSPESETRES & VECTRESET bit	
Reset: ARMv8M core with Security Extension enabled detected.	
Reset: Halt core after reset via DEMCR.VC_CORERESET.	
Reset: Reset device via AIRCR.SYSRESETREQ. D-Link>g	
Memory map 'after startup completion point' is active	

Figure 28. Read the ARC_OEMBL Register using J-Link Script



2.5 Generate Key Certificate and Code Certificate

As explained earlier, for HMAC-SHA256 based boot option, two sets of public and private ECC-P256 secp256r1 key pairs are needed to generate the key and code certificate. In this section, two demonstrations are provided. The example keys should not be used for production support for security considerations.

- Using OpenSSL and SKMT command line interface
- Using NIST vectors and SKMT GUI interface

2.5.1 Using OpenSSL and SKMT Command Line Interface

To generate the key and code certificate, there are several properties to configure:

- Input: the load address of the application. In the following example, this is the command option /loadaddr.
- Input: the size of the OEM_BL. In the following example, this is the command option /oembl size.
- Input: the version of the application. In the following example, this is the command option /ver. Note that for an MCU that has previously booted from an old version of the application via FSBL, the next version needs to be a higher version. The version number will be included in the code certificate generated (refer to Figure 12). In this example, it is set to 3, which can be used if the ARM_OEMBLn value with 0, 1, or 2.
- Input: the code flash size of the device to be used. In the following example, this is the command option /cfsize.
- Input: the application binary. In the following example, this is the command option /oembl.
- Input: the OEM_ROOT_SK. In the following example, this is the command option /oemroot_private.
- Input: the OEM_BL_ROOT_SK. In the following example, this is the command option /oembl_private.
- Output: the key certificate and code certificate. In the following example, these are the command options for /output_codecert and /output_keycert.

Open a command window and navigate to the \SecurityKeyMangementTool\cli folder and provide the following command to generate the key and code certificate. The file locations should be adapted as desired.

C:\Renesas\SecurityKeyMangementTool\cli>skmt.exe /gencert /mode "signature" /loadaddr "02000000" /oembl_size "8000" /cfsize "2000000" /ver "3" /oembl "C:\RA8_FSBL\fsp_v510\blinky_hmac_boot_ra8m1\Debug\blinky_hmac_boot_ra8m1.srec" /oembl_private file="C:\RA8_FSBL\openssl_keys\oem_bl_private_key.pem" /oemroot_private file="C:\RA8_FSBL\openssl_keys\oem_root_private_key.pem" /output_codecert "C:\RA8_FSBL\openssl_keys\blinky_hmac_openssl_ccert.bin" /output_keycert "C:\RA8_FSBL\openssl_keys\blinky_hmac_openssl_kcert.bin"

```
Output File: C:\RA8_FSBL\openssl_keys\blinky_hmac_openssl_kcert.bin
```

Output File: C:\RA8_FSBL\openssl_keys\blinky_hmac_openssl_ccert.bin

2.5.2 Use NIST ECC Key Pair and SKMT GUI Interface

This section uses the two sets of NIST CAVP ECC secp25r1 Key Pairs provided in section 2.1.2 to demonstrate the certificate generation. Both the private and public key parts of the two key pairs should be provided to SKMT to generate the key and code certificate.

Launch SKMT GUI. On the **Overview** page, select **RA Family**, **RIP-E51A Security Functions and Protected Mode**.

Next select the .srec generated in section 2.1 and define the version of the application.



R Security Key Management Tool	_	
Overview Generate UFPK Generate KUK Wrap Ke	Y TSIP UPDATE FSBL DOTF SFP	
The First Stage Bootloader supports multiple u Bootloader, for authenticity and/or integ Please refer to device-specific documen	se cases for checking application code, such a rity prior to programming and prior to executi tation for complete descriptions of all use cas	s an OEM ion. es.
OEM Bootloader Image : 1ky_hmac_bo Programming Verification Method : Signature	ot_ra8m1\Debug blinky_hmac_boot_ra8m1.sre Image Version : 2]	Browse

Figure 29. Select the Application and Version Number

The **Image Version** definition defined in Figure 29 will be stored in the code certificate. As explained in section 1.3.3, the allowed version number is 1 to 64 and update image needs to have a higher version than the current programmed image. So, for the first time when the FSBL HMAC based boot is exercised on a new MCU, the Image Version can be set to 1.

Stay on the FSBL page, configure the OEM Root Keys.



Figure 30. Provide the OEM Root Keys

Next, provide **OEM Bootloader Keys.**

OEM Bootloader	Private Key	
◯ File		Browse
Raw	710735c8388f48c684a97bd66751cc5f5a122d6b9a96a2dbe73662f7	8217446d
○ Random - Out	put File	Browse
OEM Bootloader I	Public Key	
() File		Browse
Raw Qx : f68	336a8add91cb182d8d258dda6680690eb724a66dc3bb60d2322565c39e4ab9	
Ov : 169	337aa32864870cb8e8d0ac2ff31f824e7beddc4bb7ad72c173ad974b289dc2	~

Figure 31. Provide the OEM Bootloader Keys

Next, navigate to the **Certificates** page and define the name and location of the key and code certificate and then click **Generate File(s)**. The key certificate and code certificate will then be generated.



Code Flash Start Address (hex) :	02000000
Device Code Flash Size :	2 MB 🗸 🗸
OEM Bootloader Size : © Calculate automa	(If exact size option is not available, select the next lower size)
Key Certificate : 48_FSBL\K2\oem_roo	bot_key_and_certs blinky_hmac_boot_ra8m1_key_cert.bin Browse bt_key_and_certs blinky_hmac_boot_ra8m1_code_cert.bin Browse
	Generate File(s)
itput File: C:\RA8_FSBL\K2\oem_root_key itput File: C:\RA8_FSBL\K2\oem_root_key SERATION SUCCESSEU	/_and_certs_blinky_hmac_boot_ra8m1_key_cert.bin /_and_certs_blinky_hmac_boot_ra8m1_code_cert.bin

Figure 32. Generate the Key and Code Certificate

The SKMT can also internally output NIST vectors. This is achieved by selecting Random - Output File.

OEM Bo Program Certific OEN Fil Ra OEN Fil ® Ra	e First Stage Bootload Bootloader, for au Please refer to de otloader Image : mming Verification Me cates OEM Root Key I Bootloader Priva le andom - Output File I Bootloader Publi	er suppo thenticity is OEM C:\RA8	rts multiple u y and/or integ iffic documer ky_hmac_boo) Signature) CRC Bootloader Kr	use cases fo grity prior t ntation for ot_ra8m1\l Image Ver Image Ver	or checking to programm complete d Debug\blink rsion : 32 y_and_certs\	application ning and pri scriptions y_hmac_bo	code, suctor of all use of ot_ra8m1.	h as an cution. cases. .srec Bro	OEM Browse Swse	e
Dutput File Dutput File Dutput File Dutput File	:: C:\RA8_FSBL\K2\oe :: C:\RA8_FSBL\K2\oe :: C:\RA8_FSBL\K2\oe :: C:\RA8_FSBL\K2\oe	m_root_k m_root_k m_root_k m_root_k	Ger ey_and_certs' ey_and_certs' ey_and_certs' ey_and_certs'	nerate File \oembl_pr \oembl_pr \blinky_hn \blinky_hn	(s) ivate_private ivate_public nac_boot_ra nac_boot_ra	e.key .key 8m1_key_ce 8m1_code_c	ert.bin cert.bin			

Figure 33. Using SKMT Internally Stored NIST Test Vectors

The certificates generated from either Figure 32 or Figure 33 can be used for the rest of the operations described in this application project.



Note that SKMT v1.05 has a bug which prevents it from generating code certificate with version 64. The following error will be printed when version 64 is requested.

The First Stage Bootloader supports multiple use cases for checking application code, such as an OEM Bootloader, for authenticity and/or integrity prior to programming and prior to execution. Please refer to device-specific documentation for complete descriptions of all use cases.	
OEM Bootloader Image : Vky_hmac_boot_ra8m1\Debug\blinky_hmac_boot_ra8m1.srec Brown Programming Verification Method :	:е
Certificates OEM Root Keys OEM Bootloader Keys	
Code Flash Start Address (hex) : 02000000	
Device Code Flash Size : 2 MB 🗸	
(If exact size option is not available, select the next lower size	e)
OEM Bootloader Size :	
Calculate automatically	
C Enter manually (hex)	_11
Key Certificate : C:\RA8_FSBL\K2\oem_root_key_and_certs\blinky_hmac_boot_ra8m1_key_cer Browse	
Code Certificate : C:\RA8_FSBL\K2\oem_root_key_and_certs\blinky_crc_boot_ra8m1_code_cert. Browse	
Generate File(s)	

Figure 34. Bug with SKMT v1.05 for Code Certificate Generation with Version 64

2.6 Demonstrate the Authenticated Production Programming and HMAC Boot

Download rfp_ra8m1.zip and extract the content to a local folder. Launch **RFP** and open the included rfp_ra8m1.rpj project. In this example RFP project, the SWD interface is selected as the boot interface, so the USB Debug cable can be used to access the boot mode.

If FSBL has been enabled in an earlier application or TrustZone[®] boundary has been set up previously, the **Initialize Device** (refer to Figure 23) command should be run prior to proceed to the following sections. This is needed so the previous FSBL configurations and TrustZone configurations can be erased.

Next, the RFP to download the application to the MCU and provide the credentials to authenticate and boot the application. Through the flash option programming, some credentials will be injected to the MCU as explained in section 1.3.4. Ensure the following **Operation Settings** are configured to erase the previous application, download the application and program the Flash Options.



operation Operation Settings Block Settings F	lash Options Connect Settings Unique Code
Command	Erase Options
Erase	Erase Selected Blocks \sim
Program	Program & Verify Options
∠ Verify	Erase Before Program
Program Flash Options	Verify by reading the device $\qquad \lor$
Verify Flash Options	
Checksum	Checksum Type
	CRC-32 method V
Fill with 0xFF	
Code Area / User Boot Area	Error Settings
Data Area	Enable address check of program file

Figure 35. Configure the Operation Settings

Select the application file to program to the MCU.

File Target Device Help	
Project Information Current Project: rfp_ra8x1.rpj Microcontroller: B7FA8M1AHECBD	
Program and User Key Files	
Command - X	
Add File(s) Remove Selected File(s) File Name Type Address/Offset C.\RA8_FSBLVfsp_v510\blinky_hmac_boot_ra8m1\Debug\blinky_hmac_boot_ra8m1.srec HEX	

Figure 36. Select the Application Project

Set up the Flash Options to configure the OEM Root Public Key, Code Certificate and Key Certificate.



Operation Operation Settings Block Setting	s Flash Options Connect Settings Unique Code
Disable Initialize Command	No
Disable AL2 authentication	No
Disable AL1 authentication	No
Disable LCK_BOOT transition	No
 Configuration Data Lock Bit 	
Set Option	Do Nothing
Lock bits	HEX FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
 Anti-Rollback Settings 	
Set Option	Do Nothing
ARCLS	HEX FFFF
ARCCS	HEX FFFF
 OEM Root Public Key 	
Set Option	Set
OEM Root Public Key File 1	C:\RA8_FSBL\K2\oem_root_key.rkey
Disable Rewriting	INO
✓ Certificate	
Set Option	Set
Verification Method	Signature
Code Certificate	_certs\blinky_hmac_boot_ra8m1_code_cert.bin
Key Certificate	C:\RA8_FSBL\K2\oem_root_key_and_certs\blin

Figure 37. Configure the OEM Root Key and the Certificates

Now navigate to the **Operation** tab and then click the **Start** button. RFP will read the SACC0 register value from the SREC and program the Code Certificate at the indicated memory address. The FSBL will compare the version number of the code certificate, if the version number is higher, the authentication of the OEM_BL will be proceeded. If the authentication is successful, the OEM HMAC digest will be programmed to the area after the code certificate. On the next power cycle, the FSBL will authenticate the application using the stored digest and the FSBL calculated digest, if the comparison is successful, the new application will be booted. The three LEDs should now be blinking.

	1	
File Target Device Help		
Operation Operation Settings Block Settings Flash Options Connect Settings Unique Code	•	
Project Information		
Current Project: rfp_ra8x1.rpj		
Microcontroller: R7FA8M1AHECBD		
Program and User Key Files		
C:\RA8_FSBLVsp_v510\blinky_hmac_boot_ra8m1\Debug\blinky_hmac_boot_ra8m1.srec		
CRC-32: 918431B3 Add/R	emove Files	
Command		
Erase >> Program >> Verify >> Program Flash Options >> Verify Flash Options		
	011	
Start	ок	
Config Area 11 0v0300A100 - 0v0300A11F size : 32		
[Config Area 1] 0x0300A130 - 0x0300A13F size : 16 [Config Area 2] 0x0300A200 - 0x0300A2CF size : 208		
[Config Area 4] 0x27030080 - 0x2703035F size : 736		
Verifying data [Config Area 1] 0x0300A100 - 0x0300A11F size : 32		
Config Area 1] 0x0300A100 - 0x0300A10F size : 10 [Config Area 2] 0x0300A200 - 0x0300A2CF size : 208 [Config Area 2] 0x0300A200 - 0x0300A2CF size : 208		
Setting the target device		
Disconnecting the tool		
	~	
Clear	status and message	

Figure 38. Successful Update of the Application based on HMAC SHA2-256 Verification



Upon successful boot, the J-Link console will output similar information as the following. The version_num_oem_bl and the image digest will vary based on the kit status and the application programmed.



Figure 39. J-Link Console Output for HMAC Boot

To demonstrate a failure on the HMAC boot is easy. First initialize the Device as show in Figure 23 and then perform the steps in section 2.6 except provide a wrong application image, for example the binary image of the CRC boot code or an updated the HMAC boot code. In either case, the RFP programming operation in Figure 38 will fail and pin P107 will assume a high level, thus turns on the red led.

3. Production Programming with CRC Check and CRC Boot Demonstration

When using CRC Boot, CRC32 integrity check will be performed during programming and normal execution after MCU reset.

3.1 Prepare a Blinky Example Project using FSBL with CRC Boot

The included blinky example project blinky_crc_boot_ra8m1 is created by updating the FSBL Execution Mode to **CRC boot and report measurement** as shown in Figure 40. The same error report pin is used (P107). Additionally, the J-Link Console message is updated to indicate the CRC boot mode.

Import blinky_crc_boot_ra8m1 to a workspace, open the configuration.xml file and click Generate Project Content. Build and run the included blinky project (blinky_crc_boot_ra8m1) to verify its functionality.

- The compilation result will be used in the section 3.2 for the creation of the code certificate.
- The three LEDs should be blinking.

V First Stage Bootloader (FSBL)	
 FSBL Control 0 (FSBLCTRL0) 	
FSBLEN	Enabled
FSBLSKIPSW	Enabled
FSBLSKIPDS	Enabled
FSBLCLK	240 MHz
 FSBL Control 1 (FSBLCTRL1) 	
FSBLEXMDFSBLEN	CRC boot with report measurement
 FSBL Control 2 (FSBLCTRL2) 	
PORTPN	PORTn07
PORTGN	PORT1m
 Code Certificates (SACCn) 	
SACC0	0x2006000
SACC1	0x2000000
FSBL Measurement Report Address (SAMR)	0x22001000

Figure 40. Configure FSBL for CRC Boot



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Configure the Tera Term as in Figure 25 and observe the following Tera Term output. Note that since the code certificate is not programmed yet, the output for the CRC is all 0xFFs. In addition, since the Image Version information is not used in a CRC boot, <code>version_num_oem_bl</code> output is all 0s.

The Red, Blue and Green LEDs should be blinking.
The current setting of the FSBL registers:
FSBLCTRLØ : fffffe00 FSBLCTRL1 : ffffffa FSBLCTRL2 : ffffffa SACC0 : 02006000 SACC1 : 02000000 SAMR : 22001000 HOEMRTPK : fffffff CFGDLOCK.CFGD0.CFGD_H : fffffff CFGDLOCK.CFGD0.CFGD.H : fffffff
CFGDLOCK.CFGD1.CFGD_H : ffffffff CFGDLOCK.CFGD1.CFGD_H : fffffff CFGDLOCK.CFGD2 : 0000ffff The current output of the boot measurement report:
p_report->sha256_oem_bl_fsblctrl1[0:15]: 00,00,00,00,00,00,00,00,00,00,00,00,00,
p_report->version_num_oem_bl: 0000 The CRC value of the application image: ffffffff

Figure 41. RTT Viewer Output for CRC Boot

3.2 Create the Code Certificate

The Code Certificate for CRC boot must contain the expected CRC of the OEM application. Upon MCU reset, if an integrity check is being performed, the FSBL will calculate the CRC of the application and compare it to the value in the stored Code Certificate.

Create the Code Certificate for CRC Boot using SKMT CLI

Open a command line and navigate to the SKMT \cli folder and use the following command to generate the code certificate based on the project created in section 3.1.

C:\Renesas\SecurityKeyMangementTool\cli>skmt.exe /gencert /mode "CRC" /loadaddr "02000000" /oembl_size "8000" /cfsize "200000" /oembl "C:\RA8_FSBL\fsp_v510\blinky_crc_boot_ra8m1\Debug\blinky_crc_boot_ra8m1.srec" /output_codecert "C:\RA8_FSBL\K2\certificates\blinky_crc_boot_ra8m1_code_cert.bin"

Output File: C:\RA8_FSBL\K2\certificates\blinky_crc_boot_ra8m1_code_cert.bin

Create the Code Certificate for CRC Boot using SKMT GUI



Overview Generate UFPK Gene	rate KUK Wrap Key TSIP UPDATE FSBL DOTF SFP	
The First Stage Bootloader Bootloader, for auth Please refer to device	supports multiple use cases for checking application code, suc inticity and/or integrity prior to programming and prior to exec e-specific documentation for complete descriptions of all use	h as an OEM cution. cases.
OEM Bootloader Image : Programming Verification Meth	0\blinky_crc_boot_ra8m1\Debug\blinky_crc_boot_ra8m1 od: ○ Signature Image Version : 4 ● CRC	srec Browse
Certificates OEM Root Keys	OEM Bootloader Keys	
Code Flash Start Address (hex	: 02000000	
Device Code Flash Size :	2 MB 🗸 🗸	
	(If exact size option is not available, select the	next lower size)
OEM Bootloader Size :		
Calculate	automatically	
O Enter ma	nually (hex)	
Key Certificate : C:\RA8_FS	SL\K2\certificates\blinky_hmac_boot_ra8m1_key_cert.bin	Browse
Code Certificate : C:\RA8_FS	BL\K2\certificates\blinky_crc_boot_ra8m1_code_cert.bin	Browse
	Generate File(s)	

Figure 42. Create CRC Boot Code Certificate

When code certificate is generated with CRC specified, the CRC value is output as a dummy value for the Signer ID field in the code certificate. When the measurement report for CEC verification is created, the Signer ID uses 8 times of the duplicated CRC value. CRC32 is 4byte (32 bits) and Signer ID (SHA256) is 32 bytes, the CRC value is written 8 times in Signer ID field.

3.3 Demonstrate the CRC Boot of the Application using RFP

Launch **RFP** and open the included rfp_ra8m1.rpj. We will download the application to the MCU and provide the credentials to authenticate and boot the application through the MCU's SWD boot interface.

Ensure the following **Operation Settings** are configured.

Operation Operation	Settings Block Settings	Rash Options Connect Settings Unique Cod Erase Options	e
Erase Program Verify Program Rat Verify Rash Checksum	sh Options Options	Erase Selected Blocks Program & Verify Options Erase Before Program Verify by reading the device	~
Fill with 0xFF	User Boot Area	CRC-32 method	~
Data Area		Enable address check of pr	ogram file

Figure 43. Configure the Operation Settings before Downloading the Application

Select the application file to program to the MCU.



		0			
Operation Operation Setti	ngs Block Settings Flash Optio	ons Connect Settings U	nique Code		
Project Information					
Current Project:	rfp_ra8x1.rpj				
Microcontroller:	R7FA8M1AHECBD				
Program and User Key	/ Files				
			Add/Remove File	S	
🗾 Eile Deteile				_	
File Details					
		Ad	d File(s)	Remove Selecte	ed File(s)
File Name				Type Address	/Offset
C:\RA8 FSBL\fsp v510)\blinky crc boot ra8m1\Debug\t	olinky crc boot ra8m1.sre	c H	IEX	
			0	С	ancel
Disconnecting the tool Operation completed.				С	ancel
Disconnecting the tool Operation completed. Loading Project (C¥Users	¥MyPC¥Documents¥Renesas F	lash Programmer¥∨3.13¥	rfp_ra8x 1¥rfp_ra8x 1	р)	ancel

Figure 44. Select the Application Project

Click **OK** and navigate to the **Flash Options** page to configure the **Code Certificate**.

Fi	le Ta	arget Device He	p				
Ор	eration	Operation Settings	Block Settings	Flash Options	Connect Settings	Unique Code	
	Set Op	otion		Do	Nothing		^
	Disabl	e Initialize Command		No			
	Disabl	e AL2 authentication		No			
	Disabl	e AL1 authentication		No			
	Disabl	e LCK_BOOT transiti	on	No			
~	Confi	guration Data Loc	sk Bit				
	Set Op	otion		Do	Nothing		
	Lock b	bits		HEX	FFFFFFFFFFFFF	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	
~	Anti-	Rollback Settings					
	Set Op	otion		Do	Nothing		
	ARCL	S		HEX	FFFF		
	ARCC	S		HEX	FFFF		
~	OEM	Root Public Key					
	Set Op	otion		Do	Nothing		
	OEM I	Root Public Key File	1				
	Disabl	e Rewriting		No			
~	Certif	icate					_
	Set Op	otion		Se	t		_
	Verific	ation Method		CR	С		
	Code	Certificate		tifi	cates\blinky crc	boot ra8m1 code cert.	bin 🗸 🗸

Figure 45. Configure the CRC Code Certificate



Next, navigate to the **Operation** tab and select **Start**, the application will be programming as well as the code certificate. The three LEDs should now be blinking.

Operation Departion Settings Block Settings Rash Options Connect Settings	3 Unique Code
Project Information Current Project: rfp_ra8x1.rpj Microcontroller: R7FA8M1AHECBD	
Program and User Key Files	
C:\RA8_FSBL\K2\K2\blinky_crc_boot_ra8m1\Debug\blinky_crc_boot_ra8	m1.srec
CRC-32: 69EDD7F7	Add/Remove Files
Config. Area 11 0-02000.000 - 0-02000.0115 - size - 20	
Config Area 11 0×02004100 = 0×02004115	
[Config Area 1] 0x0300A130 - 0x0300A13F size : 16 [Config Area 2] 0x0300A200 - 0x0300A2CF size : 208 [Config Area 4] 0x27030080 - 0x2703035F size : 736	
Verrying data [Config Area 1] 0x0300A100 - 0x0300A11F size : 32 [Config Area 1] 0x0300A100 - 0x0300A13F size : 16 [Config Area 2] 0x0300A200 - 0x0300A2CF size : 208 [Config Area 4] 0x27030080 - 0x2703035F size : 736 Setting the target device	
Disconnecting the tool Operation completed.	v
r	

Figure 46. Downloading the CRC Boot Application

On the J-Link console, a similar message as the following will be printed. Note that the CRC value is repeated four times as the <code>signer_id</code>.

ine Reu, blue and Gr	een LEDS SHould De Diinki	ng .	
The current setting	of the FSBL registers:		
FSBLCTRLØ	: fffffe00		
FSBLCT RL1	: fffffffd		
FSBLCTRL2	: fffffffa		
5HCC0 90001	- 02000000		
SAMR	: 22001000		
HOEMRTPK	: 2e22a5a8		
CFGDLOCK.CFGDØ.CFGD_	H : ffffffff		
CFGDLOCK.CFGDØ.CFGD_	H = ffffffff		
CFGDLOCK.CFGD1.CFGD CFCDLOCK.CFGD1.CFGD	H : tttttttt		
CFGDLOCK_CFGD1.CFGD_	<u>n - IIIIIII</u> : 0000ffff		
or approved of app			
The current output a	f the boot measurement re	port:	
n renort->sha256 oem	h] fshlctpl1[0:15]:		
8e.51.51.70.d8.fb.c8	4e.58.c8.8b.86.d3.11.fc.	f4.	
n renort-)sha256 oer	hl fshlctrl1[16:31]:		
ab,93,43,be,cf,b7,ae	,38,f7,a8,c5,a6,79,dd,d0,	37,	
p_report->signer_idl	0:15J:	-1	
54, Da, fC, e1, 54, Da, fC	,e1,54,Da,fC,e1,54,Da,fC, 16-211-	e1,	
54.ba.fc.e1.54.ba.fc	.e1.54.ba.fc.e1.54.ba.fc.	e1.	
p_report=/version_nu			
0000 ⁻			
The CRC value of the	application image:		

Figure 47. CRC Boot is Successful



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Note that the CRC32 calculated from RFP differs from the CRC32 calculated from SKMT. The RFP calculates the CRC32 of the entire file. For example, for a .srec file, all the record fields are included in the CRC32 calculation. However, for SKMT, the CRC32 calculation only includes the binary value of the OEM_BL.

To demonstrate a failure on the CRC boot is easy, first initialize the Device as show in Figure 23 and then perform the steps in section 3.3 except provide a wrong binary image, for example provide the binary image of the HMAC boot code or perform a minor update the CRC boot code. In either case, the RFP programming operation in Figure 46 will fail and P107 assume a high level which will turn on the red LED.

4. Appendix

4.1 Usage Note with TrustZone[®] Project

Assume the set of Trustzone projects is the following:

- blinky s for the secure application
- blinky ns for the matching non-secure application

When using FSBL with a set of TrustZone projects with HMAC boot, generating the ECC Key Pairs and OEM Root Key can be achieved in the same ways as described in sections 2.1 and 2.2. The same script described in section 2.4 can also be used to retrieve the ARC_OEMBL register values.

The operations in section 2.3, 2.5, and 2.6 should be adjusted to use FSBL with a set of TrustZone projects. The .rdp file generated from the IDE includes the TrustZone boundary based on the secure project flash and SRAM usage side and will be used for the setting up the TrustZone boundary.

• In section 2.3, the FSBL should be enabled in blinky_s project. Ensure SACCx is located outside the flash area used by blinky_s and blinky_ns. When using e2studio IDE, if the following selection is enabled, the IDE will pick up the generated blinky_s.rdp file to program the TrustZone boundary.



Main 🕸 Debugger 🕨 Startup 🔲 Common 🧤	Source
Debug hardware: J-Link ARM 🛛 🗸 Target Device:	R7FA8M1AH
GDB Settings Connection Settings Debug Tool Sett	ings
✓ J-Link	
Type	USB
J-Link Serial	(Auto)
Settings File	\${workspace_loc:/\${ProjName}}/\${LaunchConfigName}.jlink
Script File	
Log File	\${workspace_loc:/\${ProjName}}/JLinkLog.log
Low Power Handling	No
✓ IP Connection	
Connection Method	IP via LAN
Host Name/IP Address[:port number]	
Identifier	
Tunnel Server	
Port Number	
Password	
✓ Interface	
Туре	SWD
Speed (kHz)	4000
✓ JTAG Scan Chain	
Multiple Devices	No
IRPre	0
DRPre	0
Connection	
Register initialization	No
Reset at the beginning of connection	Yes
Reset at the end of connection	No
Reset before download	Yes
Reset after download	Yes
ID Code (Bytes)	FFFFFFFFFFFFFFFFFFFFFFFF
Hold reset during connect	Yes
Set CPSR(5bit) after download	No
Prevent Releasing the Reset of the CM3 Core	Yes
Secure Vector Address	
Non-secure Vector Address	
Hot Plug	No
Disconnection Mode	Stop
~ SWV	
Core clock (MHz)	0
✓ Trust7one	
Set TrustZone secure/non-secure houndaries	Yes
Authenticate device to Authentication Level (Al	None
- Addrendedte device to Addrendedton Level (AL	

Figure 48. Enabled Programming of TrustZone[®] Boundary in e² studio

When using Keil and IAR for TrustZone based application development, the RDPM should be manually launched. The RDPM should be configured to use the generated .rdp file to program the TrustZone boundary as shown in Figure 49.



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Action				
Read current device inform	ation	Change	debug state	
Set TrustZone secure / non	secure bound	aries 🗌 Initialize	device back to fa	ctory default
Target MCU connection:		J-Link	~	
Connection Type:		SCI	~	
Emulator Connection:		Serial No	~	
Serial No/IP Address:				
Debugger supply voltage (V):		0	\sim	
Connection Speed (bps for SCI	, Hz for SWD):	9600	\sim	
Debug state to change to:		Secure Software	Development	\sim
Memory partition sizes			1	
Use Renesas Partition Data	file			
C:\RA8_FSBL\K2\blinky_s\De	bug\blinky_s.r	pd		Browse
Code Flash Secure (KB)	32			
Code Flash NSC (KB)	0			
Data Flash Secure (KB)	0			
SRAW SECURE (KB)	0			
SKAIVI INSC (KB)	U			
Command line tool:				
	m.renesas.plat	form_865760450\	DebugComp\RA\[DevicePar Browse.
C:\Users\abusu44\.eclipse\co.				
Connecting Loading library Establishing connection Checking the device's Trus CONNECTED.	: SUCCESSFU : SUC tZone type :	L! :CESSFUL! SUCCESSFUL!		,
Connecting Loading library Establishing connection Checking the device's Trus CONNECTED. Programming secure/non-secu- - Code Flash Secure (kt SUCCESSFUL!	: SUCCESSFU : SUC tZone type : ure memory p. 3) : 32 3) : 0	L! CESSFUL! SUCCESSFUL! artitions with the	following settings	
Connecting Loading library Establishing connection Checking the device's Trus CONNECTED. Programming secure/non-secu- - Code Flash Secure (kf - Data Flash Secure (kf SUCCESSFUL! Disconnecting DISCONNECTED. SUMMARY OF RESUL Connection : SUCCESSFUL!	: SUCCESSFU : SUC tZone type : ure memory p: 3) : 32 3) : 0	L! CESSFUL! SUCCESSFUL! artitions with the	following settings	
Connecting Loading library Establishing connection Checking the device's Trus CONNECTED. Programming secure/non-sec - Code Flash Secure (kf - Data Flash Secure (kf SUCCESSFUL! Disconnecting DISCONNECTED. SUMMARY OF RESUL Connection : SUCCESSFUL! Partition setting : SUCCESSFUL!	: SUCCESSFU : SUC tZone type : ure memory p 3) : 32 3) : 0 	L! CESSFUL! SUCCESSFUL! artitions with the	following settings	

Figure 49. Using RDPM to Set Up the TrustZone[®] Boundary



- In section 2.5, the compiled binary from blinky_s should be used to generate the key and code certificates. The non-secure application is not used in the certificate generation.
- In section 2.6, the secure application and the non-secure application should be programmed. In addition, the TrustZone[®] boundary should be set up using the blinky_s.rdp file generated from the secure project. So, in addition to provide the applications similarly as in Figure 36, users should set up the TrustZone boundary by selecting the blinky_s.rdp file under the RFP **Flash Options** page as shown in Figure 50 in addition to all other settings needed as originally documented in section 2.6.

Fi	le Ta	arget Device He	p					
Ор	eration	Operation Settings	Block Settings	Flash Options	Connect Settings	Unique Code		
~	DLM I	Keys						^
	Set Opt	otion		Do	Nothing			
	AL2 Ke	ey File						_
	AL1 Ke	ey File						
	RMA K	Key File						
~	Bound	dary						
	Set Op	otion		Se				
	Use Re	enesas Partition Data	a File	Ye	5			
	Renesa	as Partition Data File		RAF	_FSBL\K2\K2\b	olinky_s\Debu	ıg \blinky_s.rpd	

Figure 50. Set up the TrustZone[®] Boundary using RFP

When using FSBL with a set of TrustZone projects with CRC boot, uses need to adjust the operations in section 3.1, 3.2 and 3.3 in similar ways as the HMAC boot except only the code certificate will be generated.

For general usage of TrustZone projects, users can refer to application projects RA8 MCU Quick Design Guide R01AN7087 and Security Design using TrustZone R11AN01467.

4.2 Debug RFP Usage Errors

Users should refer to RFP User's Manual to understand the error code output from the RFP operation. Document information is provided in the References section. For your reference, the following error code indicates the Image Version number is not set up properly.



Figure 51. Image Version Number Error

5. References

- 1. Renesas RA Family Secure Key Injection Application Project (R11AN0496)
- 2. Renesas RA Family User's Manual: Hardware (R01UH0994)
- 3. Renesas Secure Key Management Tool User's Manual (R20UT5349)
- 4. Renesas Flash Programmer Flash memory programming software User's Manual (R20UT5352).
- 5. Renesas RA Security Design using TrustZone with IP Protection (R11AN0467)
- 6. Renesas RA8 MCU Quick Design Guide (R01AN7087)



6. Website and Support

Visit the following URLs to learn about the RA family of microcontrollers, download tools and documentation, and get support.

EK-RA6M4 Resources RA Product Information Flexible Software Package (FSP) RA Product Support Forum Renesas Support renesas.com/ra/ek-ra8m1 renesas.com/ra renesas.com/ra/fsp renesas.com/ra/forum renesas.com/support



Revision History

		Description	
Rev.	Date	Page	Summary
1.00	Mar.04.24		Initial release



General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

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