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Implementing Tip and Ring Protection Circuitry for the HC5518X Ringing SLIC Family

Introduction

A very important segment of the design of telecommunications equipment is proving adequate surge protection circuitry for the equipment terminals. System designers are required to protect the system from secondary (let through) disturbances as identified in GR-1089 - CORE, Issue 2, Section 4. Developing the protection circuitry solution while maintaining overall system performance and cost can often be challenging. This application note describes circuitry which could be used to meet the GR-1089, Section 4 requirements for the HC5518X family of ringing SLICs.

Basic Protection Circuit Description

Figure 1 illustrates a basic concept for primary and secondary protection of telecommunications equipment terminals where ringing SLICs are used. Although the following discussions focus primarily on second level surge protection, it is interesting to briefly discuss primary protection and “let through” surges as defined by GR-1089. Primary surge protection usually consists of a 3 mil carbon block or gas tube (GDT). These are voltage and current limiting devices that will “let through” surges of up to 2.5kV peak surge (lightning) and 600V_{RMS} (60Hz) power line cross. Let through surge currents can range from 500A peak (2µs x 10µs) lightning to 1A (600V_{RMS}) power cross. Consult GR-1089 for additional details concerning let through surges for secondary protection.

The secondary protection must protect the T and R ports from the “let through” voltages and currents. Although secondary protection schemes are application dependent, Figure 1 shows a typical implementation for a single stage ringing SLIC where through SLIC ringing is used. The circuit usually consists of fuses, PTCs (poly switch), RFI capacitors, diode bridges, and TVS devices such as the Intersil SGT27S10. This combination of protection circuitry must clamp the T and R ports to ground when a fault condition is present that exceeds the maximum output capabilities of the ringing SLIC. When the fault condition disappears, normal operation must resume.

The “resettable” PTCs are current limiting devices which increase in resistance when an applied fault condition exceeds the specified trip limits of the PTC. When the PTC is “tripped,” it remains in a high impedance state until the fault is removed. Capacitors C_1 and C_2 provide a low impedance path to ground for RFI transients. The diode bridge is used to clamp positive surges to ground and steer negative transients to the TVS which turns “on” and clamps the T and R terminals to ground. With the appropriate selection of these protection components, secondary protection requirements specified by GR-1089 can be met while maintaining overall system performance.

Suggested Protection Circuitry for HC5518x

Utilizing operational specifications provided by the HC5518X data sheet and the GR-1089 requirements, the circuit illustrated in Figure 2 can be implemented to protect the SLIC from secondary surge levels.

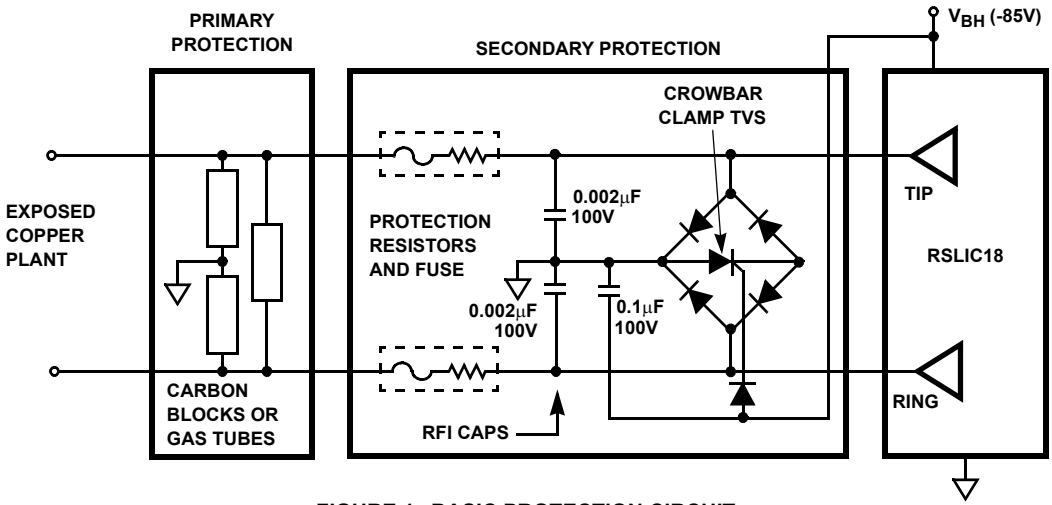


FIGURE 1. BASIC PROTECTION CIRCUIT

The circuit in Figure 2 is recommended for applications where the high battery voltage (V_{BH}) can range up to -85V.

To understand the selection of the protection devices an examination of the requirements placed upon the HC5518X, the TVS and the PTC should be reviewed.

HC5518X Protection Requirements During Fault Conditions

1. HC5518X's Trip and Ring ports must survive $100V_{PEAK}$ "residual" surges above ground or below VBH for 1µs during 2/10 lightning tests. This represents the typical "let through" lightning surge from the protection circuitry that the SLIC will encounter.
2. HC5518X's Tip and Ring ports must survive $3V_{PEAK}$ "residual" surges above ground or below VBH during AC power cross tests. This represents the typical "let through" AC power cross surge from the protection circuitry that the SLIC will encounter.
3. HC5518X must survive Tip and/or Ring faults to ground.

HC5518X Operational Conditions

1. Loop Current = 15mA to 45mA
2. Maximum ringing voltage = $83.4V_{PEAK}$ ($59V_{RMS}$)
3. Maximum On Hook Ringing Current = $42mA_{RMS}$ (5REN). PTC must not open.
4. Maximum Off Hook Ringing Current = $254mA_{RMS}$ (5REN + R_{LOOP}). PTC must not open before ring trip.
5. V_{BH} = -85V, V_{BL} = -24V, RP = 35Ωs/leg.

Using the conditions above, the selection of the protection resistance (RP), the TVS, and the PTC can be determined.

Protection Resistance Configuration

The HC5518X data sheet specifies 35Ω per leg for protection resistance. As shown in Figure 2, RP has been divided into 3 separate resistors and equals 35Ω. The total resistance of the PTC and R_{PT} on R_{PR} should equal 15Ω. The PTC represents 5Ω of RP (total) and limits the fault current to the TVS/diode bridge and the HC5518X. Additionally 10Ω,1W resistors are placed between the diode bridge and the PTC. These resistors provide additional current limiting to the diode bridge/TVS and the HC5518X. Finally, 20Ω, 1/2W resistors are placed between the diode bridge and the HC5518X to provide the final current limiting function to the SLIC. This arrangement provides the necessary current limiting to the system, selection of lower wattage resistors, and minimizes affects on circuit performance.

TVS Selection

TVS devices are solid state SCR type structures that are available in fixed or gate controlled breakover voltages (VBO). **The gate controlled version is best suited for the ringing SLIC application since its gate can be tied to the battery voltage enabling the TVS to track variations in the battery supply**. A "stopper" diode is placed in series with the gate of the TVS to prevent the VBH power supply from being shorted to ground whenever a fault condition energizes the SCR protection device. Additionally, in multi-line systems where power supplies are very robust, the "stopper" diode serves to protect the SCR and prevent disruption of service on the other lines. The Intersil SGT27S10 gated TVS was selected using the following criteria.

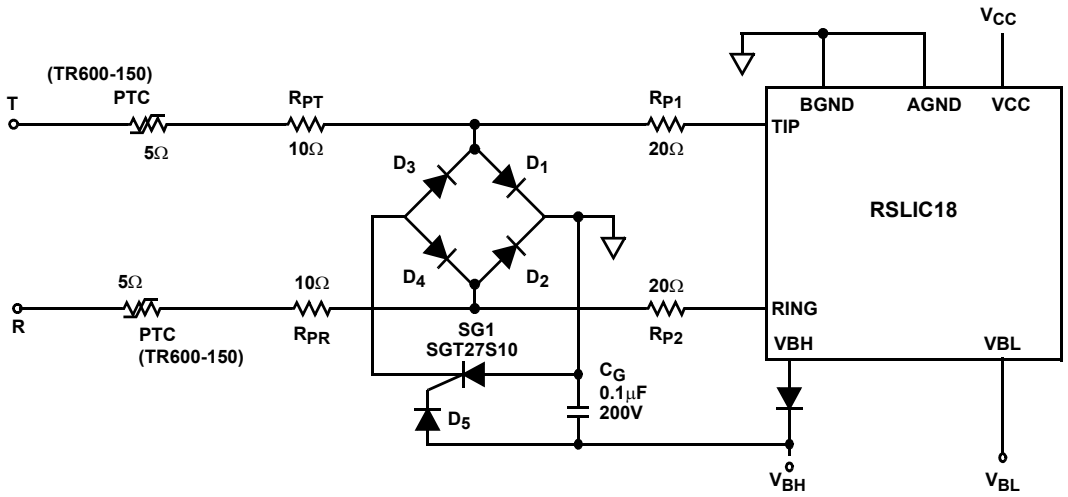


FIGURE 2. RSLIC18 PROTECTION CIRCUIT FOR V_{BH} = -85V APPLICATION

Selection of TVS for Lightning and Power Line Cross

10/1000 waveform = 1000V, 40A (GR-1089)

2/10 waveform = 2500V, 125A (GR-1089)

Peak line voltage to ground (40A peak current) = 25V (measured)

Peak line to TVS gate voltage (40A peak current) = -15V (measured)

Maximum Line to ground voltage = -90V (GR-1089)

Maximum Gate to line voltage = -90V (GR-1089)

Maximum gate current (10ms) = 1A (GR-1089)

Gate Trigger Current (Igt) = 150mA

Holding Current = 100mA

PTC (Positive Temperature Coefficient Thermistor) Selection

For the HC5518X protection circuitry the TR600-150 was selected. As a general rule of thumb, the PTC should have the lowest off state resistance possible. This allows for ease of matching to minimize affects on system performance. Additionally the TR600-150 resistance is specified as 6Ω which comprises part of the total protection resistance for the HC5518X.

PTC Specifications

PTC Resistance = 5Ω to 12Ω at 20^{o}C

1 Hour Post Trip Resistance = 20Ω at = 20^{o}C

PTC Holding Current = 83mA at 70^{o}C

55 Second Time To Trip at 20^{o}C = 350mA

55 Second Time To Trip at 70^{o}C = 193mA

Maximum Operating Voltage = 60V

Maximum Interrupt Voltage = 600V

Maximum Interrupt Current = 3A

With the selected components as shown in Figure 2, the protection circuitry can be prototyped and tested to GR-1089 requirements. It should be understood that HC5518X protection circuit is not limited to the recommended selections but any alternative selection would require retesting to GR-1089.

HC5518X Protection Circuit Surge Testing Procedure

The HC5518 protection circuit as shown in Figure 2 was tested to GR-1089 requirements. The HC5518 was exposed to each fault condition in all of its operating modes. Table 1 shows the operating modes for the HC5518X device. Using the circuit shown in Figure 2, the appropriate test signal generator and sequencing control is applied to the T and R ports at the PTCs. For lightning surge tests, Table 2 identifies the tests to be performed and the procedure. For AC power cross tests, Table 3 gives the tests to be performed and the procedure.

TABLE 1. RSLIC OP MODE CONTROL

OP MODE	F2	F1	F0	E0	BSEL
Forward Active	L	L	H	H	H/L
Reverse Active	L	H	H	H	H/L
Low Power Standby	L	L	L	H	H/L
Ringing	H	L	L	H	H/L
Tip Open	H	H	L	H	H/L
Forward Loop Back	H	L	H	H	H/L
Power Denial	H	H	H	H	H/L

Three HC5518Xs were tested to all of the fault conditions listed in Tables 2 and 3. Pre and post data was recorded for each of the surge tests. The governing criteria for pass or fail is given in the last Item of each of the test procedures.

Checking Ringing Capability

Once the protection circuitry has been selected and tested, the ringing capability of the SLIC should be evaluated for possible limitations. The HC5518X ringing capability was tested under conditions illustrated in Figure 3. The input ringing signal (sinewave) applied to the VRS pin was adjusted for maximum peak voltage swing on Tip and Ring while applying 1, 3, and 5 REN loads. The results of the evaluation are shown in Table 4.

Surge Test Results and Conclusion

Three HC5518X devices passed all of the fault conditions applied as recommended by GR-1089. After each fault condition was removed, the devices under test returned to their normal operating state that was selected. The protection circuitry as recommended in Figure 2 can be used to meet specific requirements for secondary fault protection identified in GR-1089.

TABLE 2. LIGHTNING SURGE TESTS

V_{OPEN} (RMS)	I_{SHORT} (AMP)	R_S (Ω)	WAVEFORM (μs)	TEST CONDITIONS	NO. OF TESTS	EXPECTED CURRENT
±1kV	100	10	10/1000	Tip to Source, Ring to Gnd	25 times	40A
±1kV	100	10	10/1000	Ring to Source, Tip to Gnd	25 times	40A
±1kV	100	10	10/1000	Tip and Ring to Source	25 times	40A
±2.5kV	500	5	2/10	Tip to Source, Ring to Gnd	10 times	125A
±2.5kV	500	5	2/10	Ring to Source, Tip to Gnd	10 times	125A
±2.5kV	500	5	2/10	Tip and Ring to Source	10 times	125A

TEST PROCEDURE FOR TEST NO. 1 TO 12

1. With PTC in circuit.
2. Collect pre-test data on open tip and ring voltage and loop current readings with 600Ω load for V_{BH} and V_{BL} mode and record the data.
3. Set the scope settings.
4. Store the V_P waveforms on scope screen when first applying the test signal and record the data.
5. Continue the surge test until it is complete.
6. Collect post-test data on open tip and ring voltage and loop current readings with 600Ω load for V_{BH} and V_{BL} mode and record the data.
7. The DUT passes the test, if the difference between the pre and post-test data is less than 5%. Otherwise, the DUT fails the test.

TABLE 3. AC POWER CROSS TESTS

V_{OPEN} (RMS)	I_{SHORT} (AMP)	R_S (Ω)	TEST CONDITIONS	TEST DURATION	EXPECTED CURRENT
50	0.330	150	Tip to Source, Ring to Gnd	15 minutes	300mA
50	0.330	150	Ring to Source, Tip to Gnd	15 minutes	300mA
50	0.330	150	Tip and Ring to Source	15 minutes	300mA
100	0.170	600	Tip to Source, Ring to Gnd	15 minutes	160mA
100	0.170	600	Ring to Source, Tip to Gnd	15 minutes	160mA
100	0.170	600	Tip and Ring to Source	15 minutes	160mA
200	0.330	600	Tip to Source, Ring to Gnd	1 sec, 60 times	320mA
200	0.330	600	Ring to Source, Tip to Gnd	1 sec, 60 times	320mA
200	0.330	600	Tip and Ring to Source	1 sec, 60 times	320mA
400	0.670	600	Tip to Source, Ring to Gnd	1 sec, 60 times	630mA
400	0.670	600	Ring to Source, Tip to Gnd	1 sec, 60 times	630mA
400	0.670	600	Tip and Ring to Source	1 sec, 60 times	630mA
600	1	600	Tip to Source, Ring to Gnd	1 sec, 60 times	950mA
600	1	600	Ring to Source, Tip to Gnd	1 sec, 60 times	950mA
600	1	600	Tip and Ring to Source	1 sec, 60 times	950mA

AC POWER CROSS TEST PROCEDURE

TEST PROCEDURE FOR TEST NO. 1, 2, 3, 4, 5, 6		TEST PROCEDURE FOR TEST NO. 7, 8, 9, 10, 11, 12	
1.	With PTC in circuit.	1.	With PTC in circuit.
2.	Collect pre-test data on open tip and ring voltage and loop current readings with 600Ω load for V_{BH} and V_{BL} mode and record the data.	2.	Collect pre-test data.
3.	Store the V_P waveforms on scope screen when first applying the test signal and record the data.	3.	Store the V_P waveforms on scope screen when first applying the test signal and record the data.
4.	Set storage scope to real time mode.	4.	Set storage scope to real time mode.
5.	Record the PTC time to trip data if PTC tripped.	5.	Record the thermal alarm data if SLIC went into thermal alarm within 1 minute.
6.	Record the thermal alarm data if SLIC went into thermal alarm.	6.	Replace the PTC with a 5Ω power resistor and set the timer to 1 second on, 2 seconds off.
7.	Collect the post-test data on open tip and ring voltage and loop current readings with 600Ω load for V_{BH} and V_{BL} mode and record the data.	7.	Collect the post-test data.
8.	The DUT passes the test, if the difference between the pre and post-test data are less than 5%. Otherwise, the DUT fails the test.	8.	The DUT passes the test, if the difference between the pre and post-test data are less than 5%. Otherwise, the DUT fails the test.

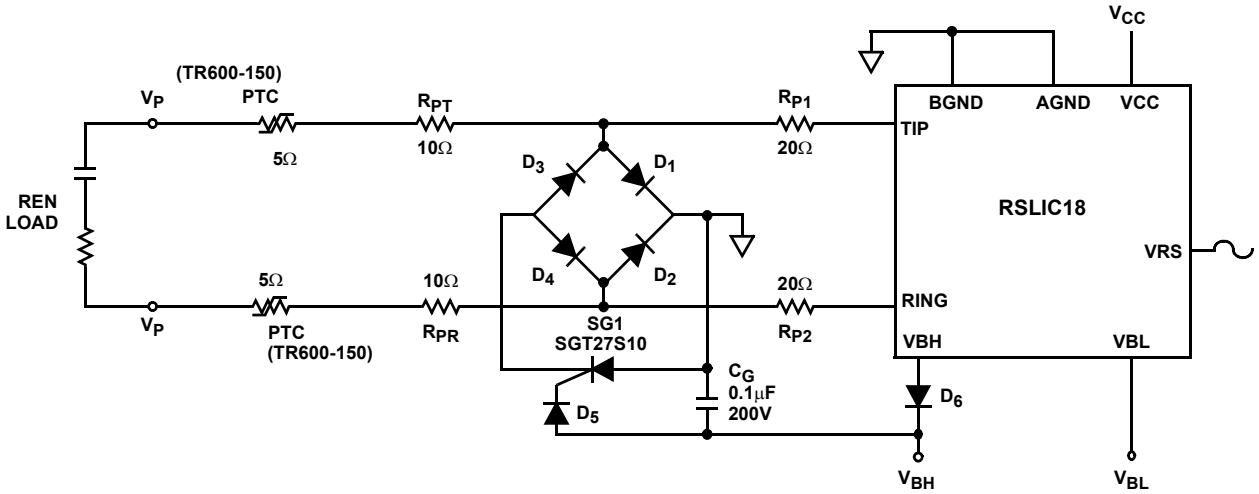


FIGURE 3. RINGING CAPABILITY TEST CIRCUIT

TABLE 4. RINGING CAPABILITY AT 1% THD

V_{BH}	1 REN	3 REN	5 REN
-90V	87.5Vp	83.5Vp	80.5Vp
-85V	83.4Vp	82.0Vp	80.5Vp
-80V	77.0Vp	74.5Vp	71.0Vp
1 REN = 6kΩ + 8µF	3 REN = 2kΩ + 24µF		5 REN = 1.2kΩ + 40µF

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