Migrating from 24-bit to 32-bit Flash Addressing

This application note is intended to help in migrating a system that uses legacy NOR flash memory with 24-bit (3-byte) addressing to one that uses a high-density NOR flash memory requiring 32-bit (4-byte) addressing. It describes new features for 32-bit addressing support. The description is based on the AT25SF2561C flash product; however, it is applicable for all other high-density products.

Contents

1. Overview

Legacy NOR flash products have been using 24-bit addressing, which let them support memory arrays of up to 128 Mbits (16 Mbytes). For higher density flash memory products, such as the Renesas AT25SF2561C, 24-bit addressing is not enough to cover the entire memory array. Thus, these products use a 32-bit addressing scheme, which enables addressing memory arrays of up to 32 Gbit (4 Gbyte).

The math is simple: with 24 address bits it is possible to access 2 to the power of 24, or 16,777,216, bytes (16 Mbytes). Any memory with a larger number of bytes must be addressed with more address bits. Because the address field in NOR flash SPI protocols includes an integral number of bytes, a leap must be made from 3 bytes to 4 bytes (from 24-bits to 32-bits).

The transition to 32-bit addressing brings some changes to the programming model, in particular the introduction of new commands and new options for old commands.

2. Summary of New Features

Multiple options are available for implementing 32-bit addressing. Some options allow a certain degree of backward compatibility with older products which use 24-bit addressing only. With those options it is possible to reduce the amount of code changes need to be applied to a host flash driver when upgrading it for 32-bit addressing.

Here is a summary of 32-bit addressing options:

- New for read, erase and program commands accepting 32-bit address only. These new commands are typically counterparts of old commands which support 24-bit addressing. They function exactly the same as their old counterparts except for the address size. Example: old read-array command with opcode 03h using a 24-bit address and a new read-array command with opcode 13h using 32-bit address.
- A new mode which changes the format of old read, erase and program commands. This mode is enabled by a new mode-change command or by setting a configuration bit in a status/configuration register. When this new mode is in effect, the old opcodes are used with a 32-bit address rather than a 24-bit address which is used by default.
- Extended address register (EAR). This third option provides 32-bit addressing indirectly by extending the 24-bit address used by old command with an 8-bit extension taken from the EAR. This option allows an application not only to keep using the old commands, but also to use them with the old format. However, this addressing method requires setting the EAR every time the upper 8-bits of the address change. It may be suitable for specific cases which will be discussed later.

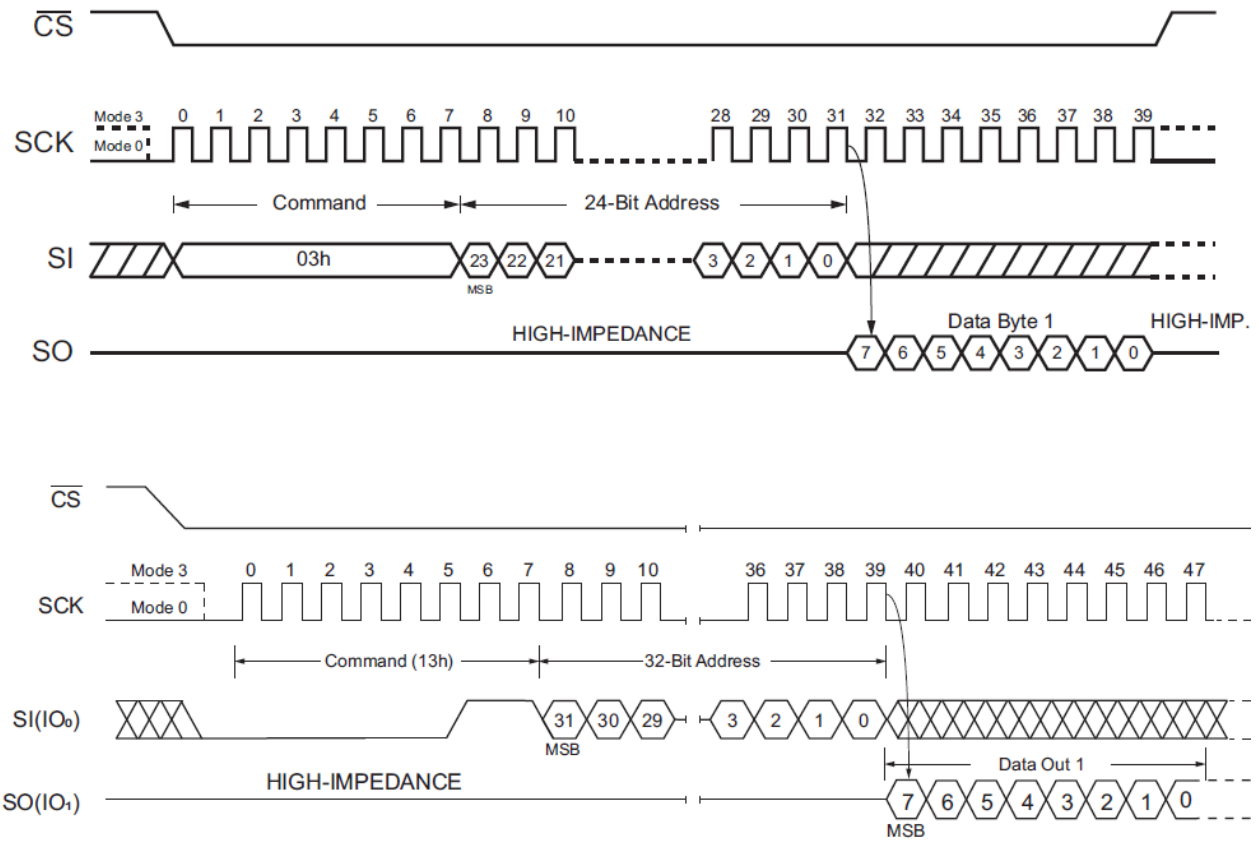
3. New Commands

High-density products, such as the Renesas AT25SF2561C, introduce multiple new commands for read, erase, and program operations. The following table lists new commands supporting 32-bit addressing alongside their old, 24-bit command counterpart:

Command Name	New Opcode – 32-bit Address	Old Opcode – 24-bit Address
Read Data	13h	03h
Fast Read	0Ch	0Bh
Fast Read Dual Output	3Ch	3Bh
Fast Read Quad Output	6Ch	6Bh
Fast Read Dual I/O	BCh	BBh
Fast Read Quad I/O	ECh	EBh
Page Program	12h	02h
Quad Page Program	34h	32h
Sector Erase (4 KB)	21h	20h
Sector Erase (32 KB)	5Ch	52h
Sector Erase (64 KB)	DCh	D8h

The new commands are available in any mode and can be used only with a 32-bit address.

For example, look at the following waveform diagrams. The first is of the old Read Data command (opcode 03h) with 24-bit address; the second is of the new Read Data command (opcode 13h) with 32-bit address.



4. New Mode

High-density products, such as the Renesas AT25SF2561C, have a new mode that changes the format of the old read, erase, program, block security and other commands. The new mode can be enabled by sending the “Enter 4-Byte Address Mode” command (opcode B7h). It can be disabled by sending the “Exit 4-Byte Address Mode” command (opcode E9h).

The read-only ADS bit in status register 3 reflects the current state of the flash.

- If ADS=0 the flash is in 3-byte (24-bit) address mode.
- If ADS=1 the flash is in 4-byte (32-bit) address mode.

Also, the ADP configuration bit in status register 3 determines whether the flash powers up in 3-byte or 4-byte address mode.

- If ADP=0 the flash memory powers up in 3-byte address mode.
- If ADP=1 the flash memory powers up in 4-byte address mode.

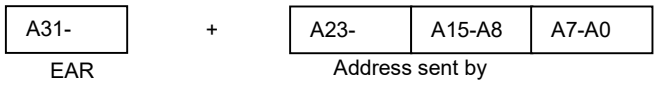
The flash address mode affects the following commands. It determines if these commands use a 24-bit address (their default format) or 32-bit address.

Command name	Opcode
Read Data	03h
Fast Read	0Bh
Fast Read Dual Output	3Bh
Fast Read Quad Output	6Bh
Fast Read Dual I/O	BBh
Fast Read Quad I/O	EBh
Page Program	02h
Quad Page Program	32h
Sector Erase (4KB)	20h
Sector Erase (32KB)	52h
Sector Erase (64KB)	D8h
Individual Block/Sector Lock	36h
Individual Block/Sector Unlock	39h
Read Block/Sector Lock	3Dh
Erase Security Registers	44h
Program Security Registers	42h
Read Security Registers	48h
Dual I/O Read Manufacture ID/ Device ID	92h
Quad I/O Read Manufacture ID/ Device ID	94h

5. Extended Address

The final option for using 32-bit addressing in high-density products is automatic address extension using the Extended Address register (EAR). This option is applicable only when the flash is in 3-byte (24-bit) addressing mode, where old commands (see table in Section 3) are used with a 24-bit address. The target address for these commands is automatically calculated as follows.

- Bits 0-23 (24 lower bits) of the address are taken from the command sent by the host.
- Bits 24-31 (8 upper bits) of the address are taken from the EAR.



The following two commands are used by the host to write and read the EAR:

Command	Opcode
Write Extended Address Register	C5h
Read Extended Address Register	C8h

The flash density determines which bits in the EAR are used for address extension. For example, in the Renesas AT25SF2561C, which has 256 Mbits of memory, only least significant bit (named EA0) of the EAR is used for address extension, this becoming bit A24 of the address. In this case, the rest of the bits (EA1-EA7) are reserved.

The extended address option allows using old commands in their short, 24-bit address format. This saves 8 clock cycles for every read, erase, or program command. However, every time any of the upper 8-bits of the address changes, the EAR must be modified using the Write Extended Address Register command. This may introduce significant overhead in cases where the application frequently moves back and forth around the memory array. Thus, the extended address option is useful in very specific cases. Here are two examples:

- The application's memory access pattern is sequential. The upper 8 bits of the memory address change rarely, only when a 128 Mbit segment boundary is crossed by the application.
- The application accesses different 128 Mbit segments at different times and does not frequently switch from one segment to another.

6. Summary

32-bit addressing is required for addressing SPI NOR Flash memories larger than 128 Mbit. The Renesas AT25SF2561C and similar high-density flash memory products offer multiple options for implementing 32-bit addressing.

When upgrading a system to 32-bit addressing, developers can choose the 32-bit addressing option that best fits their needs and modify their software driver accordingly.

7. Revision History

Revision	Date	Description
A0	12/2023	Initial release.

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