Voltage Tracking with the ZL2005

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Introduction

A common requirement for embedded system design is to be able to control and guarantee certain deterministic behavior of power sources during start-up and shut-down. The industry shift from the use of power planes to the use of a distributed power architecture has given rise to the need for an easy way control how power is applied to a single chip and across a system during start-up and shut down.

Digital-DC™ based power management and conversion ICs from Zilker Labs contain voltage tracking circuitry that makes the job of ensuring deterministic start-up power supply simple for system designers. There are several versions of tracking supported by these devices. This application note describes how to implement these features using the built-in capabilities of Zilker Labs ICs.

Overview

Power supply voltage tracking is a method of controlling a number of power supply output voltages. Powering a mix of integrated circuit technologies requires careful consideration of relative voltage levels between each technology. It is usually very important that a certain power supply rail does not exceed another power supply rail's level under any condition. An example of this requirement is in the powering of a microcontroller's core voltage versus powering its I/O pads. The core voltage is typically a lower value than the I/O pad voltage. Because of certain characteristics of the microcontroller's integrated technology the core voltage should not exceed the I/O pad voltage. Therefore, voltage tracking is implemented to keep the lesser power supply voltage always below a master power supply voltage.

The ZL2005 includes an analog input pin, VTRK, which is used to track another voltage supply. When the ZL2005 is configured to the voltage tracking mode, the voltage applied to the VTRK pin acts as a reference for the device's output regulation. Softstart settings are ignored and the output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin. The delay setting is only used on the turn-off end of the tracking condition. The delay setting sets the timeout for the tracking voltage to turnoff in the event that the tracked voltage does not achieve zero volts. Certain tracking modes are also configurable to set the percentage of tracking and response to the power good signal.

In a tracking group, the ZL2005 device that is set to the highest voltage within the group is defined as the master device. This master device will control the ramp delay and ramp rate of all tracking devices and is not itself placed in the tracking mode. The master device is configured to the highest output voltage for the group since all other device output voltages are meant to track and never exceed the master device output voltage. A delay of at least 10 ms must be configured into the master device. This delay allows the tracking devices to prepare their control loops for tracking following the ENABLE pin assertion. It is assumed for a tracking ZL2005 group, that all of the ENABLE pins are connected together and driven by a single logic source.

Tracking Mode Configured by Pin-strap

The configuration of a master ZL2005 is set by pin-strap to achieve the desired output voltage with delay and ramp time set accordingly. The master device must have a pin-strap delay setting of at least 10 ms (DLY1, DLY0 = open, open). The master device is not configured to be in the tracking mode.

The tracking devices are configured for tracking mode and will simply track the voltage of the master in the manner defined by the master device and its own configuration. The method for setting tracking mode by pin-strap is to apply a resistor from SS1 to ground and applying ground directly to SS0. The DLY1, DLY0 pins are then used to set the delay time for turn-off only. This ensures the tracking device will turn off in the event that the tracked voltage does not decay to zero within the amount of time set by DLY1, DLY0. Refer to the ZL2005 data sheet for the tracking mode pin-strap definitions.

Example of Tracking Configured by Pin-strap

ZL2005 Device Setting

Table 1 describes the pin-strap values applied to each ZL2005EV1 to prepare the device on each EVB for tracking configuration.

Table 1. ZL2005 Device Settings

Pin	Master Device, EVB #1	Tracking Device, EVB #2
SA1, SA0	low, low (address x20)	low, open (address x21)
V1, V0	high, low (2.5V)	open, low (1.2V)
SYNC	open (auto detect)	open (auto detect)
CFG	low (SYNC pin is input)	low (SYNC pin is input)
DLY1, DLY0	open, open (10 ms delay, minimum for master device)	high, low (50 ms turn-off delay)
SS1, SS0	open, high (20 ms ramp time & PG delay)	16.2 kΩ, low (tracking mode, $V_{LIM} = V_{TRK}$, 50%)
ILIM1, ILIM0	open, high (70 mV/2.7 mΩ = 25.9A)	open, high (70 mV/2.7 mΩ = 25.9A)
FC1, FC0	open, high (stable for power train)	open, high (stable for power train)
UVLO	open (4.5V min)	open (4.5V min)

ZL2005EV1 EVB Connections and Settings for Tracking

The following steps describe the connections and settings of two ZL2005EV1 evaluation boards to demonstrate the tracking mode. These connections and settings are valid for a tracking demonstration by pin-strap or PMBus command.

1. Connect the evaluation boards together using J13 of EVB #1 (address x20) and J12 of EVB #2 (address x21). The inter-device bus, ENABLE and SYNC pins are connected together via these connectors.
2. Place the ENABLE jumper to the "MSTR EN" position on both boards.
3. Set the ENABLE switch of EVB #2 to the middle position (MONITOR).
4. Connect USB cable from PC to USB jack.
5. Connect RTN of EVB #1 to RTN of EVB #2.
6. Connect VIN of EVB #1 to VIN of EVB #2.
7. Connect the power source GND to RTN and V+ to VIN.
8. Turn the input power source on.
9. Enable outputs by the ENABLE switch on board #1

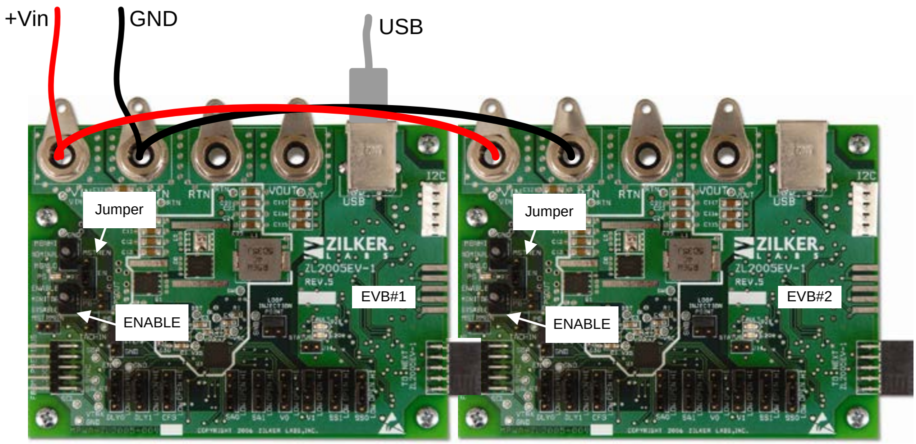

Figure 1. EVB Connections for Tracking

Tracking Mode Configured by PMBus

The ZL2005 includes a PMBus command set that supports configuration of the tracking mode. All turn-on and turn-off parameters are set by PMBus commands in the master device. All devices within a tracking group should have their steady-state operating parameters set via PMBus, including fault parameters.

Pin-strap Settings for Configuring by PMBus

Certain initial parameters must be set by pin-strap when configuring the ZL2005 by PMBus. This section describes only the pin-strap settings that are required before configuring the tracking mode through PMBus commands.

The device address is set for each ZL2005 by pins SA1 and SA0. The address for each device can be selected to fit a system's SMBus addressing scheme. The only restriction on device addressing within a tracking group is the consideration of a device's phase position when placed in a synchronized phase spreading tracking group. Even this restriction is not necessary if the PMBus command, INTERLEAVE, is used. Refer to AN2013, "ZL2005 PMBus Command Set" for description of the INTERLEAVE command.

The output voltage setting pins, V1 and V0, are used to establish the maximum output voltage that the device can be set to by a PMBus command. The output voltage pin-strap setting is used to provide a level of protection of the maximum system operating range.

Other pin-strap settings can be configured to achieve certain power up conditions. This is not necessary since the PMBus commands allow the user to set any and all parameters.

PMBus Commands for Tracking Mode

Many PMBus commands can be used to precisely configure the ZL2005 to fit an application. This section describes the PMBus commands that are specific to configuring the tracking mode. These commands for a tracking device are TRACK_CONFIG, TON_DELAY and VOUT_COMMAND. See Zilker Labs Application Note AN2013 for a complete list of PMBus commands.

The TRACK_CONFIG command is used to enable the tracking mode. This command also has bit fields that set options for the tracking mode. The tracking ratio bit sets the tracking percentage to either 50% or 100%. A 50% tracking ratio is typically selected unless the target voltage of the tracking device is set to more than 50% of the target voltage of the master device. In that case, the 100% tracking ratio must be used. The control of ramp-up behavior bit is a third settable option in the TRACK_CONFIG command. This bit sets the behavior of the output voltage during ramp-up in the case that the master voltage does not reach its target voltage and the tracking voltage does not reach the power good threshold. This option allows the tracking device to ramp-down without having to exceed the power good threshold first.

A master device in a tracking group must have its turn-on delay set to a minimum of 10 ms. This provides time for initialization of the tracking devices following the enable event. The master tracking device set the delay for the tracking group. The SS(1:0) pins or the TON_DELAY command is used to do this.

The disable delay time for the tracking device must be set to the sum of the disable delay time and ramp down time for the master device plus 5ms. This allows the tracking device to disable after tracking the master device to zero volts.

The output voltage of each ZL2005 circuit can be set lower than the pin-strap setting by using VOUT_COMMAND. Note that VOUT_COMMAND does not immediately change all VOUT margins and fault thresholds. These VOUT parameters will only be recalculated when the new VOUT_COMMAND value has been stored by either STORE_USER or STORE_DEFAULT then restored by a RESTORE command or power cycled on the ZL2005 device.

Example of Tracking Configured by PMBus

ZL2005 EVB Setting

Table 2 describes the pin-strap values applied to each ZL2005EV1 to prepare the device on each EVB for tracking configuration by PMBus.

Table 2. Pin-strap Settings for Tracking Configured by PMBus

Pin	Master Device, EVB #1	Tracking Device, EVB #2
SA1, SA0	low, low (address x20)	low, open (address x21)
V1, V0	high, open (3.3V, set to 2.5V via PMBus)	open, open (1.5V, set to 1.2V via PMBus)
SYNC	open	open
DLY1, DLY0	open, open (10 ms delay, minimum for master device)	high, low (50 ms turn-off delay)
SS1, SS0	open, open (10 ms ramp time & PG delay)	open, open (ignored for PMBus tracking)
ILIM1, ILIM0	open, high (70 mV/2.7 mΩ = 25.9A)	open, high (70 mV/2.7 mΩ = 25.9A)
FC1, FC0	open, high (stable for power train)	open, high(stable for power train)
UVLO	open (4.5V min)	open (4.5V min)
CFG	open	open

PMBus Configuration Files

The following text file listings are the PMBus configuration files to place a device in either master mode or tracking mode. These files are referred to as PowerPlans. PowerPlans are downloadable to the ZL2005 using the ZL2005 Evaluation Software. For purposes of this example, the PowerPlan for EVB #1 is downloaded to the master device on the EVB set for address 0x20. The PowerPlan for EVB #2 is downloaded to the tracking device on the EVB set for address 0x21.

Tracking Example – PMBus configuration file for master device on EVB #1

```
#ZL2005EV1_Tracking_EVB #1
#PowerPlan file
#
#PMBus Command-     Value
#
#Erase user store
RESTORE_FACTORY
STORE_USER_ALL
STORE_DEFAULT_ALL
#
#Set output voltage of the first EVB to 2.5V
VOUT_COMMAND  0x5000
#
#Set output peak/valley current protection to 30 to -10A
IOUT_OC_FAULT_LIMIT 0xDBC0
IOUT_UC_FAULT_LIMIT 0xD580
#
#Set output average current protection to 25A to -8A
IOUT_AVG_OC_FAULT_LIMIT    0xDB20
IOUT_AVG_UC_FAULT_LIMIT    0xD600
#
#Set IOUT_SCALE to 2.7mOhms
IOUT_SCALE   0xC2B3
#
#Set IOUT_CAL_OFFSET to -3.5A
IOUT_CAL_OFFSET     0xC480
#
#Use Rdson current sense method with external tempco sensor
MFR_CONFIG   0xABC1
#
#Set temperature compensation at 4400ppm/ C
TEMPCO_CONFIG 0xAC
#
#PID taps
PID_TAPS     A=1634, B=-2799, C=1227
#
#NLR_CONFIG  Enable,1.5%,No Outer,1.5%,3,3,0
NLR_CONFIG   0xA250
#
STORE_DEFAULT_ALL
RESTORE_DEFAULT_ALL
```

Tracking Example – PMBus configuration file for master device on EVB #2

```
#ZL2005EV1_Tracking_EVB #2
#PowerPlan file
#
#PMBus Command-     Value
#
#Erase user store
RESTORE_FACTORY
STORE_USER_ALL
STORE_DEFAULT_ALL
#
#Set output voltage of the first EVB to 1.2V
VOUT_COMMAND 0x2666
#
#Set Tracking mode: Enable,limit=Vtarget,50%,decrease w/o PG
TRACK_CONFIG 0x85
#
#Set Time-off delay(2) = Toff delay(1) + Toff fall(1) + 5ms
TOFF_DELAY   25#ms
#
#Set output peak/valley current protection to 30 to -10A
IOUT_OC_FAULT_LIMIT 0xDBC0
IOUT_UC_FAULT_LIMIT 0xD580
#
#Set output average current protection to 25A to -8A
IOUT_AVG_OC_FAULT_LIMIT    0xDB20
IOUT_AVG_UC_FAULT_LIMIT    0xD600
#
#Set IOUT_SCALE to 2.7mOhms
IOUT_SCALE   0xC2B3
#
#Set IOUT_CAL_OFFSET to -3.5A
IOUT_CAL_OFFSET     0xC480
#
#Use Rdson current sense method with external tempco sensor
MFR_CONFIG   0xABC0
#
#Set temperature compensation at 4400ppm/ C
TEMPCO_CONFIG 0xAC
#
#PID taps
PID_TAPS     A=1634, B=-2799, C=1227
#
#NLR_CONFIG  Enable,1.5%,No Outer,1.5%,3,3,0
NLR_CONFIG   0xA250
#
STORE_DEFAULT_ALL
RESTORE_DEFAULT_ALL
```

Tracking Example – Performance

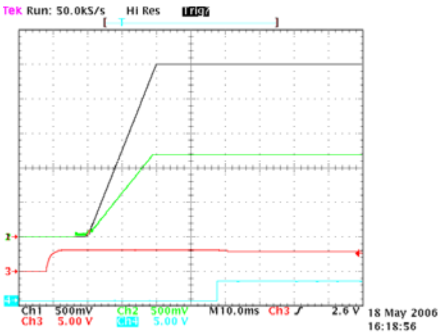

Figure 2. Enable Sequence

Channel 1 = VOUT, EVB #1
Channel 2 = VOUT, EVB #2
Channel 3 = ENABLE (trigger)
Channel 4 = Power Good, EVB #2

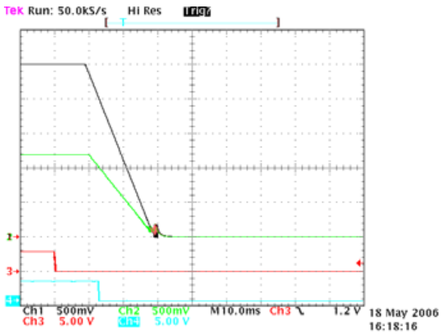

Figure 3. Disable Sequence

Channel 1 = VOUT, EVB #1
Channel 2 = VOUT, EVB #2
Channel 3 = ENABLE (trigger)
Channel 4 = Power Good, EVB #2

Figure 2 shows the scope is set to trigger on the ENABLE event. The ENABLE signal is the first to go high. The next signal to change is the beginning of the VOUT1 turn-on ramp since it has been configured to be the master device of the tracking group. It occurs 10 ms after ENABLE (DELAY1 set to 10 ms). The time of the VOUT1 ramp is 20 ms (softstart set to 20 ms). VOUT2 then begins tracking at 50% of VOUT1. The ramp time for VOUT2 is set by the combination of the ramp time of VOUT1 and the VOUT2 target voltage. Power Good 2 goes high 10ms after VOUT2 is above the power good threshold (by default, power good delay = softstart = 20 ms).

Figure 3 shows the scope is set to trigger on the ENABLE event. The ENABLE signal is the first to go low. The delay for VOUT1 to begin its turn off is set to 10 ms. The ramp time for VOUT1 is 20 ms (softstart set to 20 ms).The next signal to change is the VOUT2 turn off ramp since it has been configured to track 50% of VOUT1. The next signal to change is the Power Good 2 which goes low after VOUT2 drops below the power good threshold.

References

[1] *ZL2005 Data Sheet*, Zilker Labs, Inc., 2006.

[2] AN2013 – *ZL2005 and PMBus™*, Zilker Labs, Inc., 2006.

Revision History

Date	Rev. #	
July 10, 2006	1_0	Initial Release
October 3, 2006	1.1	Updated EVB picture on Page 3
May 4, 2009	AN2023.0	Assigned file number AN2023 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to app note content.

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