

### Introduction

The ISL75052SEH is a radiation hardened, single output LDO specified for an output current of 1.5A. The device operates from an input voltage range of 4.0V to 13.2V and provides for output voltages of 0.6V to 12.7V. The output is adjustable based on a resistor divider setting. Dropout voltages as low as 75mV (at 0.5A) typical can be realized using the device. This allows the user to improve the system efficiency by lowering  $V_{IN}$  to nearly  $V_{OUT}$ .

The SPICE model for the ISL75052SEH was developed to help system designers evaluate the operation of this IC prior to or in conjunction with proto-typing a system design. This model accurately simulates typical performance characteristics at room temperature (+25 °C) such as frequency analysis, steady state analysis, and transient analysis. Behaviors not supported are the bias current cancellation circuit and some temperature analysis. Functionality has been tested on ORCAD 10.0 and CADENCE ORCAD 16.5. Other SPICE simulators may be used, however, the model may require translation.

### Reference Documents

- ISL75052SEH Data Sheet; [FN8456](#)
- ISL75052SEH SMD [5962-13220](#)

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### Project Files

The zip file: **ISL75052SEH.zip** contains the project file ISL75052SEH.opj to be used in ORCAD simulator. The project file has the model definition file (.lib), symbol file (.olb) and various design files (.dsn) to simulate start up, OCP, load transients, etc. The application circuit is shown in Figure 1. Figures 2 through 9 show a comparison of the simulation results versus bench results for various tests. The close agreement between model and actual measurement demonstrate the accuracy of the model, making it a very powerful tool.

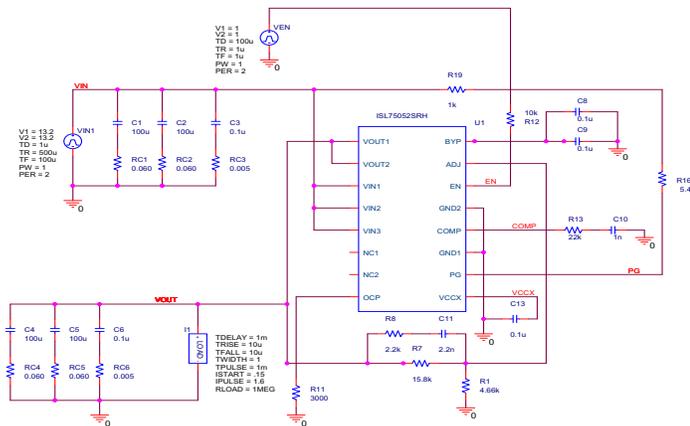


FIGURE 1. ISL75052SEH

# Simulation Performance Curves

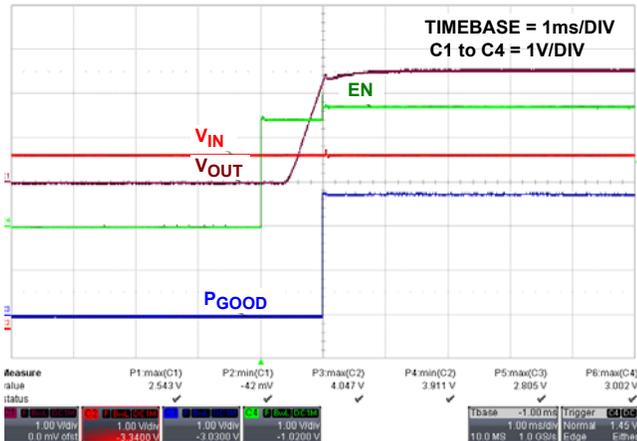


FIGURE 2. +25 °C START-UP WITH ENABLE, VIN = 4V, VOUT = 2.5V, IOUT = 1.5A

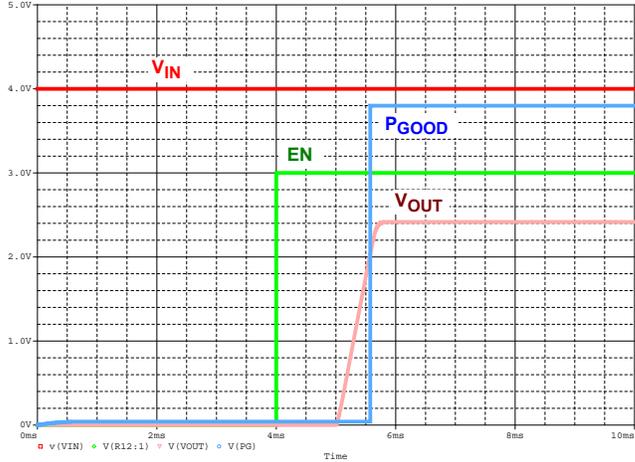


FIGURE 3. SIMULATED +25 °C START-UP WITH ENABLE, VIN = 4V, VOUT = 2.5V, IOUT = 1.5A

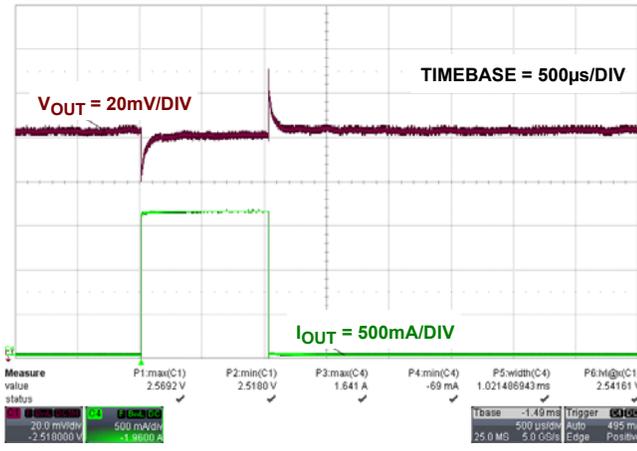


FIGURE 4. LOAD STEP RESPONSE, +25 °C, VIN = 4.0V, VOUT = 2.5V, IOUT = 0.15A TO 1.6A, COUT = 200µF, 30mΩ

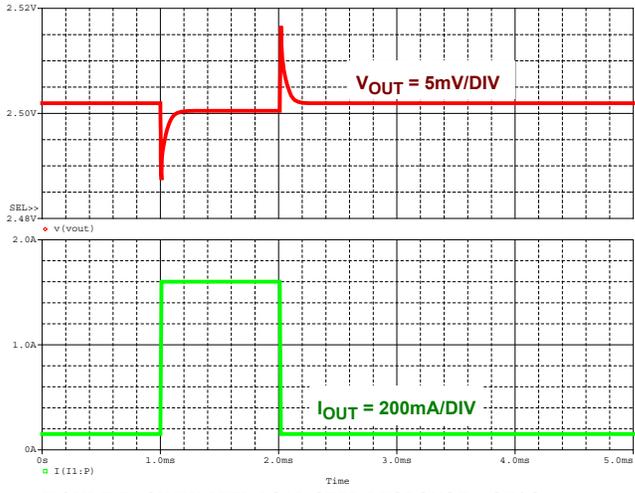


FIGURE 5. SIMULATED LOAD STEP RESPONSE, +25 °C, VIN = 4.0V, VOUT = 2.5V, IOUT = 0.15A TO 1.6A, COUT = 200µF, 30mΩ

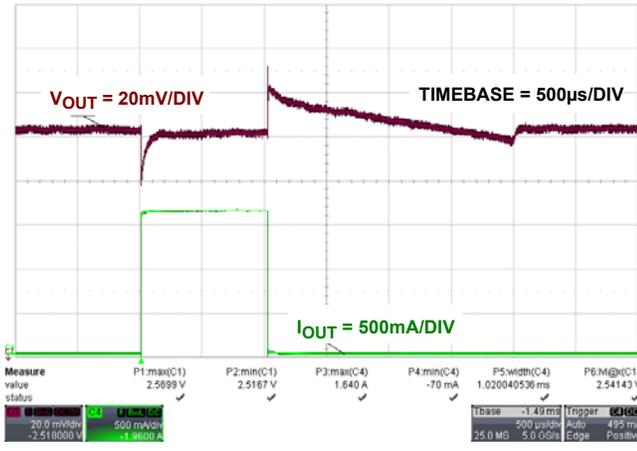


FIGURE 6. LOAD STEP RESPONSE +25 °C, VIN = 4.0V, VOUT = 2.5V, IOUT = 0A TO 1.6A, COUT = 200µF, 30mΩ

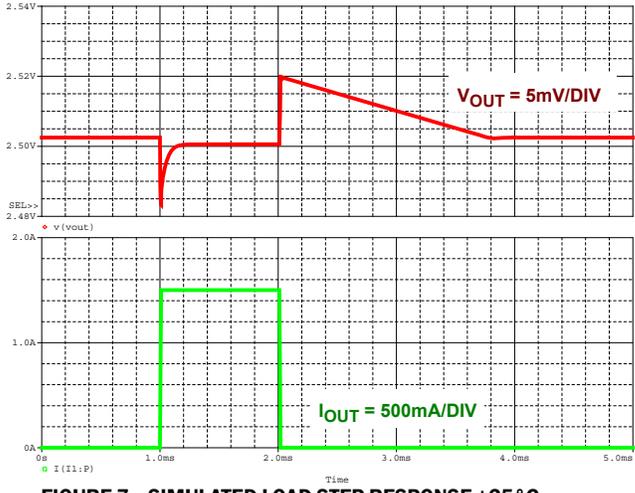
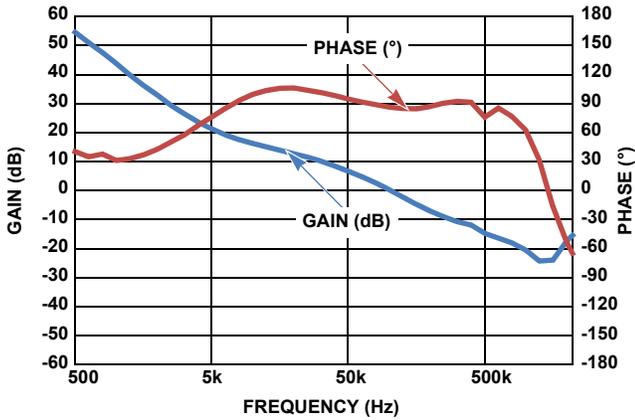
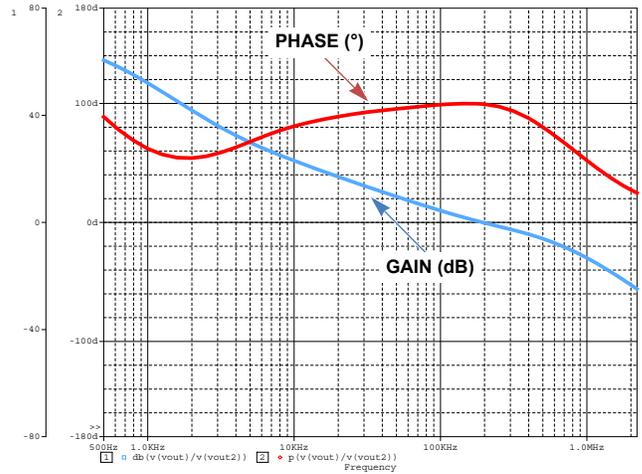


FIGURE 7. SIMULATED LOAD STEP RESPONSE +25 °C, VIN = 4.0V, VOUT = 2.5V, IOUT = 0A TO 1.6A, COUT = 200µF, 30mΩ

## Simulation Performance Curves (Continued)



**FIGURE 8. GAIN PHASE PLOTS,  $V_{IN} = 4V$ ,  $V_{OUT} = 2.5V$ ,  $I_{OUT} = 1.5A$ ,  $R_{COMP} = 22k$ ,  $C_{COMP} = 1nF$ ,  $C_{OUT} = 200\mu F$ ,  $30m\Omega$ . PHASE MARGIN =  $84.56^\circ$ , GAIN MARGIN =  $18.06dB$**



**FIGURE 9. SIMULATED GAIN PHASE PLOTS,  $V_{IN} = 4V$ ,  $V_{OUT} = 2.5V$ ,  $I_{OUT} = 1.5A$ ,  $R_{COMP} = 22k$ ,  $C_{COMP} = 1nF$ ,  $C_{OUT} = 200\mu F$ ,  $30m\Omega$ . PHASE MARGIN =  $84.56^\circ$ , GAIN MARGIN =  $18.06dB$**

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1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.  
Tel: +1-408-432-8888, Fax: +1-408-434-5351

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9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-651-700, Fax: +44-1628-651-804

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852-2886-9022

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**  
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics India Pvt. Ltd.**  
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

**Renesas Electronics Korea Co., Ltd.**  
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5338