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Development of a Spice Op-Amp Macro Model for Current-Feedback AmplifiersDC/DC Module Trim with Digital Potentiometers

Current-feedback amplifiers (CFAs) are the high-speed relatives of more common voltage-feedback amplifiers (VFAs). CFAs have wider bandwidths and faster slew rates. Applications such as DSL rely on their fast and strong output drives.

Models are important because they allow engineers to test designs before they go through the time-intensive and costly process of building a working prototype. In this application note, we introduce you to a circuit model for a current-feedback amplifier. Since it would take far too long to simulate every nuance of a complete design, this macro model simulates the most common effects, such as transient response, frequency response, voltage noise and output slew rate limiting. Detailed descriptions of each stage in the model will be presented with examples of model performance and correlation to actual device behavior.

Figure 1 shows the conceptual approach of the current feedback amplifier. CFAs have a unity gain buffer to force the inverting input (Vin-) to follow the non-inverting input (Vin+). This topology is very different from the high impedance inputs of the voltage-feedback amplifier. In the CFA case, the inverting input node shows the low input impedance (Zin-) from the output of the buffer. The error signal is the current (I) flowing into or out of the inverting node. The error current is converted by a large transimpedance, Z, to the output voltage. Rf is used to control the feedback current. This is another major deviation from the voltage-feedback topology. In VFAs, the feedback network (Rf and Rg) primarily set the voltage gain. In CFAs, the feedback network does set the gain, but the value of Rf also controls the bandwidth of the amplifier.

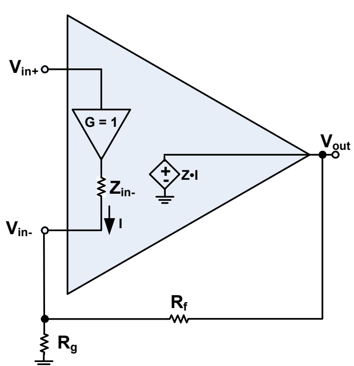

FIGURE 1. THE BLOCK DIAGRAM OF A CURRENT FEEDBACK AMPLIFIER

A five-stage model represents the actual circuit and the block diagram is shown in Figure 2. These five basic blocks are the input stage, the gain stage, the frequency-shaping stage, the output stage and the noise module.

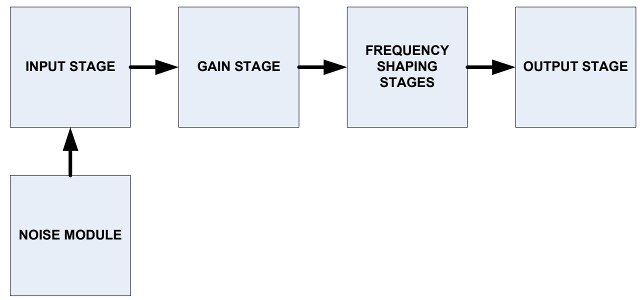

FIGURE 2. THE BLOCK DIAGRAM OF A CFA MACRO MODEL

The Input Stage

As stated, the biggest difference between a CFA and a VFA is the input stage. Figure 3 shows an example, the input stage of a CFA model. Four bipolar transistors are included, Q1 to Q4. The effective output of this stage is at nodes 11 and 12, which are coupled into the gain stage by using voltage controlled current source. The bias current I1-I2 of Q1-Q2 should be set by:

$$I_1 = I_2 = \frac{kT}{2q \bullet Z_{in-}} \quad \text{i.e.} \quad Z_{in-} = \frac{1}{2g_m} \qquad \text{(EQ. 1)}$$

The impedance at the inverting input, Zin-, can be measured. In this example, I1 = I2 = 85µA. R1, R2, C1, C2 are used to fit the frequency response and to control the input stage slew rate.

There are many other components used in the input block. Cs1 and Cs2 are the inverting input capacitance. Cin1 is the non-inverting input capacitance. The input bias current is modeled by current sources Ib1 and Ib2. The input offset voltage is modeled by the voltage source Vos. The current source Gb1 is used to model the input current common mode rejection at the inverting input.

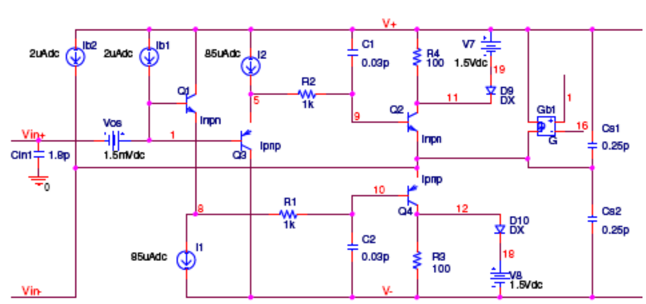

FIGURE 3. INPUT STAGE OF A CFA (EL5165)

The Gain Stage

This stage is similar to the gain stage of a VFA. It performs many important functions.

1. This stage sets the open loop trans-impedance of the part.
2. It provides output slew rate limiting.
3. It contributes the dominant pole to the AC characteristic.
4. It level shifts the signal from two voltages referred to the supplies to a single voltage referred to the mid-point.
5. It limits the output voltage swing.

Taking a closer look at the components of the gain stage in Figure 4, slew rate limiting is set by limiting the current to C3 and C4 in Figure 4. The current limiting is set in the input stage by clamping the voltage across R3 and R4 shown in Figure 3. This voltage is decided by voltage sources V1 and V2 and diodes D1 and D2. R7-C3 and R8-C4 decide the dominant pole of this model. D3-D4 and V5-V6 are used to control the output clamping voltage.

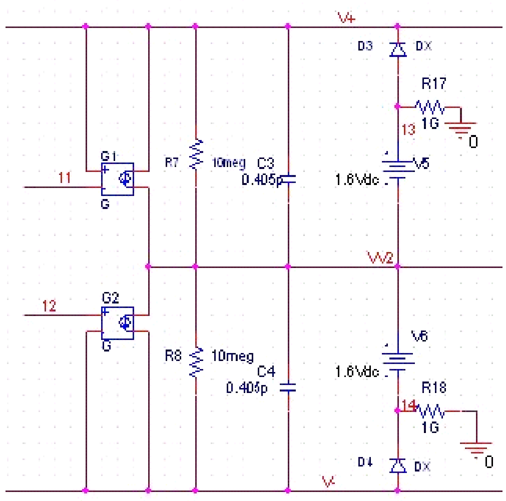

FIGURE 4. GAIN STAGE

Frequency-Shaping Stages

The frequency-shaping stages of a CFA model are very similar to that of a VFA. Each frequency-shaping block provides unity gain, so it is easy to add more poles and zeros. For more information of the frequency-shaping stages, see [Reference 2]. For our example op amp, only three pole stages are used, which is shown in Figure 5. E3 is used to set the reference level at the middle of the supplies, V+ and V-.

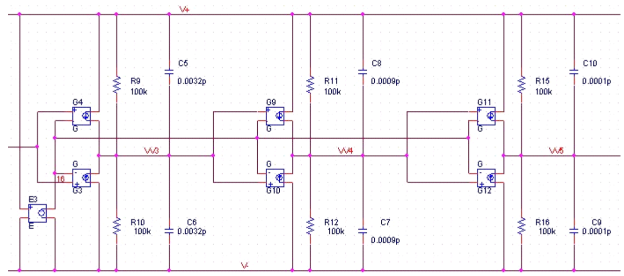

FIGURE 5. HIGHER ORDER POLE STAGES

Noise Module

The input current noise of the current feedback op amp model can't be neglected. It is described as:

$$pA/\sqrt{Hz}$$

Voltage noise is also important, so both a voltage noise module and a current noise module are needed for our CFA model.

For the right noise analysis, one trick called "noiseless resistors" can be used at the input stage. All the resistors in the input stage should be substituted by voltage controlled current sources (Device G in SPICE) where input and output terminals are connected together and the gm is set to the reciprocal of the required resistance.

We will use two pieces to construct the total noise model. The noise module of Figure 6 generates 1/f and white noise by using a 1.5V voltage source biasing a diode-resistor series combination. White noise is generated by the thermal noise-current generated in the material of the resistors.

$$i_n^2 = \frac{4kT}{R}$$ **where k is the Boltzmann's constant** (EQ. 2)

So the required value of the resistor for a given noise-voltage spectral density is:

$$R = \frac{e_n^2}{2 \times 4kT}$$ **where en is the spectral density of the white noise voltage** (EQ. 3)

Flicker noise, also called 1/f noise, refers to the noise exhibiting power spectral density inversely proportional to the frequency. More generally, this noise has a spectral density of:

$$S_N \propto \frac{1}{|f|^{\beta}}$$ **where B > 0** (EQ. 4)

As a data point, the frequency where the flicker noise curve crosses the white noise curve is defined as the corner frequency. The small amount of flicker noise that remains is modeled within the SPICE diode model. Referring to Figure 6,

$$i_n^2 = 2qI_d + KF \bullet \frac{I_d^{AF}}{frequency}$$ (EQ.5)

where Id is the DC diode current. AF and KF are the model parameters of the SPICE diode and q is the charge of the electron. The flicker noise exponent (AF) is set to 1 and the flicker noise coefficient (KF) is set:

$$KF = \frac{E_a^2}{2R^2 \bullet I_d} \quad \text{(EQ. 6)}$$

where Ea is the noise-voltage spectral density at 1Hz.

The simulated voltage noise will show the 1/f noise-voltage spectral density with the correct corner frequency.

The noise module in Figure 7 only simulates the white noise portion of the current noise by utilizing thermal noise of two parallel resistors.

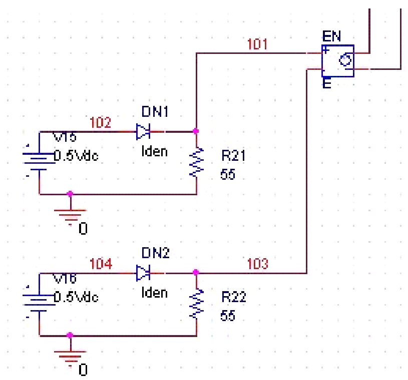

FIGURE 6. NOISE VOLTAGE MODULE

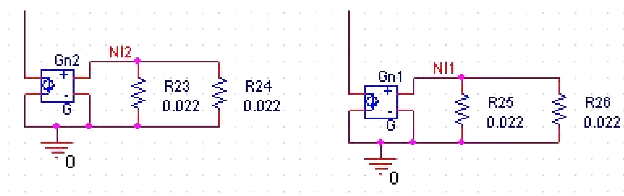

FIGURE 7. NOISE CURRENT MODULE

Output Stage

After the frequency shaping-stages, the signal appears at Node VV5, which is referenced to the midpoint of the two supply rails. Each controlled source can generate enough current to support the desired voltage drop across its parallel resistor. R13 and R14 are equal to twice the open loop output resistance, so their parallel combination gives the correct Zout. D5-D8 and G9-10 are used to force a current from the positive rail to the negative rail to correct the real current sink or source. G11-12 drive the output.

$$G9 = G10 = G11 = G12 = \frac{1}{2Z_{out}} \quad \text{(EQ. 7)}$$

$$R13 = R14 = 2Z_{out} \quad \text{(EQ. 8)}$$

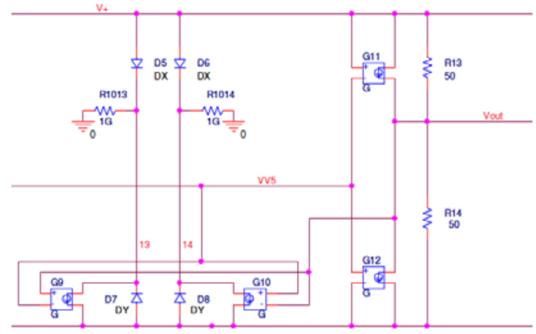

FIGURE 8. OUTPUT STAGE

Simulation Results

The simulation results of the macro model should be compared with the real world device to verify its functionality. The example op amp used in this application note is the EL5165, a high speed current feedback amplifier. Some SPICE simulation results are compared with the measured results.

The gain plots in Figure 9 shows a remarkable similarity between our model on the left at a gain of two and measurements from the EL5165 on the right. The measurements from the device are taken at both unity gain and a gain of two. There is less than 1% error between the -3dB frequency of the two gain-of-two measurements.

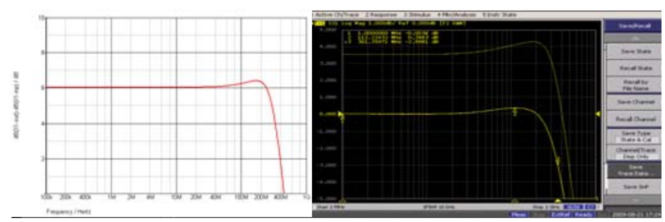

FIGURE 9. AC RESPONSE FOR GAIN = +2 OF THE MACRO MODEL (LEFT) AND EL5165 (RIGHT) (Rf = 499Ω)

At a gain of three, the discrepancy increases a bit, as shown in Figure 10. Now the error in cut-off frequency is within 5%.

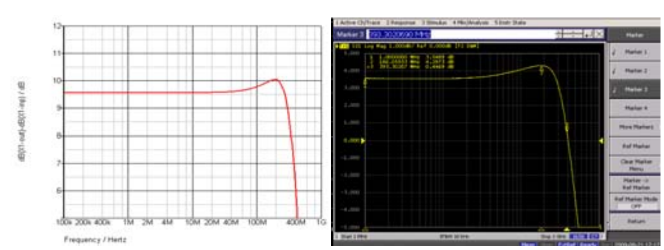

FIGURE 10. AC RESPONSE FOR GAIN = +3 OF THE MACRO MODEL (LEFT) AND EL5165 DEVICE (RIGHT) (Rf = 249Ω)

Since the feedback resistor controls the bandwidth, we offer a comparison of frequency response for a range of resistors in Figure 11. The values of resistance are listed on the plot on the right that comes from the data sheet. The left plot is from our macro model. Again, the matching of -3dB frequency is within 5%.

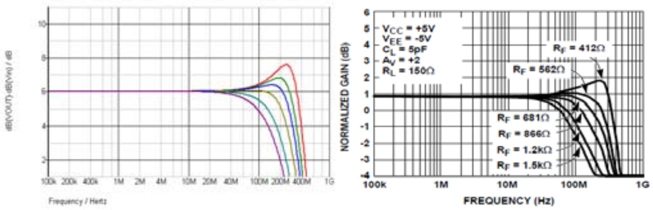

FIGURE 11. FREQUENCY RESPONSE WITH DIFFERENT RF FOR THE MODEL (LEFT) AND THE DEVICE (RIGHT)

After examining the small-signal response versus frequency, the next logical step is to inspect the large-signal response, as shown in Figure 12. Here we look at the slew rate of the step response with a gain of two driving a load of 150Ω from a ±5V supply. While the time base (x-axis) is at different resolutions in the two plots, the slew rate of the macro model shown on the left is 5000V/µs. This agrees to 5% from the slew rate on the output signal of the EL5165 on the right.

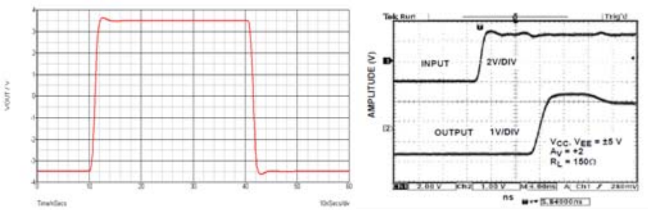

FIGURE 12. LARGE-SIGNAL STEP RESPONSE FOR THE MACRO MODEL (LEFT) AND FROM THE DEVICE DATA SHEET (RIGHT)

After frequency response and slew rate, our next goal is to match the noise performance. We have chosen to demonstrate the voltage noise, so the model in Figure 6 is included, but not the current noise model from Figure 7. The voltage noise model exhibits the spectrum shown in the plot on the left and has a value of

$$2.15 \quad nV/\sqrt{Hz} \text{ at 1MHz}$$

The datasheet curve for voltage noise is on the right and has a value of:

$$2.1 \quad nV/\sqrt{Hz} \text{ at 1MHz.}$$

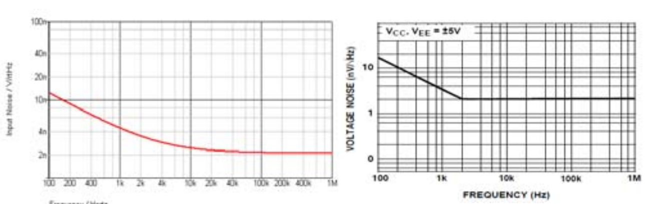

FIGURE 13. INPUT NOISE VOLTAGE VERSUS FREQUENCY FOR MACRO MODEL (LEFT) AND DEVICE DATA SHEET (RIGHT)

Conclusion

A more comprehensive SPICE macro model for a current feedback amplifier is developed. This macro model includes effects such as transfer response, accurate AC response, DC offset and voltage noise. It is convenient to use such a model and change the parameters to fit other current feedback amplifiers.

Several of Intersil's current feedback amplifiers use the same model topology with different internal model values.

EL5165 Macro Model Netlist

```
.subckt EL5165 3 2 7 4 6
*
*Input Stage
C_Cin1 0 3 1.8p
V_Vos 1 N4150175 1.5mVdc
I_I1 8 4 DC 85uAdc
I_I2 7 5 DC 85uAdc
I_Ib1 7 1 DC 2uAdc
I_Ib2 7 2 DC 2uAdc
G_Gi1 8 10 8 10 0.001
G_Gi2 5 9 5 9 0.001
G_Gi3 12 4 12 4 0.01
G_Gi4 7 11 7 11 0.01
G_Gb1 7 2 1 16 0.0000001
Q_Q1 7 1 8 Inpn
Q_Q2 11 9 2 Inpn
Q_Q3 4 1 5 Ipnp
Q_Q4 12 10 2 Ipnp
D_D9 19 11 DX
D_D10 12 18 DX
V_V7 7 19 1.5dc
V_V8 18 4 1.5Vdc
C_C1 9 7 0.03p
C_C2 4 10 0.03p
C_Cs1 2 7 0.25p
C_Cs2 4 2 0.25p
I_I3 7 4 DC 3mAdc
*Gain stage
C_C3 VV2 7 0.405p
C_C4 4 VV2 0.405p
D_D3 13 7 DX
D_D4 4 14 DX
G_G1 7 VV2 7 11 0.01
G_G2 VV2 4 12 4 0.01
R_R7 VV2 7 10meg
R_R8 4 VV2 10meg
R_R17 13 0 1G
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```
R_R18       14 0 1G
V_V5        13 VV2 1.6Vdc
V_V6        VV2 14 1.6Vdc
*High-order poles
E_E3        16 4 7 4 0.5
C_C5        VV3 7  0.0032p
C_C6        4 VV3  0.0032p
C_C7        4 VV4  0.0009p
C_C8        VV4 7  0.0009p
C_C9        4 VV5  0.0001p
C_C10       VV5 7  0.0001p
R_R9        VV3 7  100k
R_R10       4 VV3  100k
R_R11       VV4 7  100k
R_R12       4 VV4  100k
R_R15       VV5 7  100k
R_R16       4 VV5  100k
G_G3        4 VV3 VV2 16 0.00001
G_G4        7 VV3 VV2 16 0.00001
G_G9        7 VV4 VV3 16 0.00001
G_G10       4 VV4 VV3 16 0.00001
G_G11       7 VV5 VV4 16 0.00001
G_G12       4 VV5 VV4 16 0.00001
*Output stage
G_G5        15 4 6 VV5 0.0001
G_G6        17 4 VV5 6 0.0001
G_G7        7 6 7 VV5 -0.04
G_G8        6 4 VV5 4 -0.04
R_R13       6 7  25
R_R14       4 6  25
D_D5        7 15 DX
D_D6        7 17 DX
D_D7        4 15 DY
D_D8        4 17 DY
*Voltage noise
E_EN        N4150175 3 101 103 1
V_V15       102 0 0.5Vdc
V_V16       104 0 0.5Vdc
D_DN1       102 101 Iden
D_DN2       104 103 Iden
R_R21       0 101  55
R_R22       0 103  55
*Current noise
R_R23       0 NI2  0.022
R_R24       0 NI2  0.022
R_R25       0 NI1  0.022
R_R26       0 NI1  0.022
G_Gn1       3 0 NI1 0 1
G_Gn2       2 0 NI2 0 1
*
* Models
*
.model lpnp pnp(is=1e-15 bf=1E9 VAF=65)
.model lnpn npn(is=1e-15 bf=1E9 VAF=65)
.model Iden d(kf=100e-14 af=1)
.MODEL DY D(IS=1E-20 BV=50 Rs=1)
.MODEL DX D(IS=1E-15 Rs=1)
.ends EL5165
```

References

[1] Derek Bowers, Mark Alexander, Joe Buxton, "A Comprehensive Simulation Macromodels for 'Current Feedback' Operational Amplifiers," IEEE Proceedings, Vol. 137, April 1990 pp.137-145.

[2] Mark Alexander, Derek Bowers, "AN-138 SPICE-Compatible Op Amp Macro-Models", Analog Devices Inc., Application Note 138.

[3] "AN-840 Development of an Extensive SPICE Macromodel for 'Current-Feedback' Amplifiers", National Semiconductor Corp., Application Note 840.

[4] "Current Feedback Amplifier Theory and Applications", Intersil Corp., Application Note 9420.

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