8V79S680

QREF-to-QCLK Phase Deterministic

Abstract

This document provides the procedure to obtain a result of S680 output QREF-to-QCLK phase deterministic. To achieve phase deterministic, the source to 8V79S680 REF and CLK input should also be phase deterministic. In the procedure, the 8V19N490 QCLK and QREF outputs are used as signal source for the 8V79S680 inputs.

This document also provides general hardware interface, register data loading, and control procedure sequences on both the 8V19N490 and 8V79S680. An example experiment result is also shown in this document. The 8V79S680 QREF-to-QCLK phase deterministic only works for QCLK divider = 1.

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1. Hardware Interface

The hardware Interface between the 8V19N490 QCLK and QREF outputs to the 8V79S680 CLK and REF inputs is shown in Figure 1. The 8V19N490 QCLK to 8V79S680 CLK input can be either AC coupling or DC coupling. The 8V19N490 QCLK can be configured to either LVPECL or LVDS style driver. For the 8V19N490 QREF output to 8V79S680 REF input interface, because the timing of the first rising edge of the 8V19N490 QREF is critical, the 8V19N490 QREF to 8V79S680 REF input must be DC coupling to avoid initial AC coupling ramp-up that causes timing uncertainty. The 8V19N490 QREF DC coupling can be either an LVDS or LVPECL style driver. **Note:** If the 8V19N490 output is set to the LVDS style driver, the Bias_Type must be set to logic high/low when the QREF output is not active, such as Bias_Type = 0.

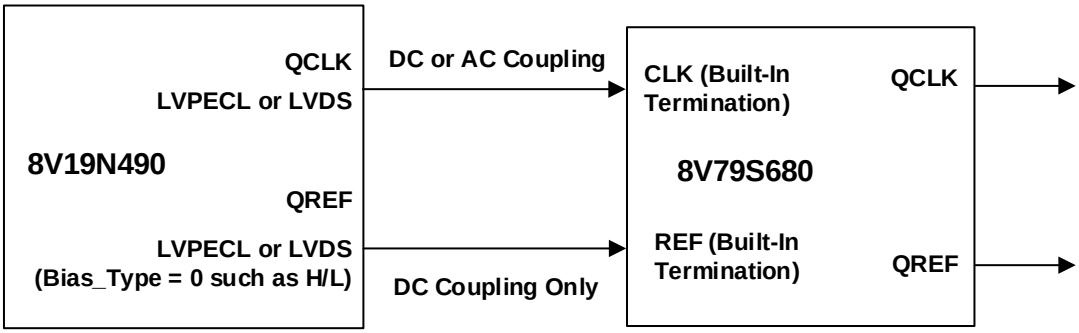

Figure 1. 8V19N490 to 8V79S680 Interface

2. Procedure

1. Power up the 8V19N490 and 8V79S680.
2. Load the 8V19N490 data to initialize and activate QCLK, but do not activate N490 Sysref.

   The data contains general settings of input/output frequency, charge pump current, desired Sysref global delay, individual delay, and other system requirement configuration.

   a. Make sure the Sysref Global Power is powered up (for example, PD_S = 0, R18 D7 = 0), and the active output of the individual QREFs are powered up (PD_QREFx = 0) and enabled (EN_QREFx = 1). Make sure Sysref Pulse R70, D7 = 0 to ensure the Sysref is not activated at this point.

   b. Sysref can be in either continuous mode or limit pulse mode. (The example in this lab used limit pulse mode with pulse count = 4).

   c. Sysref can be either an internal trigger or external trigger. (The example in the following lab section used internal trigger).
3. Initialize the 8V19N490.

   a. RELOCK = 1, R72, D7 = 1

   b. PB_CAL = 1, R73, D7 = 1

   c. INIT_CLK = 1, R71. D7 = 1

   d. QREF is not activated at this point.
4. Load the 8V79S680 data and initialize the device. At this point, the 8V79S680 QCLK output should be active. The 8V79S680 QREF is not active at this point but its REF input is ready to receive Sysref from the 8V19N490 QREF.

   a. Load the 8V79S680 data with the desire QCLK output divider and QCLK delay.

      The active QREFs are enabled; however, the signal is not active.

   b. PB_CAL = 1, R73, D7 = 1

c. RELOCK = 1, R72, D7 = 1

d. INIT_CLK = 1, R71, D7 = 1

5. Activate 8V19N490 Sysref output.

e. At the 8V19N490, write R70, D7 = 1. Both the 8V19N490 QREF and 8V79S680 REF should be active at this point. Observe the phase delay between 8V79S680 QREF first rising edge and its QCLK rising edge.

6. To observe the 8V79S680 QREF to QCLK phase deterministic, turn off the power and repeat Step 1 through Step 5. The 8V79S680 QREF to QCLK should be phase deterministic.

3. Experiment

The experiment results show the 8V79S680 QCLK-to-QREF phase deterministic. The 8V19N490 QREF to 8V79S680 is also phase deterministic. The following is the set-up condition for this experiment example.

3.1 8V19N490

- Limit pulse mode with pulse count = 4
- Internal trigger
- QCLK frequency = 491.52MHz, LVDS, AC coupling
- QREF (Sysref frequency) = 7.68MHz, LVDS, Bias_Type = 0, R19, D7 = 0, DC coupling
- Sysref global delay = 1.017ns
- Individual QREF Coarse delay = 0ps
- Individual QREF Fine delay = 0ps

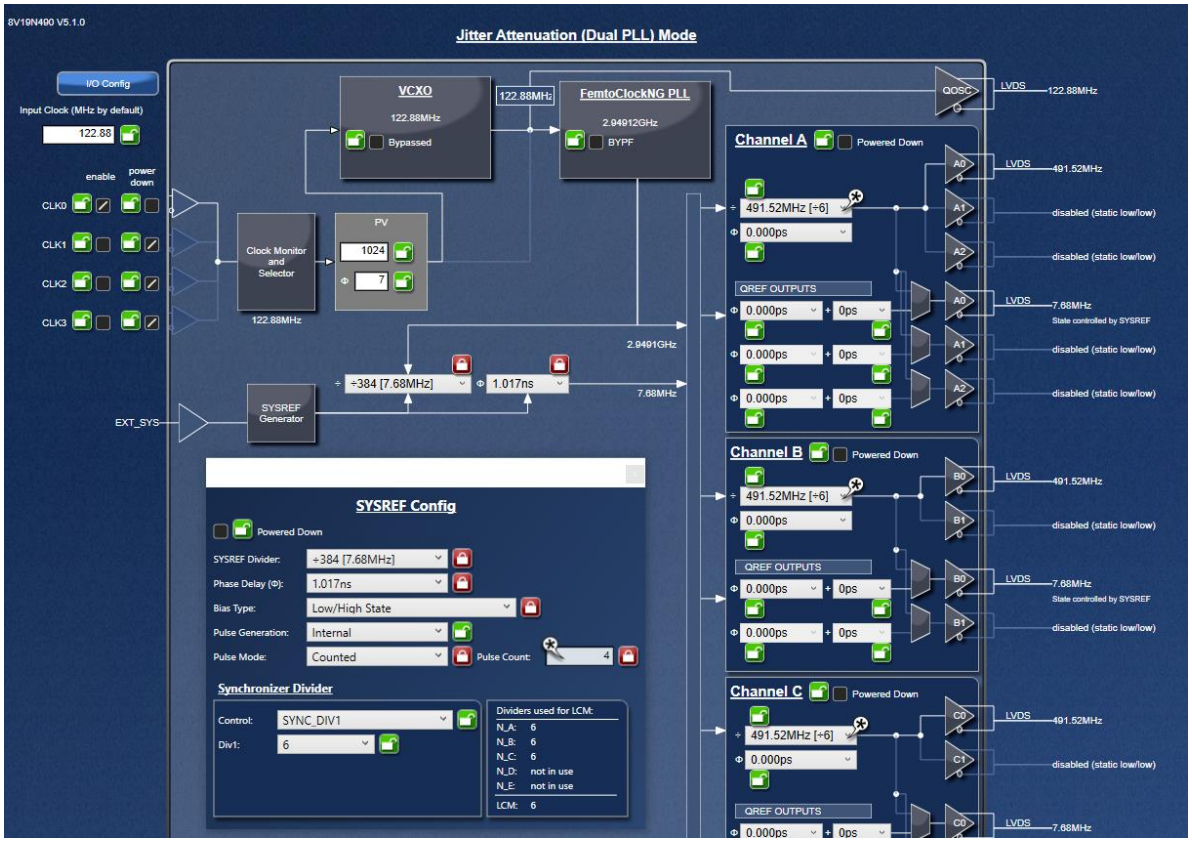

Figure 2. 8V19N490 Configuration

3.2 8V79SS680

- QCLK LVDS style
- QCLK frequency divider = 1
- QCLK phase delay setting = 31 (example only, user can adjust)
- QREF LVDS with Bias_Type = 0, R19, D7 = 0
- DLC = 01
- P_DCB = 100
- M_DCB = 100

Figure 3. 8V79S680 Configuration

3.3 Experiment Example Result

- Ch2 = N490 QREF output
- Ch1 = N490 QCLK output
- Ch4 = S680 QREF output
- Ch3 = S680 QCLK output

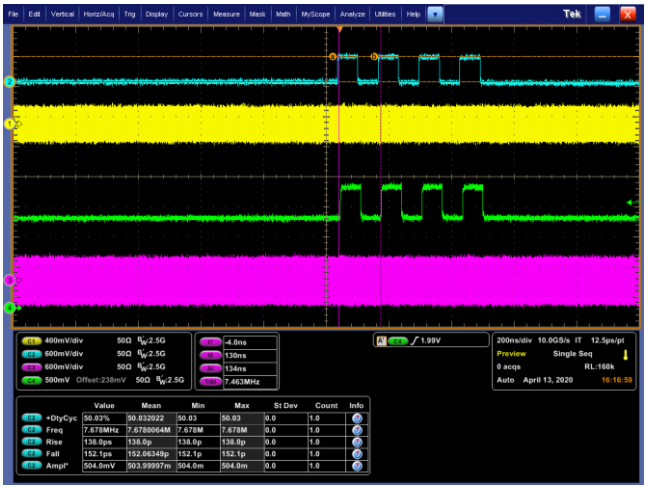

Figure 4. Waveform Sysref Limit Pulse Mode with Pulse Count = 4

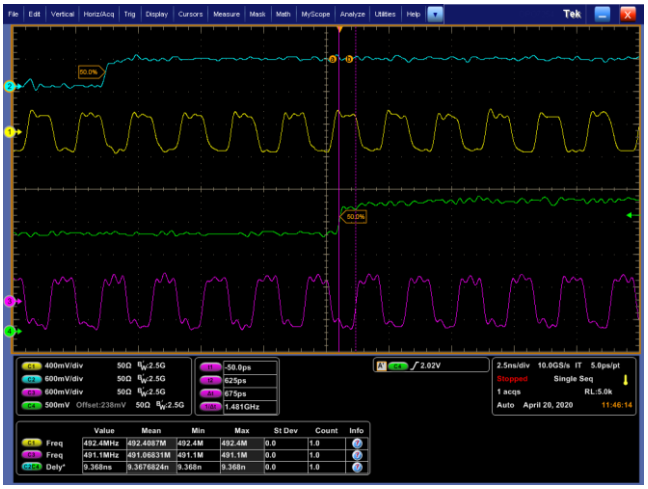

Figure 5. Zoom-In to Show 8V79S680 QREF-to-QCLK Phase Deterministic

Figure 5 is zoomed in to show the 8V79S680 QREF-to-QCLK phase deterministic as the vertical cursor marking every power-up and repeat the above steps. The 8V19N490 QREF to 8V79S680 also phase deterministic.

4. Conclusion

The 8V79S680 QREF to QCLK can be phase deterministic with proper care. The REF and CLK input must be from a phase deterministic source such as the 8V19N490 QCLK and QREF outputs. The 8V19N490 QREF output to 8V79S680 REF input interface mask is DC coupling and is set to proper Bias_Type when configured to LVDS. The 8V19N490 QCLK output to 8V79S680 CLK input interface is either DC or AC coupling. The experiment results show the phase deterministic at every power-up and followed the procedure.

5. Revision History

Revision Date	Description of Change
Oct.28.20	Initial release.

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