

## I<sup>2</sup>C Controlled Window Comparators SLG46537

The application note gives step-by-step guidelines for creating an I<sup>2</sup>C controlled window comparators using a SLG46537V device. A unique set of components of the SLG46537 allows the creation of such a system.

The application note comes complete with design files which can be found in the Reference section.

### Contents

1. Terms and Definitions .....	2
2. References .....	2
3. Introduction .....	3
4. Design overview .....	3
5. I <sup>2</sup> C operation .....	3
6. Conclusion .....	4
7. Revision History .....	5

### Figures

Figure 1. Dual window comparator design viewed in the GreenPAK Designer and I <sup>2</sup> C block configuration .....	3
Figure 2. ACMPs powering up via I <sup>2</sup> C programming of Virtual OUTs. Timing Diagram .....	4
Figure 3. ACMPs Vref programming via I <sup>2</sup> C. Timing Diagram .....	4

### 1. Terms and Definitions

ACMP	Analog Comparator
ASIC	Application-Specific Integrated Circuit
MSB	Most Significant Bit
LSB	Least Significant Bit
LUT	Look-Up Table

### 2. References

For related documents and software, please visit:

[GreenPAK Programmable Mixed-Signal Products | Renesas](#)

Download our free Go Configure Software Hub [1] to open the .gp5 files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] [Go Configure Software Hub](#), Software Download and User Guide, Renesas Electronics

[2] [AN-1089 I<sup>2</sup>C controlled window comparators.gp](#), GreenPAK Design File, Renesas Electronics

[3] [GreenPAK Development Tools](#), GreenPAK Development Tools Webpage, Renesas Electronics

[4] [Application Notes](#), GreenPAK Application Notes Webpage, Renesas Electronics

### 3. Introduction

The SLG46537 GreenPAK5 has an I<sup>2</sup>C communication interface for controlling its internal blocks configuration and some connections. It is highly flexible and easy to use. This example shows its use and configuration in the design of a dual window comparator.

### 4. Design overview

The design itself is a typical window comparator. 4 ACMPs are used to create 2 full window comparators inside the chip. The I<sup>2</sup>C interface is used to turn on ACMPs and change their Vref values.

The basic window comparator consists of 2 ACMPs and a 2-bit LUT connected to their outputs. Both ACMPs IN+ are connected to one source, their IN- sources are different Vref values. The LUT truth table is configured to produce a HIGH level when the input analog voltage is between ACMPs references and produce LOW in all other cases. All ACMPs could be dynamically turned on and off via their PWR UP nodes. In this design PWR Ups are connected via I<sup>2</sup>C virtual OUTs, so they can be controlled through I<sup>2</sup>C commands. IN- references of ACMP0-ACMP3 are configured as 100, 300, 600, 900 mV respectively. All IN+ inputs source from one pin. All output PINs are configured as Push Pull 1X (please refer to [Figure 1](#))

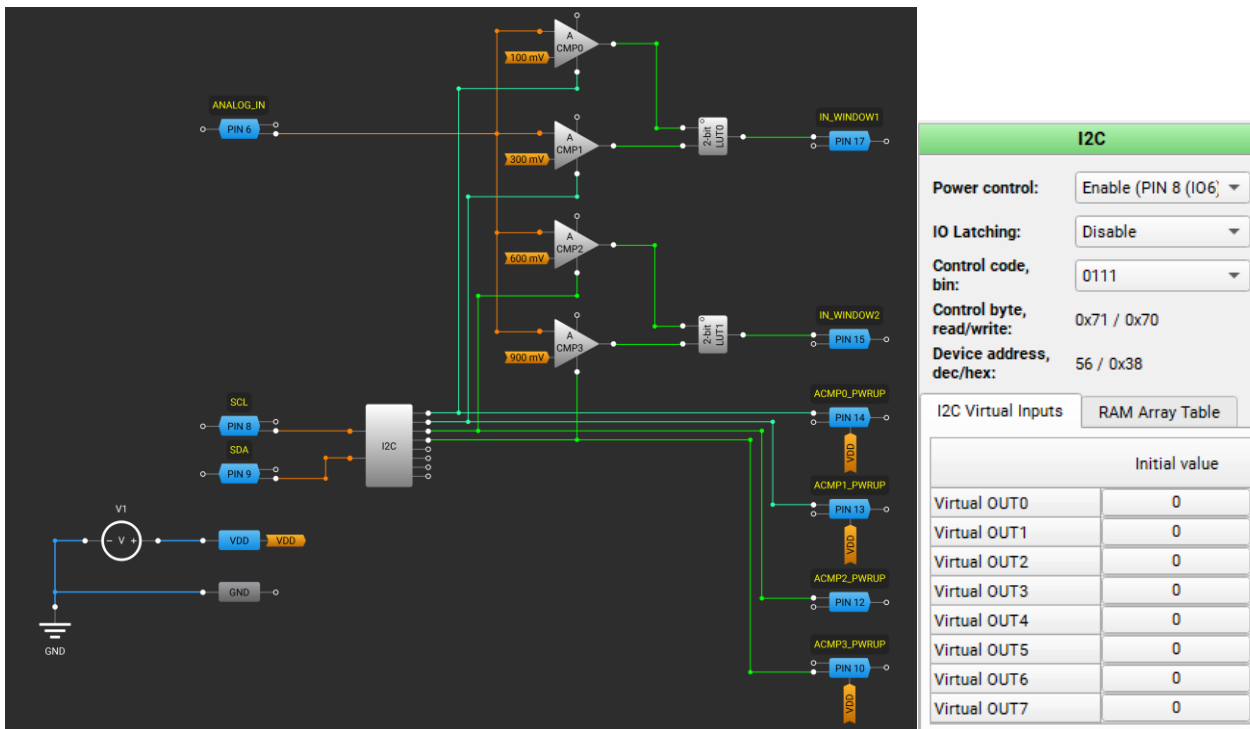


Figure 1. Dual window comparator design viewed in the GreenPAK Designer and I<sup>2</sup>C block configuration

### 5. I<sup>2</sup>C operation

ACMP Vrefs and PWR Ups are controlled via I<sup>2</sup>C protocol. It is a standard serial data transmission protocol. An example of correct chip and internal blocks addressing begins in [Figure 2](#). Certain pin assignments in the SLG46537 are reserved by default: SCL (serial clock) input is assigned to PIN8, while SDA (serial data) input is assigned to PIN9.

The address of Virtual OUTs is 244 (11110100). To switch a Virtual OUT HIGH, the corresponding bit should be sent into the GreenPAK.

During GreenPAK operation there is the possibility of changing some of the chip's blocks configurations. In this design, a reference voltage of ACMPs is changed by sending to respective ACMP address its configuration byte.

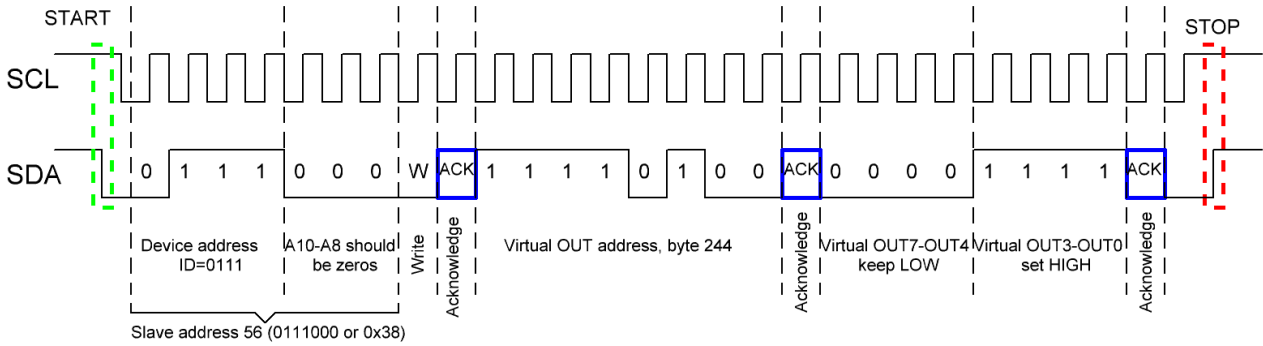


Figure 2. ACMPs powering up via I2C programming of Virtual OUTs. Timing Diagram

Typically, I2C slave device address consists of 7 bits. GreenPAK5 uses only the 4 MSB to control its device address, so 3 LSB (A10-A8) should be set to '000'. The device address ID is configured in the I2C block properties. In this case it is set to 0111, so the slave address is 56 (0111000 or 0x38). After the device address, the read/write bit follows. If it is LOW the data will be written to GreenPAK, if it is HIGH the data will be read from the GreenPAK.

Figure 3 shows the process of sequential configuration byte writing into GreenPAK. After the device address and read/write bit, ACMP0 is addressed (byte 203 or 11001011). The configuration byte follows next. It consists of Low Bandwidth Filter option bit (MSB), two Gain option bits and 5 Vref option bits (LSB). To have the next ACMP configured there is no need to send separate I2C code. The described code can be continued after ACK signal with 8 configuration bits.

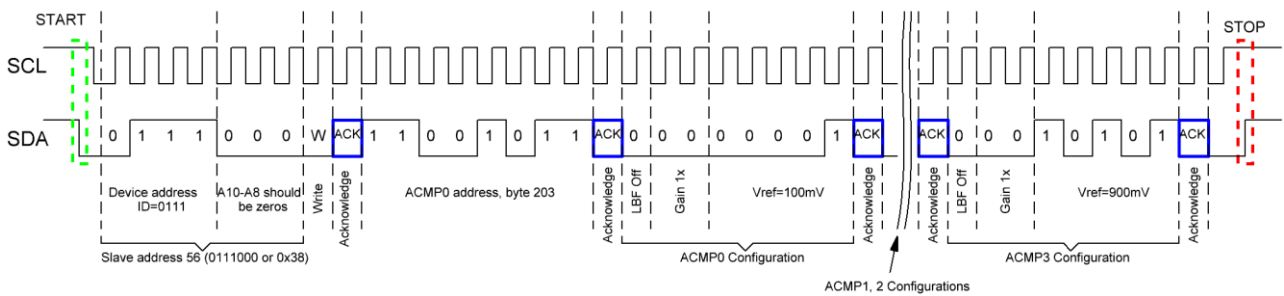


Figure 3. ACMPs Vref programming via I2C. Timing Diagram

## 6. Conclusion

This example describes the implementation of dynamic control and reconfiguration using I2C in GreenPAK5. Dynamic access to these and other blocks within the GreenPAK programmable mixed-signal ASIC afford the designer great flexibility.

## 7. Revision History

Revision	Date	Description
1.00	Nov 27, 2015	Initial release.
2.00	Apr 7, 2026	The part number has been changed from SLG46531V to SLG46537V.

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