

Introduction

It is often necessary to divide a signal frequency by a fixed coefficient, which is simple if this coefficient is an even number equal to 2, 4, 8 and so on. However, dividing by odd or fractional coefficients is a more complicated task. Using the LUTs and DFFs resources in GreenPAK, one can efficiently divide a given frequency by 1.5, 2.5, 3, 3.5, 4.5, 5, and many other coefficients.

Frequency divide by 1.5, 3, 3.5

Here DFFs each provide frequency division by 2, while XOR LUTs are used to eliminate the odd half input clock which comes to the first DFF. This makes it possible to get coefficients $2-0.5=1.5$; $1.5*2=3$; $4-0.5=3.5$.

Blocks configurations are shown in figures 1-5 below.

2-bit LUT4				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0

2-bit LUT5				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0

Figure 2. LUTs properties

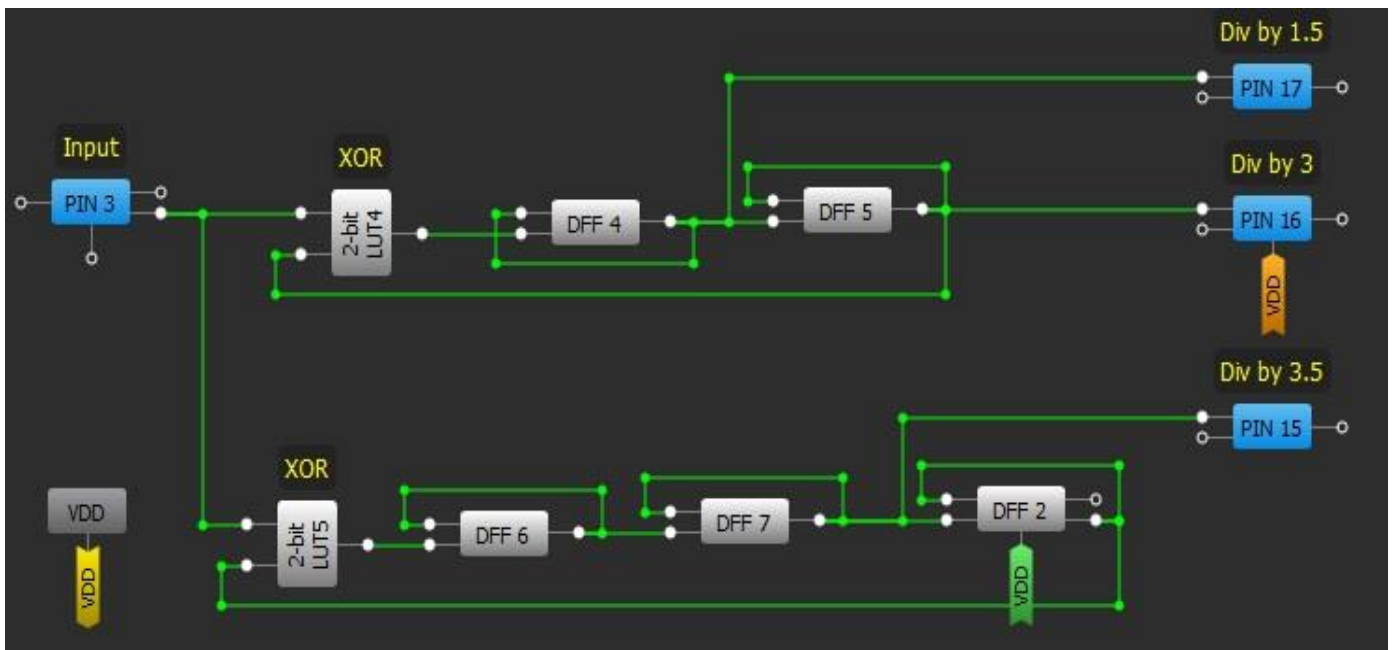


Figure 1. Frequency divide by 1.5, 3, 3.5 circuit design

PIN 3	
I/O selection:	Digital input
Input mode: OE = 0	Digital in without Sc
Output mode: OE = 1	None
Resistor:	Floating
Resistor value:	Floating
PIN 15	
I/O selection:	Digital output
Input mode: OE = 0	None
Output mode: OE = 1	1x push pull
Resistor:	Floating
Resistor value:	Floating
PIN 16	
I/O selection:	Digital output
Input mode: OE = 0	None
Output mode: OE = 1	1x push pull
Resistor:	Floating
Resistor value:	Floating
PIN 17	
I/O selection:	Digital output
Input mode: OE = 0	None
Output mode: OE = 1	1x push pull
Resistor:	Floating
Resistor value:	Floating

Figure 3. Pins properties

2-bit LUT0/DFF/LATCH4	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	None
Initial polarity:	Low
Q output polarity:	Inverted (nQ)
2-bit LUT1/DFF/LATCH5	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	None
Initial polarity:	Low
Q output polarity:	Inverted (nQ)
2-bit LUT2/DFF/LATCH6	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	None
Initial polarity:	Low
Q output polarity:	Inverted (nQ)
2-bit LUT3/DFF/LATCH7	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	None
Initial polarity:	Low
Q output polarity:	Inverted (nQ)
3-bit LUT2/DFF/LATCH2	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	nRESET
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

Figure 4. DFFs properties

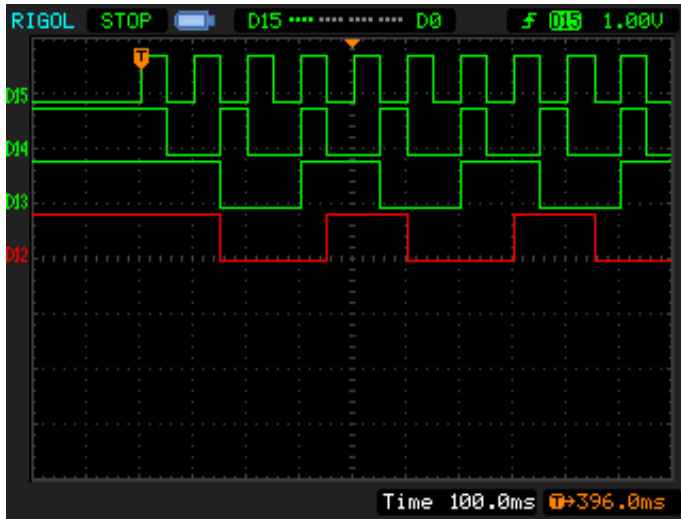


Figure 5. Frequency divider functional diagram
(D15 – Input signal; D14 – F/1.5;
D13 – F/3; D12 – F/3.5)

PIN 2	
I/O selection:	Digital input
Input mode: OE = 0	Digital in without Sc
Output mode: OE = 1	None
Resistor:	Floating
Resistor value:	Floating
PIN 14	
I/O selection:	Digital output
Input mode: OE = 0	None
Output mode: OE = 1	1x push pull
Resistor:	Floating
Resistor value:	Floating
PIN 16	
I/O selection:	Digital output
Input mode: OE = 0	None
Output mode: OE = 1	1x push pull
Resistor:	Floating
Resistor value:	Floating

Figure 7. Pins properties

Frequency divide by 2.5, 5

This case operates differently than the previous 1.5, 3, 3.5 example. Here, the same CLK signal is supplied to a string of DFF CK inputs, but LUTs and feedback reconfigure their D inputs. In this way frequency division by 2.5 can be designed. DFF3 is used to divide by 2 a previously divided by 2.5 frequency and output the divide by 5 signal.

Blocks configurations are shown in figures 6-9.

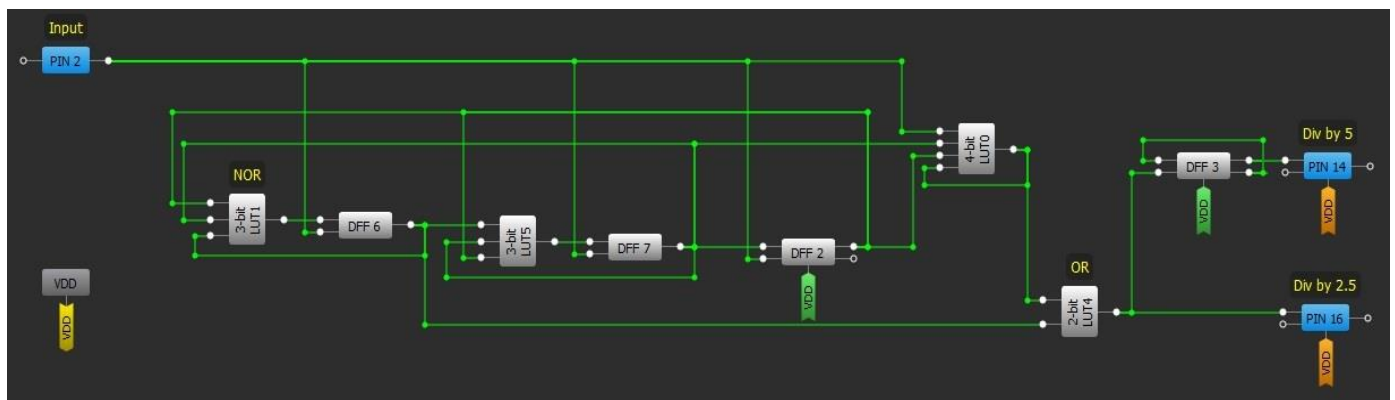


Figure 6. Frequency divider by 2.5; 5 circuit design

3-bit LUT1				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

3-bit LUT5				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0

2-bit LUT4				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1

4-bit LUT0/CNT2/DLY2				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Type:

Figure 8. LUTs properties

2-bit LUT2/DFF/LATCH6	
Type:	<input type="text" value="DFF / LATCH"/>
Mode:	<input type="text" value="DFF"/>
nSET/nRESET option:	<input type="text" value="None"/>
Initial polarity:	<input type="text" value="Low"/>
Q output polarity:	<input type="text" value="Non-inverted (Q)"/>

2-bit LUT3/DFF/LATCH7	
Type:	<input type="text" value="DFF / LATCH"/>
Mode:	<input type="text" value="DFF"/>
nSET/nRESET option:	<input type="text" value="None"/>
Initial polarity:	<input type="text" value="Low"/>
Q output polarity:	<input type="text" value="Non-inverted (Q)"/>

3-bit LUT2/DFF/LATCH2	
Type:	<input type="text" value="DFF / LATCH"/>
Mode:	<input type="text" value="DFF"/>
nSET/nRESET option:	<input type="text" value="nRESET"/>
Initial polarity:	<input type="text" value="Low"/>
Q output polarity:	<input type="text" value="Non-inverted (Q)"/>

3-bit LUT3/DFF/LATCH3	
Type:	<input type="text" value="DFF / LATCH"/>
Mode:	<input type="text" value="DFF"/>
nSET/nRESET option:	<input type="text" value="nRESET"/>
Initial polarity:	<input type="text" value="Low"/>
Q output polarity:	<input type="text" value="Non-inverted (Q)"/>

Figure 9. DFFs properties

By taking a signal from the other DFFs outputs it is possible to get a divide by 5 signal as well, but with different duty cycle (not 50%, as previously) and phase shift (see figure 10): D3 – DFF2, D4 – DFF7, D5 – DFF6.

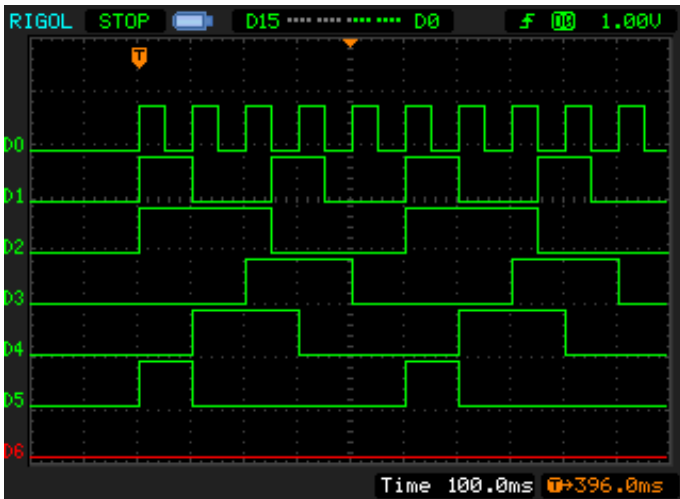


Figure 10. Frequency divider functional diagram (D0 – Input signal; D1 – F/2.5; D2, D3, D4, D5 – F/5)

Frequency divide by 4.5

Frequency division by 4.5 circuit is based on the previous circuit (divider by 5).

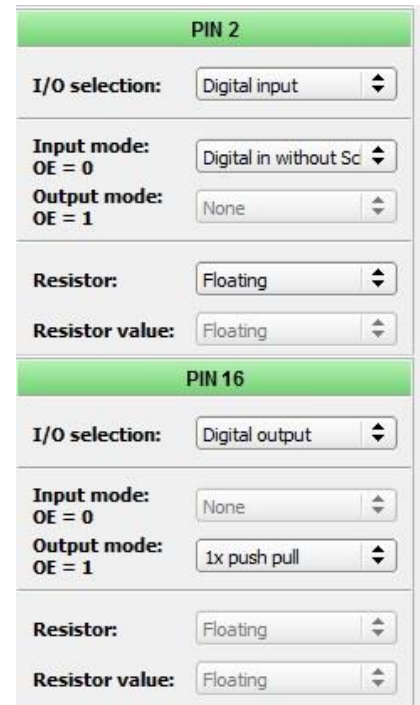


Figure 12. Pins properties

There are some additional blocks (DFF4 and 2-bit LUT5) which provide elimination of half clock period for DFFs (as in the divide by 1.5, 3, 3.5 circuit). This allows us to get divide by 4.5.

Blocks configurations are shown in figures 11-14.

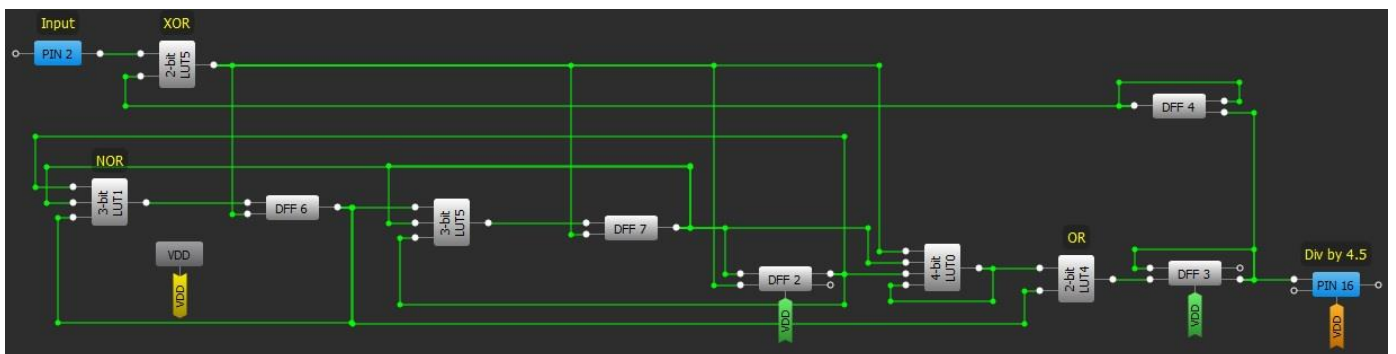


Figure 11. Frequency divide by 4.5 circuit design

2-bit LUT5				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0

3-bit LUT1				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

3-bit LUT5				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0

4-bit LUT0/CNT2/DLY2				
Type: LUT				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

2-bit LUT4				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0

Figure 13. LUTs properties

2-bit LUT2/DFF/LATCH6	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	None
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

2-bit LUT3/DFF/LATCH7	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	None
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

3-bit LUT2/DFF/LATCH2	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	nRESET
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

3-bit LUT3/DFF/LATCH3	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	nRESET
Initial polarity:	Low
Q output polarity:	Non-inverted (Q)

2-bit LUT0/DFF/LATCH4	
Type:	DFF / LATCH
Mode:	DFF
nSET/nRESET option:	None
Initial polarity:	Low
Q output polarity:	Inverted (nQ)

Figure 14. DFFs properties

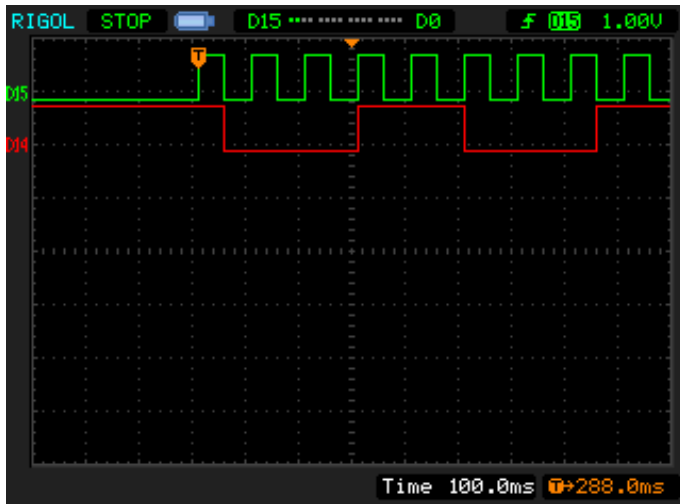


Figure 15. Frequency divider functional waveforms

(D15 – Input signal; D14 – $F/4.5$)

Conclusion

Frequency dividers which are typically not simple to realize can be constructed using LUTs and DFFs.

As was shown, it is possible to divide a frequency by 1.5, 2.5, 3, 3.5, 4.5, 5. Such circuits may be used as a single device or as a part of a larger circuit.

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