# **inter<sub>sil</sub>**"

## HS-26CT32RH-T

### Radiation HardenedQuad Differential Line Receiver

Intersil's Satellite Applications Flow<sup>™</sup> (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HS-26CT32RH-T is a Quad Differential Line Receiver designed for digital data transmission over balanced lines and meets the requirements of EIA Standard RS-422. Radiation Hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CT32RH-T has an input sensitivity of 200mV (typ.) over the common mode input voltage range of  $\pm$ 7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. TTL compatible Enable and Disable functions are common to all four receivers.

### Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-26CT32RH-T are contained in SMD 5962-95631. A "hot-link" is provided from our website for downloading.

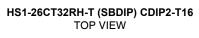
Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

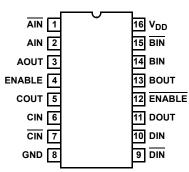
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose .....1 x 10<sup>5</sup> RAD(Si)
  - SEU and SEL ..... Immune to 100MeV/mg/cm<sup>2</sup>
- EIA RS-422 Compatible Inputs
- TTL Compatible Enable Inputs
- Input Fail Safe Circuitry
- High Impedance Inputs when Disabled or Powered Down
- Low Power Dissipation 138mW Standby (Max)
- Single 5V Supply
- Full -55°C to 125°C Military Temperature Range

#### Pinouts

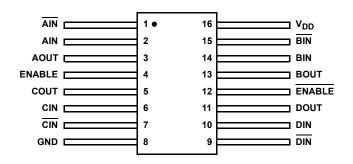
# DATASHEET

FN4593 Rev 1.00 July 1999



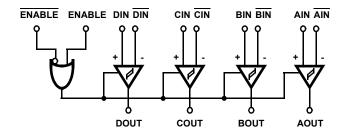


#### HS9-26CT32RH-T (FLATPACK), CDFP4-F16 TOP VIEW



# **intersi**["

#### Functional Diagram



| трити | TABLE |
|-------|-------|
| IKUIN | IADLE |

| DEVICE POWER<br>ON/OFF | INPUTS |        |                       | OUTPUT |
|------------------------|--------|--------|-----------------------|--------|
|                        | ENABLE | ENABLE | INPUT                 | OUT    |
| ON                     | 0      | 1      | Х                     | HI-Z   |
| ON                     | 1      | Х      | $VID \ge VTH \ (Max)$ | 1      |
| ON                     | 1      | Х      | $VID \leq VTH$ (Min)  | 0      |
| ON                     | Х      | 0      | $VID \ge VTH\;(Max)$  | 1      |
| ON                     | Х      | 0      | $VID \le VTH$ (Min)   | 0      |
| ON                     | 1      | Х      | Open                  | 1      |
| ON                     | х      | 0      | Open                  | 1      |

© Copyright Intersil Americas LLC 2002. All Rights Reserved. All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at <a href="http://www.intersil.com/en/support/qualandreliability.html">www.intersil.com/en/support/qualandreliability.html</a>

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com



#### **Die Characteristics**

#### DIE DIMENSIONS:

2140µm x 3290µm x 533µm ±25.4µm (85 x 130 x 21mils ±1mil)

#### **METALLIZATION:**

M1: Mo/Tiw Thickness: 5800Å M2: Al/Si/Cu Thickness: 10kÅ ±1kÅ

#### SUBSTRATE POTENTIAL:

Internally connected to  $V_{\mbox{\scriptsize DD}}.$  May be left floating.

#### BACKSIDE FINISH:

Silicon

#### PASSIVATION:

Type: SiO<sub>2</sub> Thickness: 8kÅ ±1kÅ

#### WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm<sup>2</sup>

#### TRANSISTOR COUNT:

315

#### PROCESS:

Radiation Hardened CMOS, AVLSI

#### Metallization Mask Layout

#### HS-26CT32RH-T

