

Applying Power MOSFET Drivers

The EL7xxx series of high speed power MOSFET drivers achieve noteworthy improvements in speed, efficiency, input impedance, and functionality thru the application of advanced CMOS technology and novel circuit design. However, their ability to deliver high peak currents with rapid  $dV/dT$ 's makes them susceptible to over stress. Recommended design practices will be discussed to assist the designer in achieving reliable operation.

**Common Causes Resulting in MOSFET Driver Problems**

**Cause 1**

CMOS Latch-up: Inherent to CMOS integrated circuitry, is a parasitic SCR which can be triggered by injecting current thru any input or output pad. This occurs whenever the input/output pins exceed the supply rails by more than 0.6V. This condition may exist for any one of the following reasons.

1. During the power up/power down sequence, when voltage is applied to an input without supply voltage.
2. Ground or  $V_{DD}$  "bounce" (relative to the input) during switching. This is often attributed to inductance in the current path.
3. Inductive kick-back from the output load.

**Cause 2**

Over-Voltage Spikes: Power line spikes will occur when a rapid change in current (typical during switching) is present on an inductive supply line. Exceeding the maximum supply voltage can rupture the internal transistor gate oxide, causing catastrophic failure.

**Cause 3**

Insufficient Overdrive: During switching, some ground bounce is going to occur. If the ground bounce is greater than the overdrive to the input, oscillation may result as the effective drive to the input is modulated. Since the typical input delay is only 20ns, a slowly rising drive waveform will still be very close to the threshold when the output switches. The ensuing ground bounce may be enough to toggle the input.

**Cause 4**

Thermal Overload: The high peak drive capability of the Elantec power MOSFET drivers, far exceeds their continuous rating. Limited by the high thermal resistance associated with PDIP and SOIC packages, junction temperatures can exceed the 125°C rated maximum. Users should be aware of those factors which contribute to the total power dissipated, including quiescent current, conduction losses, and switching losses.

**Guidelines for Improved Operation**

The most important thing to remember in applying CMOS drivers is to minimize inductance to the power pins as illustrated in Figure 1.

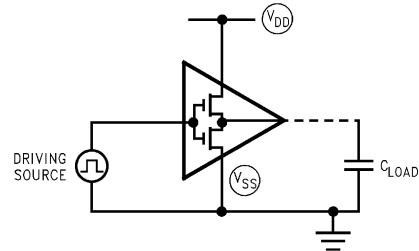


FIGURE 1. TROUBLE PRONE CONFIGURATION

To prevent CMOS latch-up restrict the inputs/outputs from exceeding the power rails. This may require the use of clamping diodes, output snubbers, power supply bypassing and decoupling. Effective bypassing requires a minimum path length between capacitor and supply pins. Choose a capacitor with good high frequency characteristics, such as ceramic and/or tantalum construction. Refer to Figure 2.

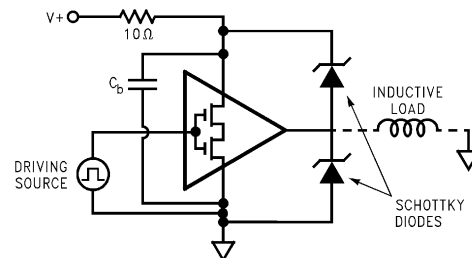
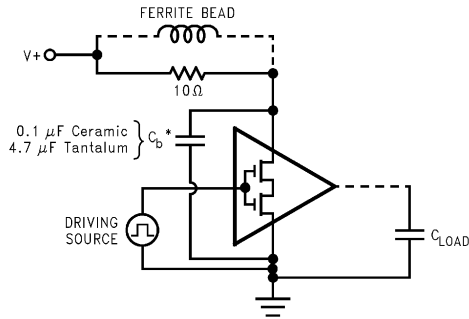


FIGURE 2. SUGGESTED CONFIGURATION FOR DRIVING INDUCTIVE LOADS

Overvoltage spikes can be controlled with decoupling. A small resistor (10Ω) from the supply, or a ferrite bead, followed by a 4.7μF tantalum capacitor with short leads to the power pins is very effective. The suggested configuration is shown in Figure 3.



\*C<sub>b</sub> should be physically located close to the power pins.

FIGURE 3. SUGGESTED DECOUPLING/BYPASSING

Sensitivity to insufficient drive is most pronounced at supply voltages greater than 12V due to the higher internal peak currents. Where high supply voltage operation is required, 0V to 5V input drive is suggested, with a minimum rise/fall time of 200ns.

Excessive power dissipation typically results when driving large capacitive loads at high frequencies. These losses are described by:

$$P = CV^2F \text{ where}$$

P = Power

C = Capacitance (Internal and External)

V = Supply Voltage

F = Clock Frequency

Internal dissipation can be reduced by adding an external resistor or inductor, as shown in Figure 4. Also, since the power varies as the square of the voltage, a reduction in supply voltage from 15V to 12V results in a 33% power savings.

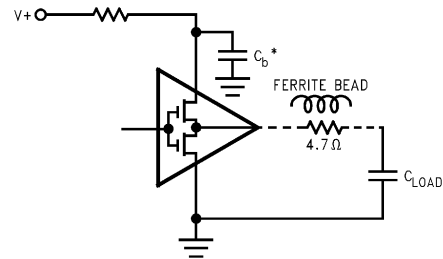


FIGURE 4. REDUCING CV<sup>2</sup>F LOSSES

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