

## Product Change Notice (PCN)

**Subject:** Datasheet change for the Listed ISL80111\*, ISL80112\* and ISL80113\* Intersil Products

**Publication Date:** 9/30/2016

**Effective Date:** 9/30/2016

### Revision Description:

Initial Release

### Description of Change:

This notice is to inform you that Intersil has updated the electrical specifications on the “Recommended Operating Conditions”, DC Input and Bias Line Regulation and DC Output Load Regulation limits for the products listed below:

ISL80111IRAJZ	ISL80112IRAJZ	ISL80113IRAJZ
ISL80111IRAJZ-T	ISL80112IRAJZ-T	ISL80113IRAJZ-T
ISL80111IRAJZ-T7A	ISL80112IRAJZ-T7A	ISL80113IRAJZ-T7A

### Reason for Change:

The change aligns the data sheet with the product characteristics and is necessary to maintain product manufacturability in support of customer delivery requirements. Details regarding the change are contained on the following page. The updated data sheet is available on the Intersil web site at:

<http://www.intersil.com/content/dam/Intersil/documents/isl8/isl80111-12-13.pdf>

### Impact on fit, form, function, quality & reliability:

The change will have no impact on the form, fit, function, quality, reliability and environmental compliance of the devices.

### Product Identification:

There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts. Product affected by this change is identifiable via Intersil’s internal traceability system.

**Qualification status:** Not applicable

**Sample availability:** 9/30/2016

**Device material declaration:** Available upon request

*Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.*

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: <a href="mailto:PCN-US@INTERSIL.COM">PCN-US@INTERSIL.COM</a>	Europe: <a href="mailto:PCN-EU@INTERSIL.COM">PCN-EU@INTERSIL.COM</a>	Japan: <a href="mailto:PCN-JP@INTERSIL.COM">PCN-JP@INTERSIL.COM</a>	Asia Pac: <a href="mailto:PCN-APAC@INTERSIL.COM">PCN-APAC@INTERSIL.COM</a>

**From:**

**Recommended Operating Conditions** (Notes 4, 6)

Junction Temperature Range . . . . . -40 °C to +125 °C  
 VIN Relative to GND (ISL80113) (Note 9) . . . . . VOUT + 0.4V to 5V  
 VIN Relative to GND (ISL80112) (Note 9) . . . . . VOUT + 0.3V to 5V  
 VIN Relative to GND (ISL80111) (Note 9) . . . . . VOUT + 0.2V to 5V  
 Nominal VOUT Range . . . . . 800mV to 3.3V  
 PG, ENABLE, SENSE/ADJ, SS Relative to GND . . . . . 0V to 5.5V  
 VBIAS Relative to GND . . . . . 0V to 5.5V  
 VBIAS Relative to VOUT . . . . . +0.8V minimum

**To:**

**Recommended Operating Conditions** (Notes 4)

Junction Temperature Range . . . . . -40 °C to +125 °C  
 VIN Relative to GND (ISL80113) (Note 8) . . . . . VOUT + 0.30V to 3.6V  
 VIN Relative to GND (ISL80112) (Note 8) . . . . . VOUT + 0.25V to 3.6V  
 VIN Relative to GND (ISL80111) (Note 8) . . . . . VOUT + 0.20V to 3.6V  
 Nominal VOUT Range . . . . . 800mV to 3.3V  
 PG, ENABLE, ADJ, SS Relative to GND . . . . . 0V to 5.5V  
 VBIAS Relative to GND . . . . . 0V to 5.5V

**From:**

**Electrical Specifications** Unless otherwise specified, VIN = VOUT + 0.4V, VBIAS = 2.9V, VOUT = 1.2V, CBIAS = 1μF, CIN = 10μF, COUT = 2.2μF, TJ = +25 °C, IL = 0mA. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to "Power Dissipation" on page 13 and Tech Brief TB379. Boldface limits apply over junction temperature (Tj) range, -40 °C to +125 °C. Pulse load techniques used by ATE to ensure TJ = TA where datasheet limits are defined.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
<b>DC CHARACTERISTICS</b>						
VBIAS UVLO	UVLO_BIAS_r	VBIAS Rising		2.3	<b>2.9</b>	V
	UVLO_BIAS_f	VBIAS Falling	<b>1.55</b>	2.1	<b>2.8</b>	V
VBIAS UVLO Hysteresis	UVLO_B_HYS			0.2		V
DC ADJ Pin Voltage Accuracy	VADJ	1.0V ≤ VIN ≤ 3.6V, ILOAD = 0A, 2.9V ≤ VBIAS ≤ 5.5V, VOUT = VADJ	<b>494</b>	502	<b>510</b>	mV
<b>DC Input Line Regulation</b>	ΔVOUT	VOUT + 0.4V ≤ VIN ≤ 3.6V		<b>0.01</b>	<b>0.9</b>	mV
<b>DC Bias Line Regulation</b>	ΔVOUT	2.9V < VBIAS < 5.5V with respect to ADJ pin		<b>0.3</b>	<b>1.4</b>	mV
<b>DC Output Load Regulation</b>	ΔVOUT	0A ≤ ILOAD ≤ 3A	<b>-2</b>	<b>-0.2</b>	<b>2</b>	mV
Feedback Input Current		VADJ = 0.5V		10	<b>80</b>	nA
VIN Quiescent Current	IQ (VIN)	VOUT = 2.5V		8	<b>10</b>	mA
VIN Quiescent Current	IQ (VIN)	VOUT = <b>3.3</b>		10.6		mA

**To:**

**Electrical Specifications** Unless otherwise specified, VIN = 3V, VBIAS = 5.5V, VOUT = 0.5V, TJ = +25 °C, IL = 0mA. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to "Power Dissipation" on page 13 and Tech Brief TB379. Boldface limits apply across junction temperature (Tj) range, -40 °C to +125 °C. Pulse load techniques used by ATE to ensure TJ = TA where datasheet limits are defined.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
<b>DC CHARACTERISTICS</b>						
VBIAS UVLO	UVLO_BIAS_r	VBIAS Rising		2.3	<b>2.9</b>	V
	UVLO_BIAS_f	VBIAS Falling	<b>1.55</b>	2.1	<b>2.8</b>	V
VBIAS UVLO Hysteresis	UVLO_B_HYS			0.2		V
DC ADJ Pin Voltage Accuracy	VADJ	1.0V ≤ VIN ≤ 3.6V, ILOAD = 0A, 2.9V ≤ VBIAS ≤ 5.5V, VOUT = VADJ	<b>494</b>	502	<b>510</b>	mV
<b>DC Input Line Regulation</b>	(VOUT low line - VOUT high line) / VOUT low line	2.9V ≤ VIN ≤ 3.6V, VOUT = 2.5V	<b>-0.18</b>	0.02	<b>0.18</b>	%
<b>DC Bias Line Regulation</b>	(VOUT low line - VOUT high line) / VOUT low line	4.5V < VBIAS < 5.5V, VOUT = 2.5V	<b>-0.28</b>	0.06	<b>0.28</b>	%
<b>DC Output Load Regulation</b>	(VOUT no load - VOUT high load) / VOUT no load	0A < ILOAD < Full Load, VOUT = 2.5V	<b>-0.40</b>	0.04	<b>0.40</b>	%
Feedback Input Current		VADJ = 0.5V		10	<b>80</b>	nA
VIN Quiescent Current	IQ (VIN)	VOUT = 2.5V		8	<b>10</b>	mA
VIN Quiescent Current	IQ (VIN)	VOUT = <b>3.3V</b> , VIN = 3.6V, VBIAS = 5V		10.6		mA