

HS-0546RH, HS-0547RH

Radiation Hardened Single 16/Differential 8 Channel CMOS Analog Multiplexers
with Active Overvoltage Protection

FN3544
Rev.4.00
March 13, 2006

The HS-0546RH and HS-0547RH are radiation hardened analog multiplexers with Active Overvoltage Protection and guaranteed r_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70V peak-to-peak levels with $\pm 15V$ supplies and digital inputs will sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur: each input presents $1k\Omega$ of resistance under this condition. These features make the HS-0546RH and HS-0547RH ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44V dielectrically isolated CMOS technology. The HS-0546 is a 16 channel device and the HS-0547 is an 8 channel differential version. If input overvoltage protection is not needed, the HS-0506 and HS-0507 multiplexers are recommended.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95693. A "hot-link" is provided on our homepage for downloading.
<http://www.intersil.com>

Features

- Electrically Screened to SMD # 5962-95693
- QML Qualified per MIL-PRF-38535 Requirements
- Gamma Dose 1×10^4 RAD(Si)
- No Latch-Up
- No Channel Interaction During Overvoltage
- Guaranteed r_{ON} Matching
- Maximum Power Supply 44V
- Break-Before-Make Switch
- Analog Signal Range. $\pm 15V$
- Access Time. $1.0\mu s$

Applications

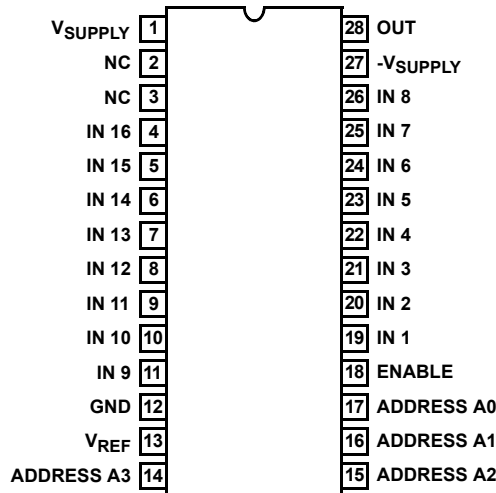
- Data Acquisition Systems
- Control Systems
- Telemetry

Ordering Information

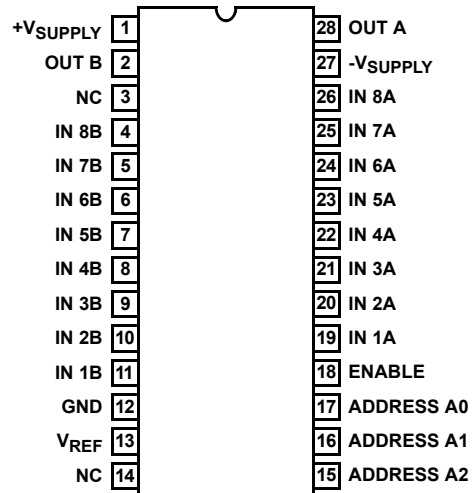
| ORDERING NUMBER | INTERNAL MKT. NUMBER | PART MARKING | TEMP. RANGE (°C) |
|-----------------|----------------------|-------------------|------------------|
| 5962D9569301V9A | HS0-0546RH-Q | Q-5962D9569301V9A | 25 |
| 5962D9569301VXC | HS1B-0546RH-Q | Q-5962D9569301VXC | -55 to 125 |
| 5962D9569302V9A | HS0-0547RH-Q | Q-5962D9569302V9A | 25 |
| 5962D9569302VXC | HS1B-0547RH-Q | Q-5962D9569302VXC | -55 to 125 |

Pinouts

HS-0546RH GDIP1-T28 (CERDIP) OR CDIP2-T28 (SBDIP)
TOP VIEW

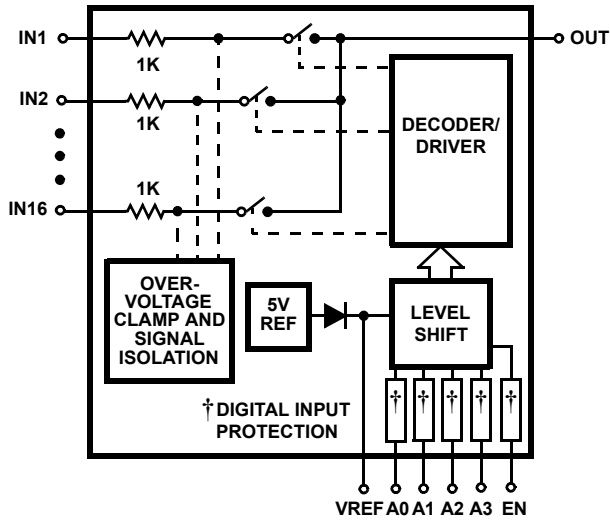


HS-0547RH GDIP1-T28 (CERDIP) OR CDIP2-T28 (SBDIP)
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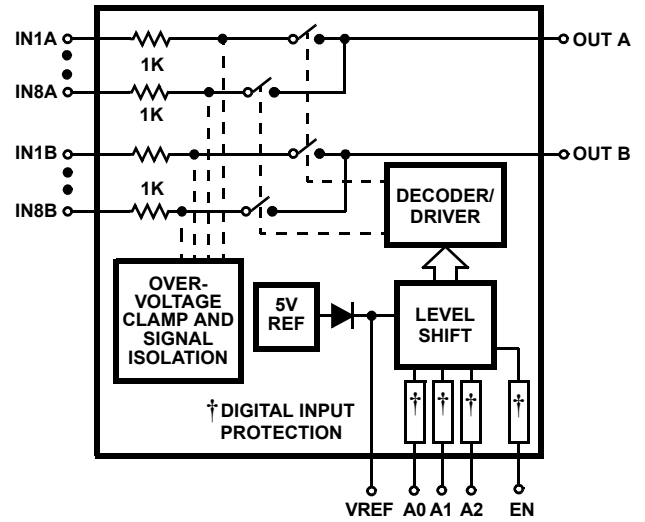


Functional Diagrams

HS-0546RH



HS-0547RH



HS-0546RH TRUTH TABLE

| A3 | A2 | A1 | A0 | EN | "ON" CHANNEL |
|----|----|----|----|----|--------------|
| X | X | X | X | L | NONE |
| L | L | L | L | H | 1 |
| L | L | L | H | H | 2 |
| L | L | H | L | H | 3 |
| L | L | H | H | H | 4 |
| L | H | L | L | H | 5 |
| L | H | L | H | H | 6 |
| L | H | H | L | H | 7 |
| L | H | H | H | H | 8 |
| H | L | L | L | H | 9 |
| H | L | L | H | H | 10 |
| H | L | H | L | H | 11 |
| H | L | H | H | H | 12 |
| H | H | L | L | H | 13 |
| H | H | L | H | H | 14 |
| H | H | H | L | H | 15 |
| H | H | H | H | H | 16 |

HS-0547RH TRUTH TABLE

| A2 | A1 | A0 | EN | "ON" CHANNEL PAIR |
|----|----|----|----|-------------------|
| X | X | X | L | NONE |
| L | L | L | H | 1 |
| L | L | H | H | 2 |
| L | H | L | H | 3 |
| L | H | H | H | 4 |
| H | L | L | H | 5 |
| H | L | H | H | 6 |
| H | H | L | H | 7 |
| H | H | H | H | 8 |

Switching Waveforms

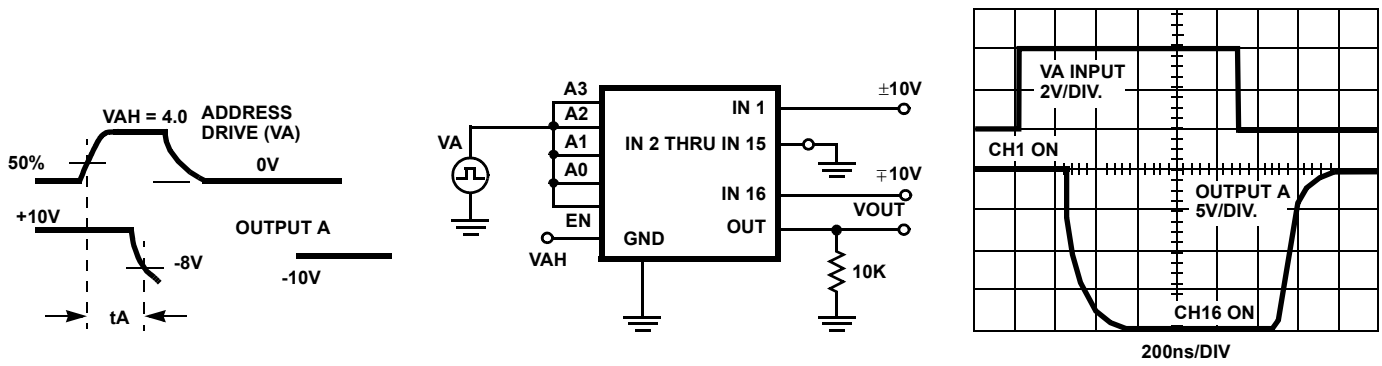


FIGURE 1. ACCESS TIME

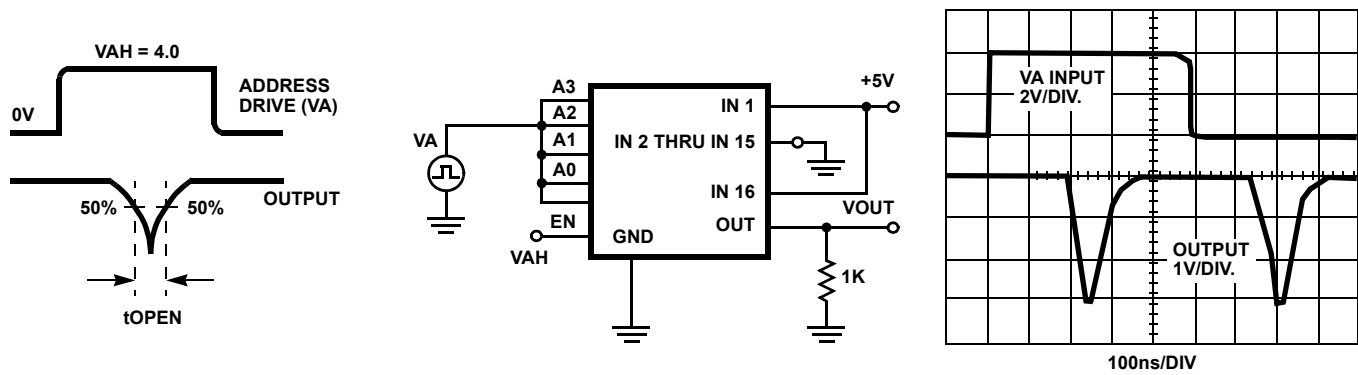


FIGURE 2. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

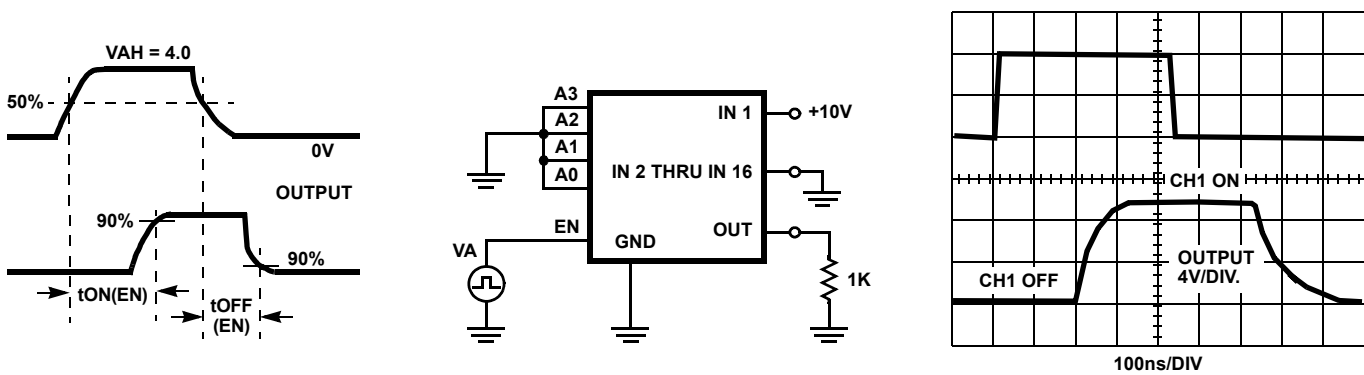


FIGURE 3. ENABLE DELAY $t_{ON}(EN)$, $t_{OFF}(EN)$

Schematic Diagrams

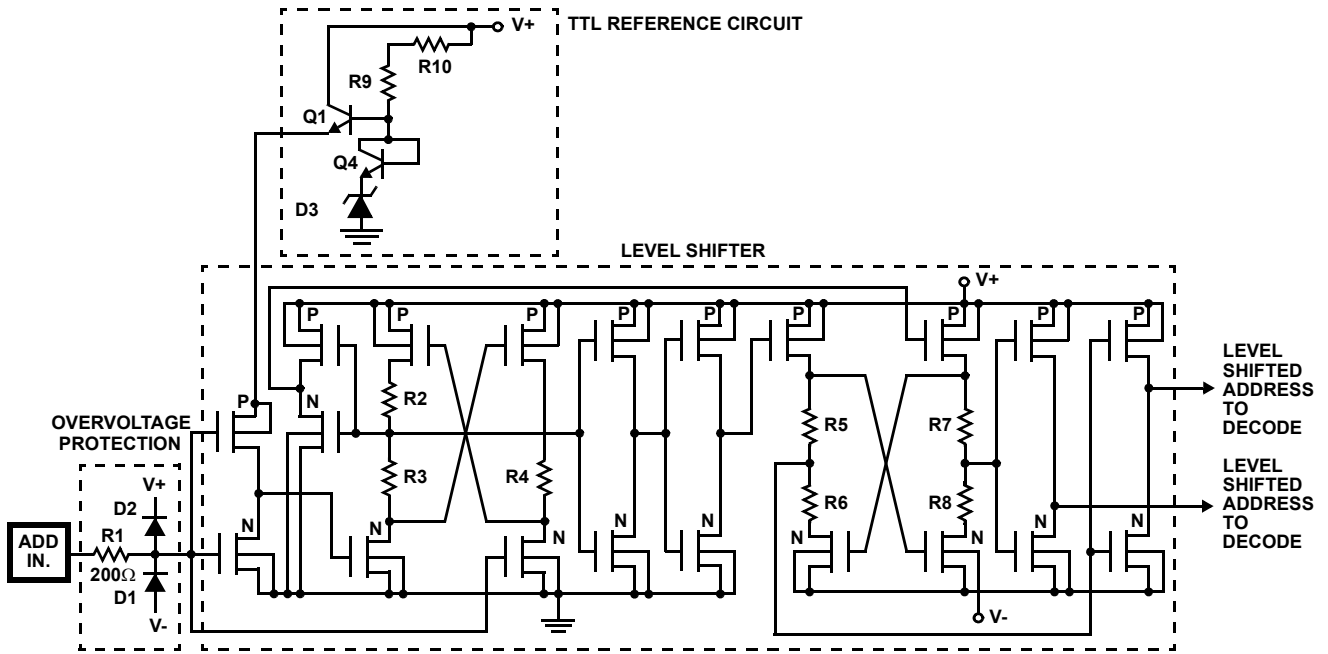


FIGURE 4. ADDRESS INPUT BUFFER AND LEVEL SHIFTER

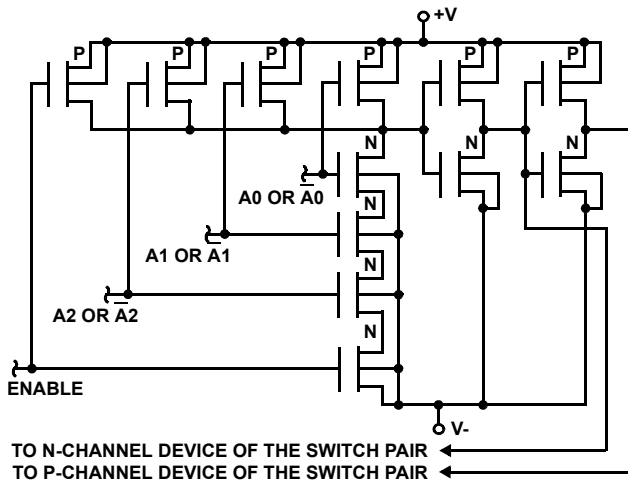


FIGURE 5. ADDRESS DECODER

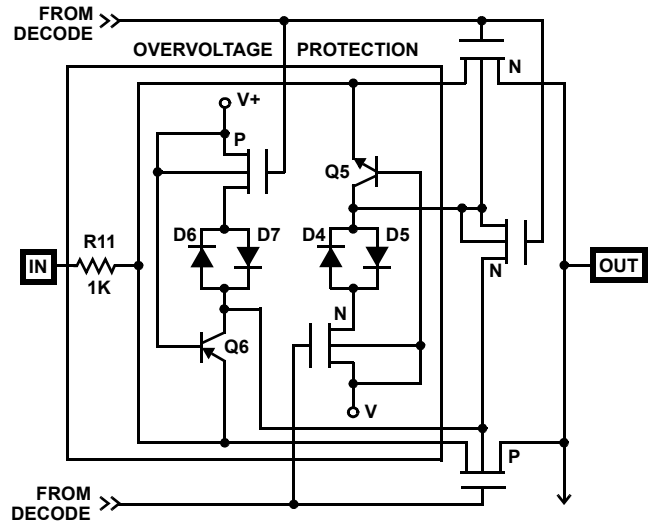
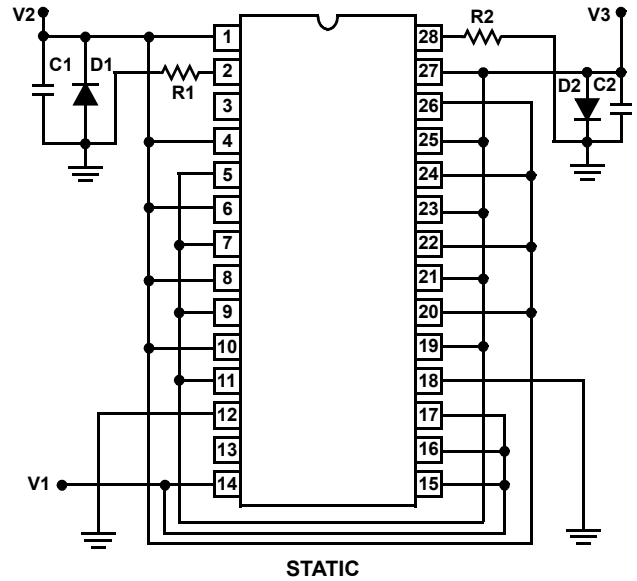
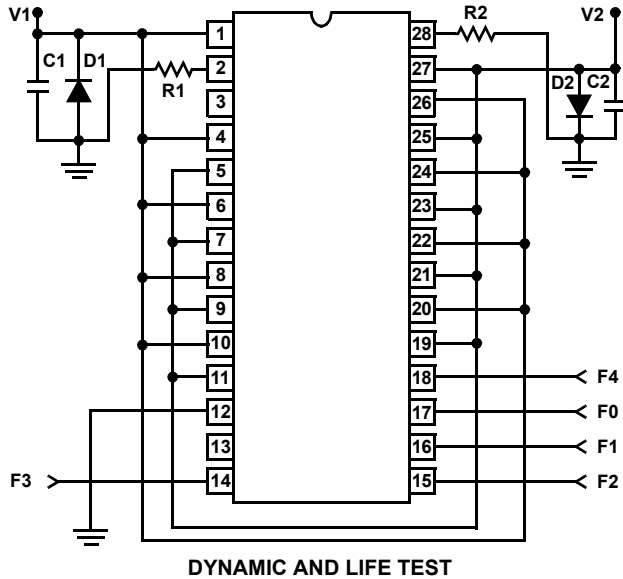


FIGURE 6. MULTIPLEX SWITCH

Burn-In/Life Test Circuits



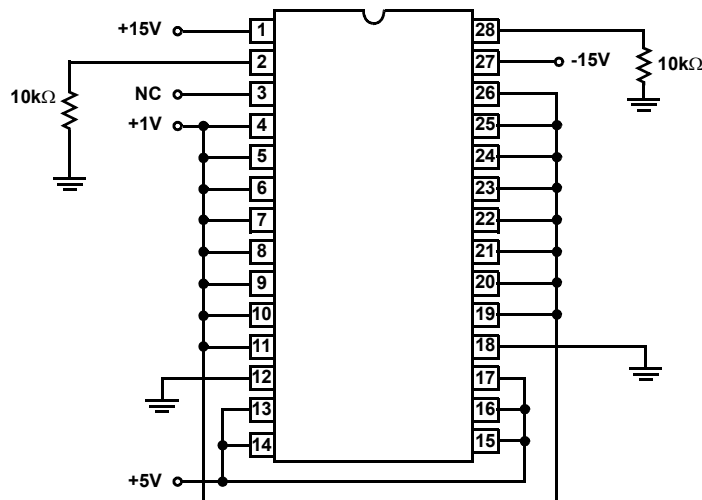
NOTES:

1. The Dynamic Test Circuit is utilized for all life testing.
2. V1 = +15V minimum, +16V maximum.
3. V2 = -15V maximum, -16V minimum.
4. R1, R2 = 10kΩ, ±5%, 1/4 or 1/2W (per socket).
5. C1, C2 = 0.01μF minimum (per socket) or 0.1μF minimum (per row).
6. D1, D2 = 1N4002 or equivalent (per board).
7. F0 = 100kHz, 10%; F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2
40% - 60% duty cycle; VIL = 0.8V maximum;
VIH = 4.0V minimum.

NOTES:

8. V1 = +5V minimum, +6V maximum.
9. V2 = +15V minimum, +16V maximum.
10. V3 = -15V maximum, -16V minimum.
11. R1, R2 = 10kΩ, ±5%, 1/4 or 1/2W (per socket).
12. C1, C2 = 0.01μF minimum (per socket) or 0.1μF minimum (per row).
13. D1, D2 = 1N4002 or equivalent (per board).

Irradiation Circuit



Die Characteristics

DIE DIMENSIONS:

83.9 mils x 159 mils x 19 mils

INTERFACE MATERIALS:

Glassivation:

Type: Nitride
 Thickness: $7k\text{\AA} \pm 0.7k\text{\AA}$

Top Metallization:

Type: Al
 Thickness: $16k\text{\AA} \pm 2k\text{\AA}$

Substrate:

CMOS, DI

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

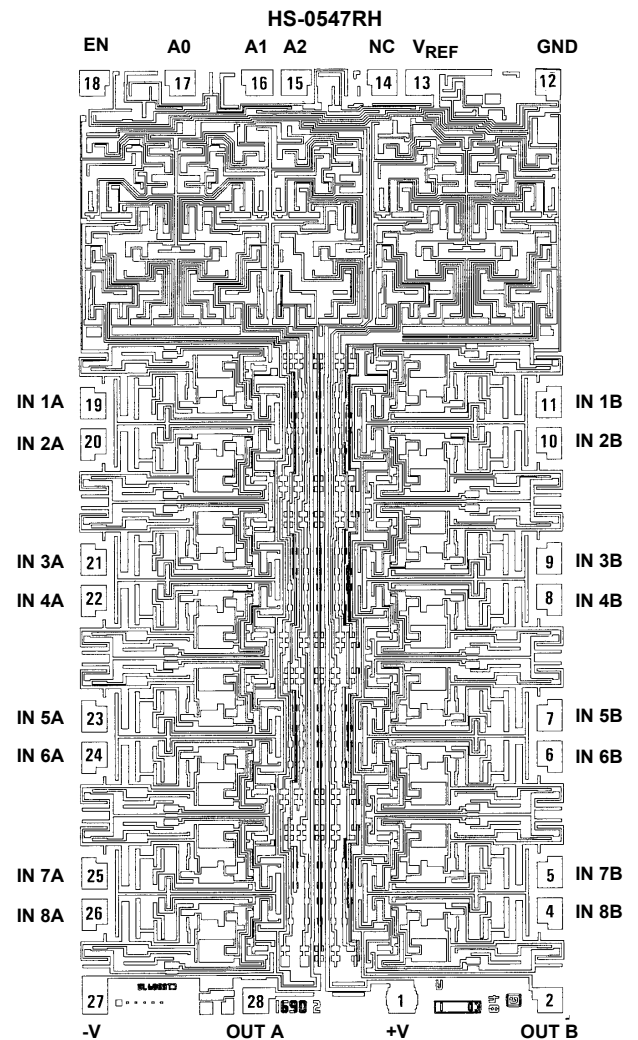
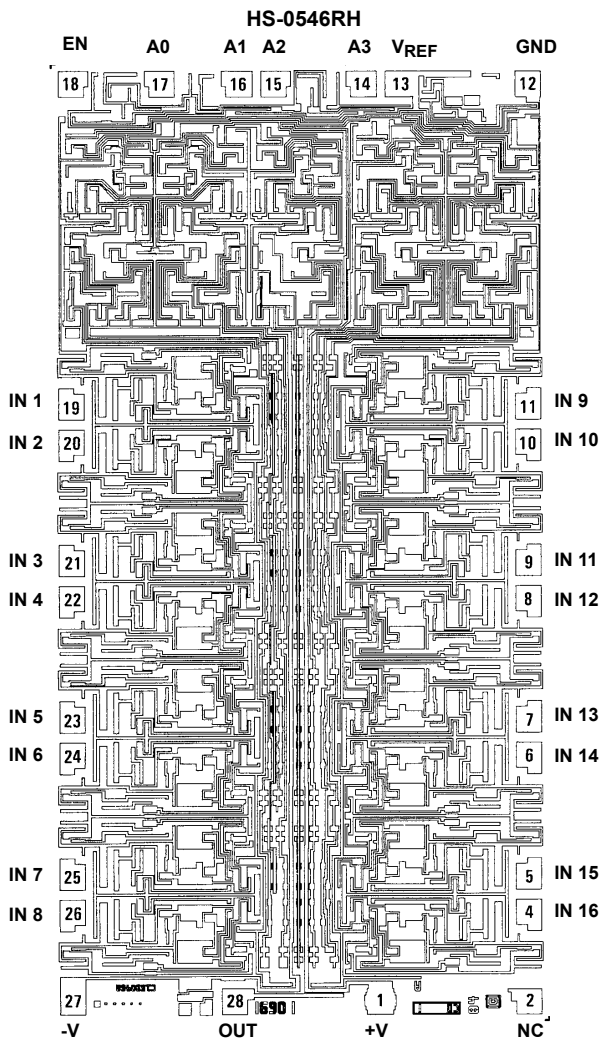
Worst Case Current Density:

$1.4 \times 10^5 \text{ A/cm}^2$

Transistor Count:

HS-0546 - 485
 HS-0547 - 485

Metallization Mask Layout



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