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M32C/80 Series

Using DMACII (Calculation Transfer, Memory + Memory)

1. Abstract

This application note describes how to use single transfers of DMACII in calculation transfer mode.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M32C/80 Series

This program can also be used when operating other microcomputers within the M16C family, provided they have DMACII function. However, some functions may have been modified.
Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Detailed description

The following explains an example use of DMACII transfer for the case where when an interrupt request which has had its priority level set to 7 by the interrupt control register occurs, the contents of two memory locations are added together and the added content is transferred to a given memory location by a DMACII transfer.

During calculation transfer mode when a DMACII request occurs, the content of a memory location specified by SADR (or immediate data) and that specified by OADR are added together and the added content is transferred to a memory location specified by DADR.
If the source of transfer direction is made variable, the source of transfer address and the address to be operated on become variable.
Figure 1 shows a typical operation of an calculation transfer.

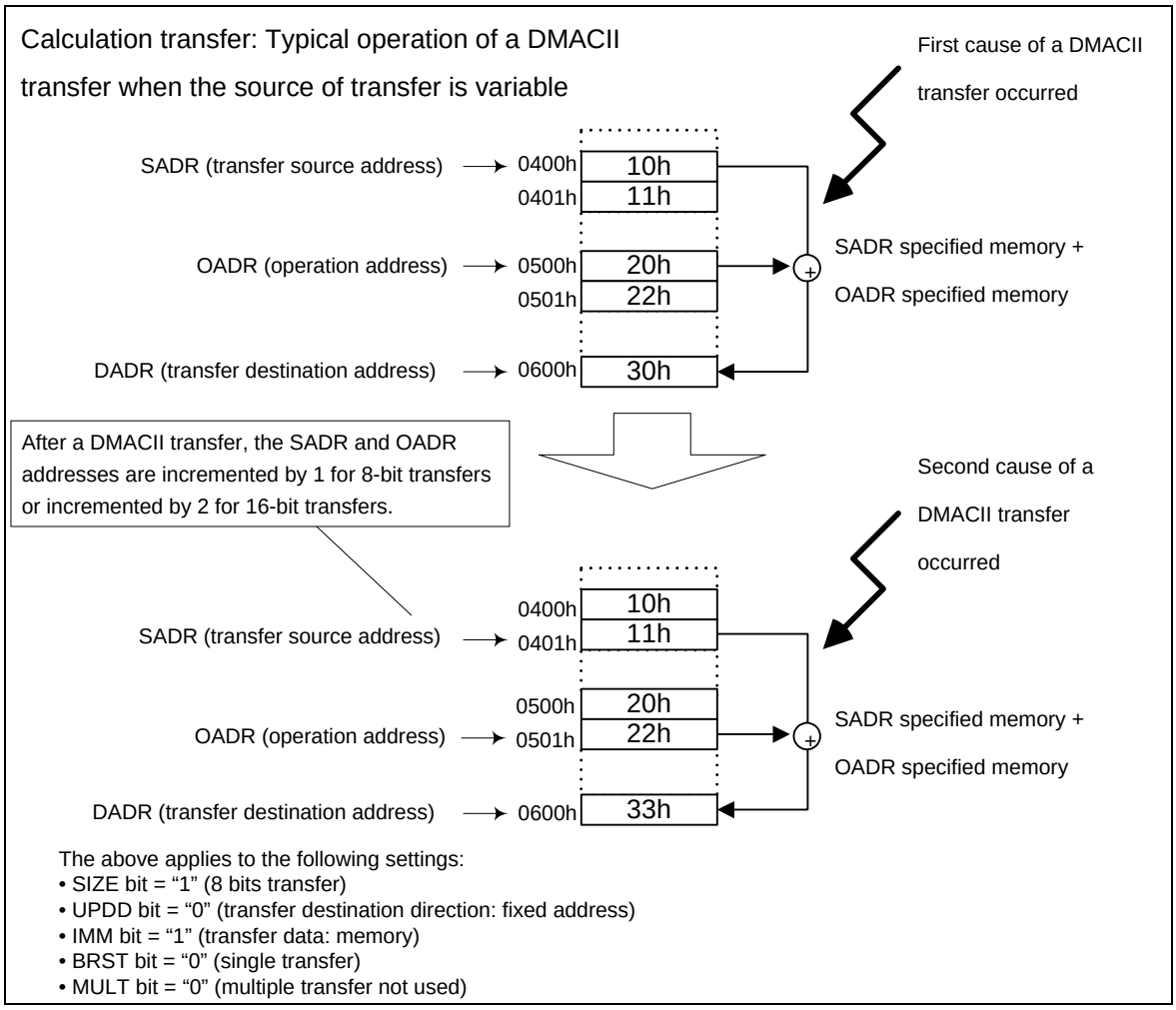


Figure 1 DMACII Typical Operation of a DMACII Calculation Transfer

3.1 DMAC II Transfer Mode

This application note example offers functions of single transfer mode (calculation transfer mode) shown in Table 1.

Table 1 Selectable Functions in Single Transfer Mode (Calculation Transfer Mode)

Item	Definition	Selection
Transfer Block	8 bits	Yes
	16 bits	
Transfer Data	Immediate data	
	Data in memory	Yes
Source Direction	Fixed address	
	Forward address	Yes
Destination Direction	Fixed address	Yes
	Forward address	
End-of-Transfer Interrupt	Interrupts not used	Yes
	Interrupts used	
Chained Transfer Function	Not chain transferred	Yes
	Chain transferred	

3.2 DMAC II Index

The DMAC II index is configured with 10 bytes when interrupts and chain transfers are not used in calculation transfer mode. The DMAC II index must be located on the RAM area.

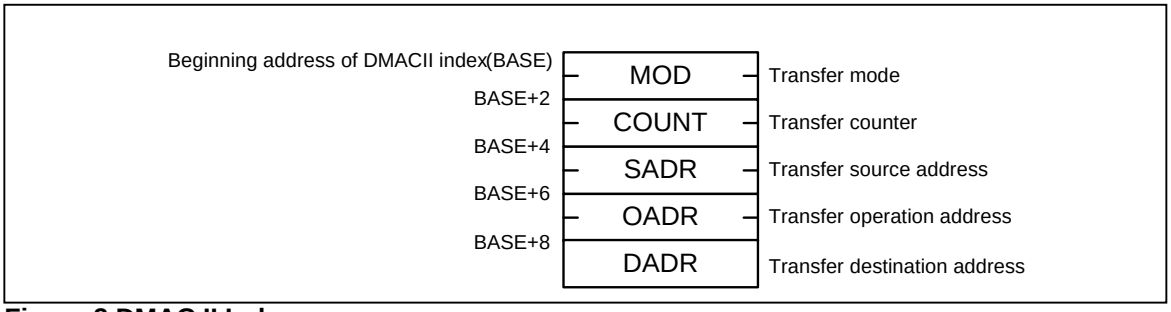


Figure 2.DMAC II Index

3.3 DMAC II Transfer

The interrupt requests from all peripheral functions whose ILVL2–ILVL0 bits in the interrupt control register have been set to “111b” constitute the cause of requests to DMAC II. In this application note, the INT0 interrupt is used for the cause of DMAC II request.

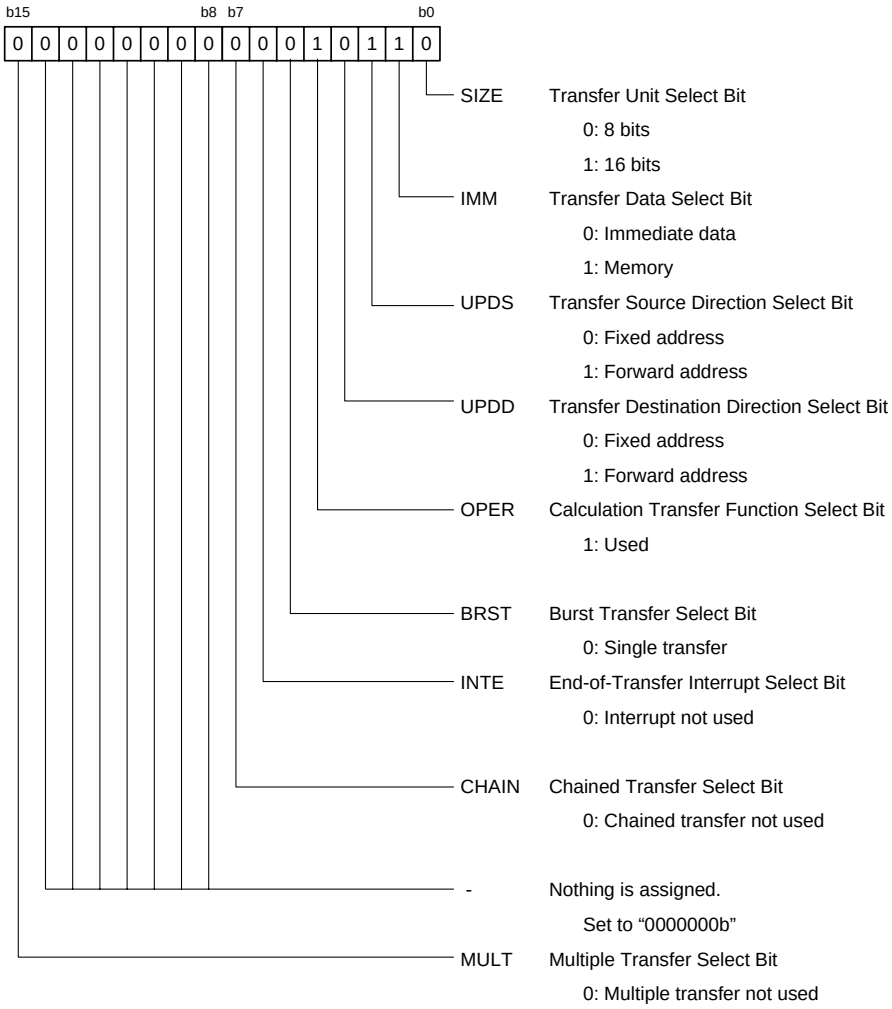
3.4 Setting Up the Relocatable Vector Table

Set the beginning address of the DMAC II index in the interrupt vector for the peripheral function interrupt that constitutes the cause of DMAC II request.

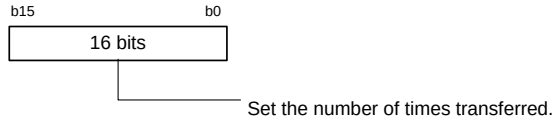
3.5 Register Setting

To enable the operation defined in "Section 3. Detailed description", the following register settings must be taken place step by step. For detail configuration of each register, please refer to M32C/80 Series HARDWARE MANUAL.

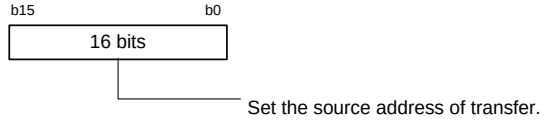
(1) Transfer mode (MOD)



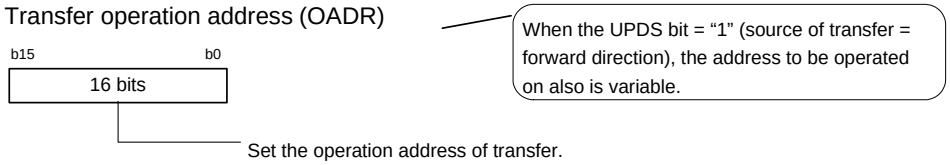
(2) Transfer count (COUNT)



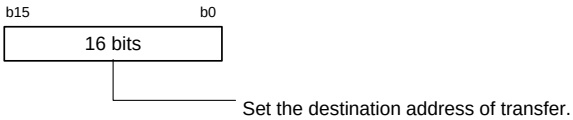
(3) Transfer source address (SADR)



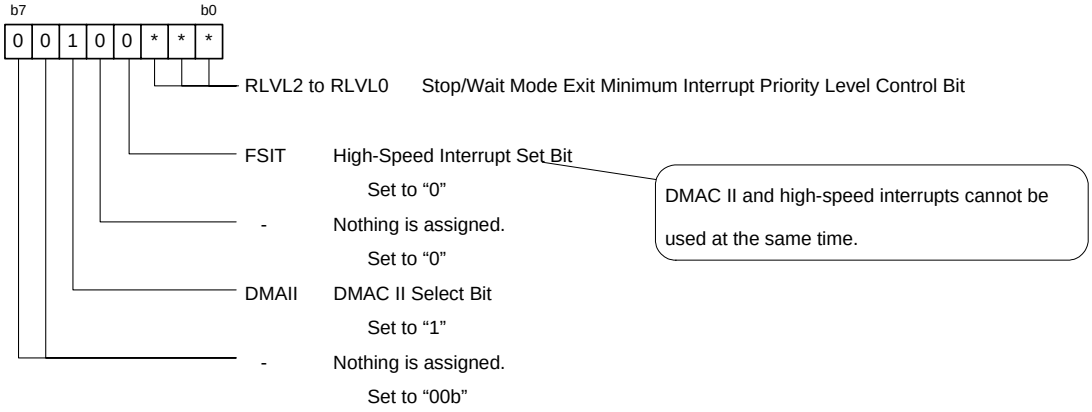
(4) Transfer operation address (OADR)



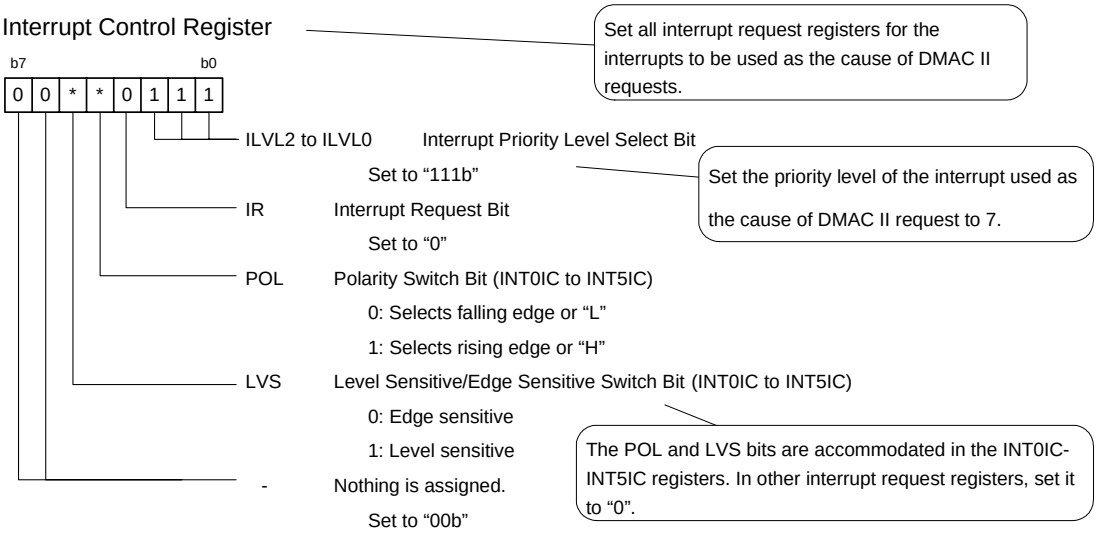
(5) Transfer destination address (DADR)



(6) RLVL register



(7) Interrupt Control Register



4. Example of a Sample Program

4.1 C language source

```
/*****************************************************************************
/*  FILENAME: rej05b0638_src.c                                        *
/*  Ver : 1.00                                                      *
/*  FUNCTION: DMACII(Calculation Transfer, Memory + Memory)              *
/*****************************************************************************/
/*****************************/
/*   include file            */
/*****************************/
#include <stdio.h>
#include "sfr32c83.h"

/*****************************/
/*   DMACII                  */
/*****************************/
struct{
   union {
      struct{
         char    size:1;        /* Transfer Unit Select Bit */
         char    imm:1;         /* Transfer Data Select Bit */
         char    upds:1;        /* Transfer Source Direction Select Bit */
         char    updd:1;        /* Transfer Destination Direction Select Bit */
         char    oper:1;        /* Calculation Transfer Function Select Bit */
         char    brst:1;        /* Burst Transfer Select Bit */
         char    inte:1;        /* End-of-Transfer Interrupt Select Bit */
         char    chain:1;       /* Chained Transfer Select Bit */
         char    reserve:7;
         char    mult:1;        /* Multiple Transfer Select Bit */
      }bit;
      unsigned short  all;
   }mod;
   unsigned short count;      /* Transfer count */
   unsigned char near *sadr;   /* Transfer source address */
   unsigned char near *oadr;   /* Transfer operation address */
   unsigned char near *dadr;   /* Transfer destination address */
}dm_index;

/*  Transfer data array  */
static unsigned char near data[5] = {0x10,0x20,0x30,0x40,0x50};
/*  Calculation data array */
static unsigned char near cal_data[5] = {0x01,0x02,0x03,0x04,0x05};
/*  Transfer destination memory */
static unsigned char near dest;

/*****************************/
/*   main                    */
/*****************************/
void main(void){
   asm("   fclr    i   ");    /* Interrupt disable */
   /*  DMACII setting  */
```

```
    dm_index.mod.all = 0x0016;  /* Transfer Unit:      8bit    */
                           /* Transfer Data:      Memory  */
                           /* Transfer Source:    Forward */
                           /* Transfer Destination:Fixed   */
                           /* Calculation Transfer:Have    */
                           /* Burst Transfer:     Single  */
                           /* Interrupt:          None    */
                           /* Chained Transfer:   None    */
                           /* Multiple Transfer:  None    */

    dm_index.count = 5;        /* number of transfer  = 5 */
    dm_index.sadr = data;      /* Source of transfer  = beginning address of the data array    */
    dm_index.oadr = cal_data;  /* Calculation address = beginning address of the cal_data array */
    dm_index.dadr = &dest;     /* Set destination of transfer */

    /*  Set the interrupt used for DMAC II  */
    rlvl = 0x20;             /* Interrupt priority level 7 is used for DMAC II transfers */

    int0ic = 0x07;           /* INT0 interrupt level 7 (used for DMACII) */

    while(1);
}
```

4.2 Relocatable Vector Tables

```
    ;-----------------------------------------------------------------
    ; variable vector section
    ;-----------------------------------------------------------------
              .section  vector,ROMDATA              ; variable vector table
              .org      VECTOR_ADR

              .lword    dummy_int           ; BRK (software int 0)
              .lword    dummy_int           ;
              .lword    dummy_int           ;
              .lword    dummy_int           ;
              .lword    dummy_int           ;
              .lword    dummy_int           ;
              .lword    dummy_int           ;
              .lword    dummy_int           ; DMA0 (software int 8)
    ;
    ;
    ;                           (Omission)
    ;
    ;
              .lword    dummy_int           ; INT5 (software int 26)
              .lword    dummy_int           ; INT4 (software int 27)
              .lword    dummy_int           ; INT3 (software int 28)
              .lword    dummy_int           ; INT2 (software int 29)
              .lword    dummy_int           ; INT1 (software int 30)
              .glb      _dm_index
              .lword    _dm_index           ; INT0 (software int 31)
              .lword    dummy_int           ; TIMER B5 (software int 32)
    ;
    ;
    ;                           (Omission)
    ;
    ;
```

5. Reference

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M32C/80 Group Hardware Manual
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