R8C/33T Group

The implement of the inverter noise immunity by SCU setting

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Summary

Touch panel microcomputer R8C/33T group builds hardware (SCU: sensor control unit) that perceives the contact of the human body by measuring the stray capacity generated between the touch electrode and the human body into.

In this application note we describe the influence of inverter noise and its reducing method.

Target device

R8C/33T group

Contents

1. Influence of the inverter noise for the touch detecting

1.1 Outline

R8C/33T SCU capacitance touch sensing measures the count value using the threshold voltage of CHxA terminal. And power supply, RF (Radio Frequency), and the other noises influence to the count value for the touch detecting. In this application note, we show the method of the inverter noise (approximately 20KHz to 300KHz switching noises) immunity.

1.2 Inverter noise image

Figure 1.2-1 shows the evaluation environment of noise immunity. We used our demonstration Board for R8C/33T and triple CCFL(Cold Cathode Fluorescent Lamp) unit.

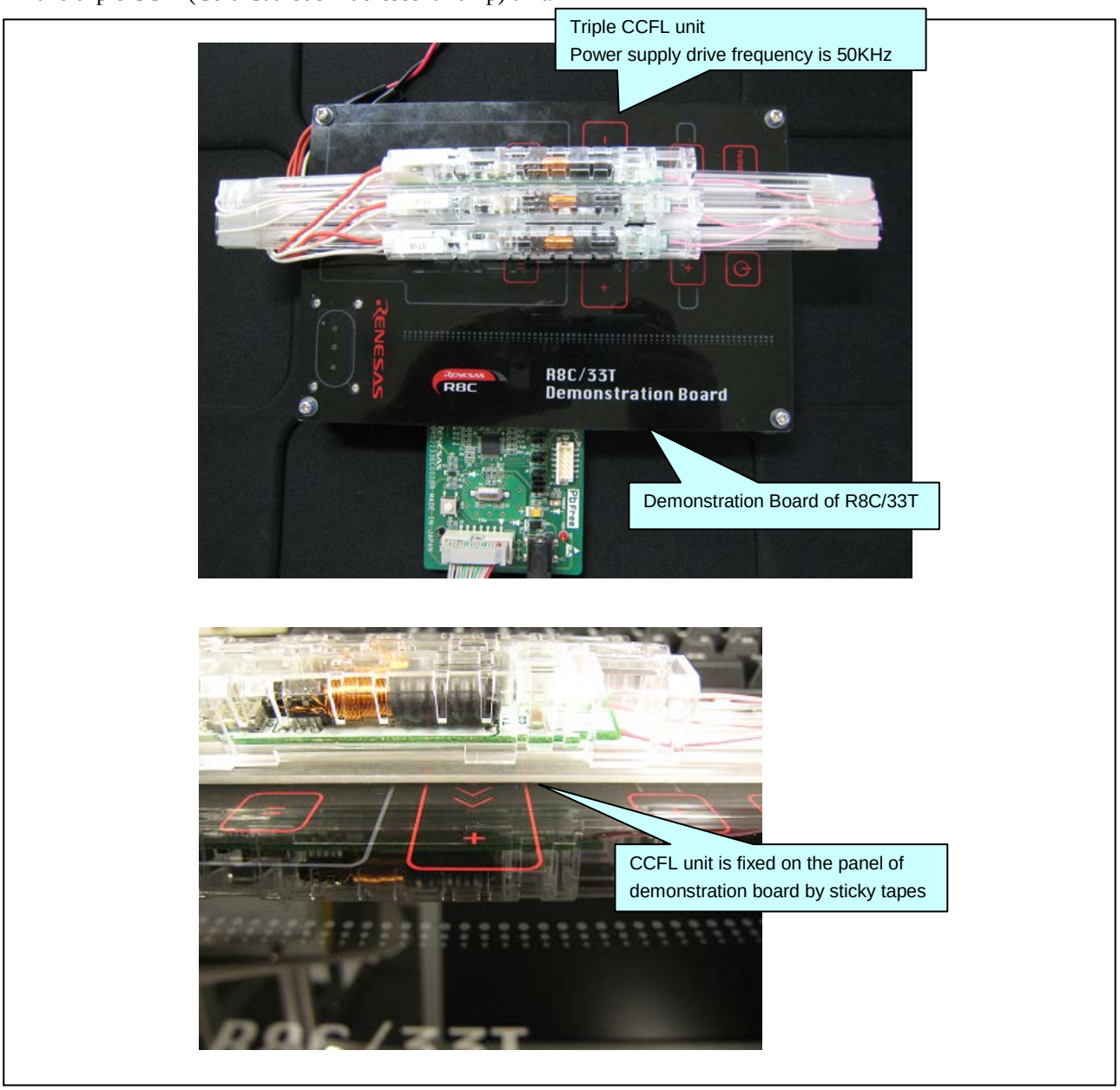
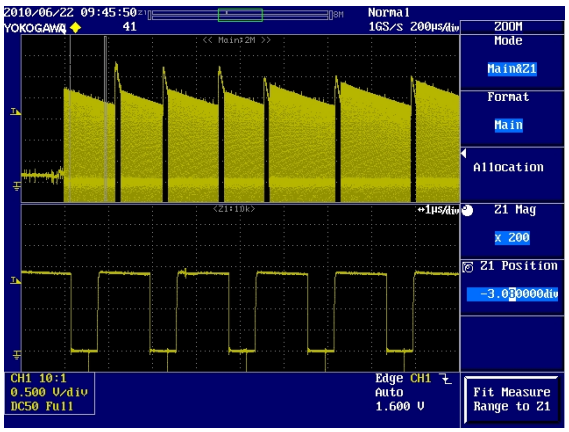
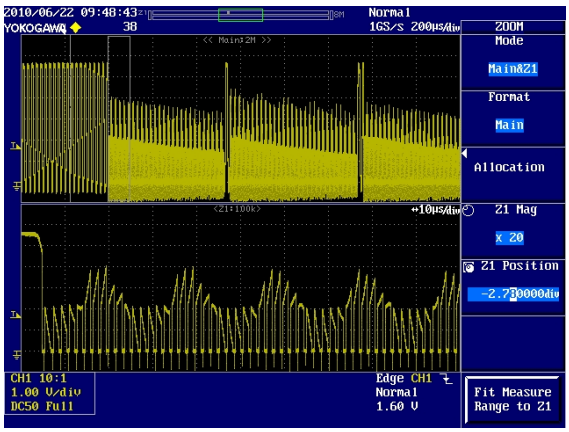


Figure 1.2-1 the evaluation environment

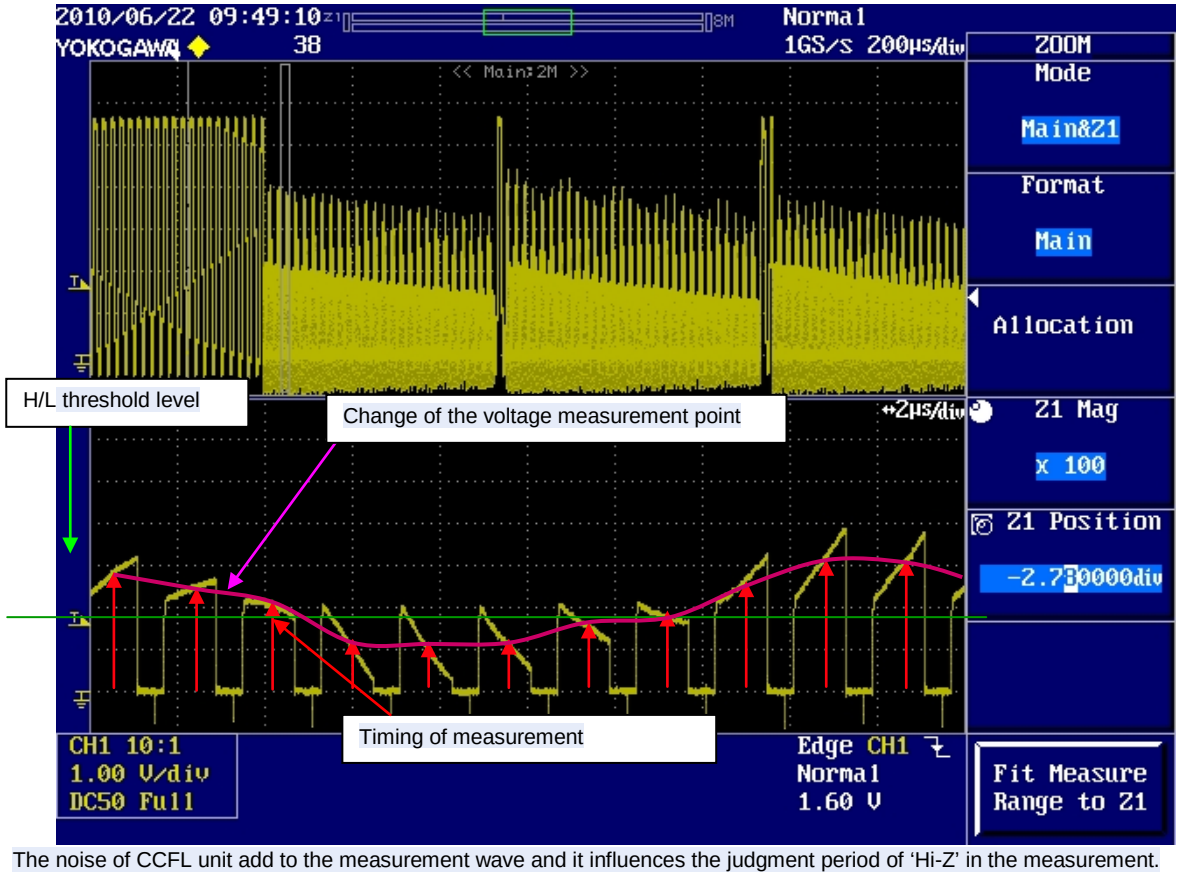
Figure 1.2-2 shows the waveform of touch measurement when CCFL unit turns ON. When the noise amplitude (noise intensity) is large at measuring terminal (CHxA), it influences to the periods of 'Hi-z'. Because the periods of 'Hi-z' is the judgment timing of 'High' or 'Low', the noise makes the judgment of touch or not frustrate.



The measurement waveform of noise-free.



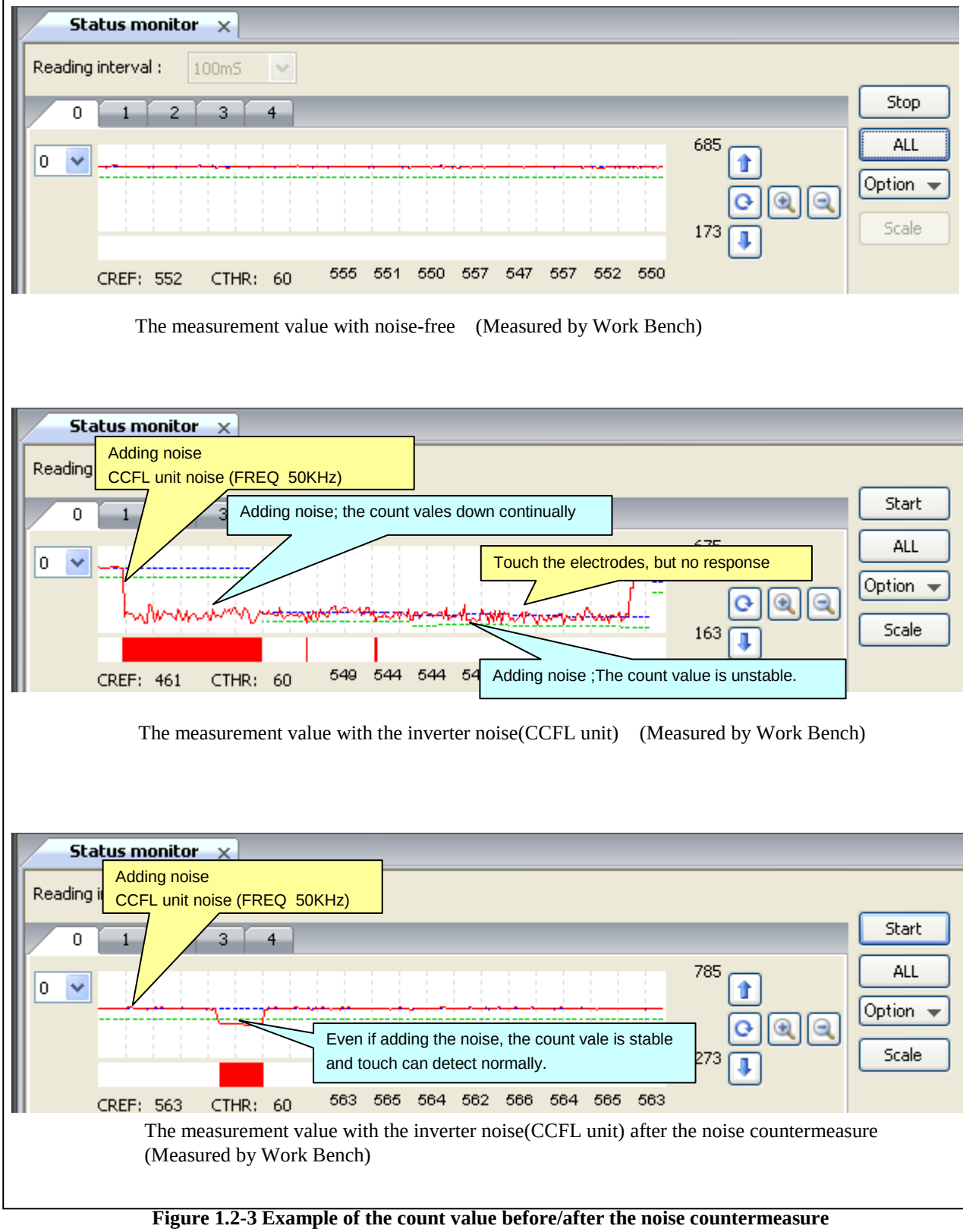
The measurement waveform of adding inverter noise (CCFL unit turn ON)



The noise of CCFL unit add to the measurement wave and it influences the judgment period of 'Hi-Z' in the measurement.

Figure 1.2-2 Waveform of terminal CHxA with CCFL unit turn ON

Similarly, Figure 1.2-3 shows the example of the influence for the count value and the count value with the countermeasure of the inverter noise.



The measurement value with noise-free (Measured by Work Bench)

The measurement value with the inverter noise(CCFL unit) (Measured by Work Bench)

The measurement value with the inverter noise(CCFL unit) after the noise countermeasure (Measured by Work Bench)

Figure 1.2-3 Example of the count value before/after the noise countermeasure

2. How to reduce the noise influence

2.1 Reduction of the inverter noise influence

For the noise reduction of 20KHz - 300KHz zone, it is important to judge the timing of 'high' or 'Low'.
As shown Figure 2.1-1, the measure waveform of 'Hi-Z' period is unstable by the noise influence and the edge of 'Low' to 'Hi-Z' is more stable than 'Hi-Z' period (See red line). So it is measured at this timing to reduce the noise.

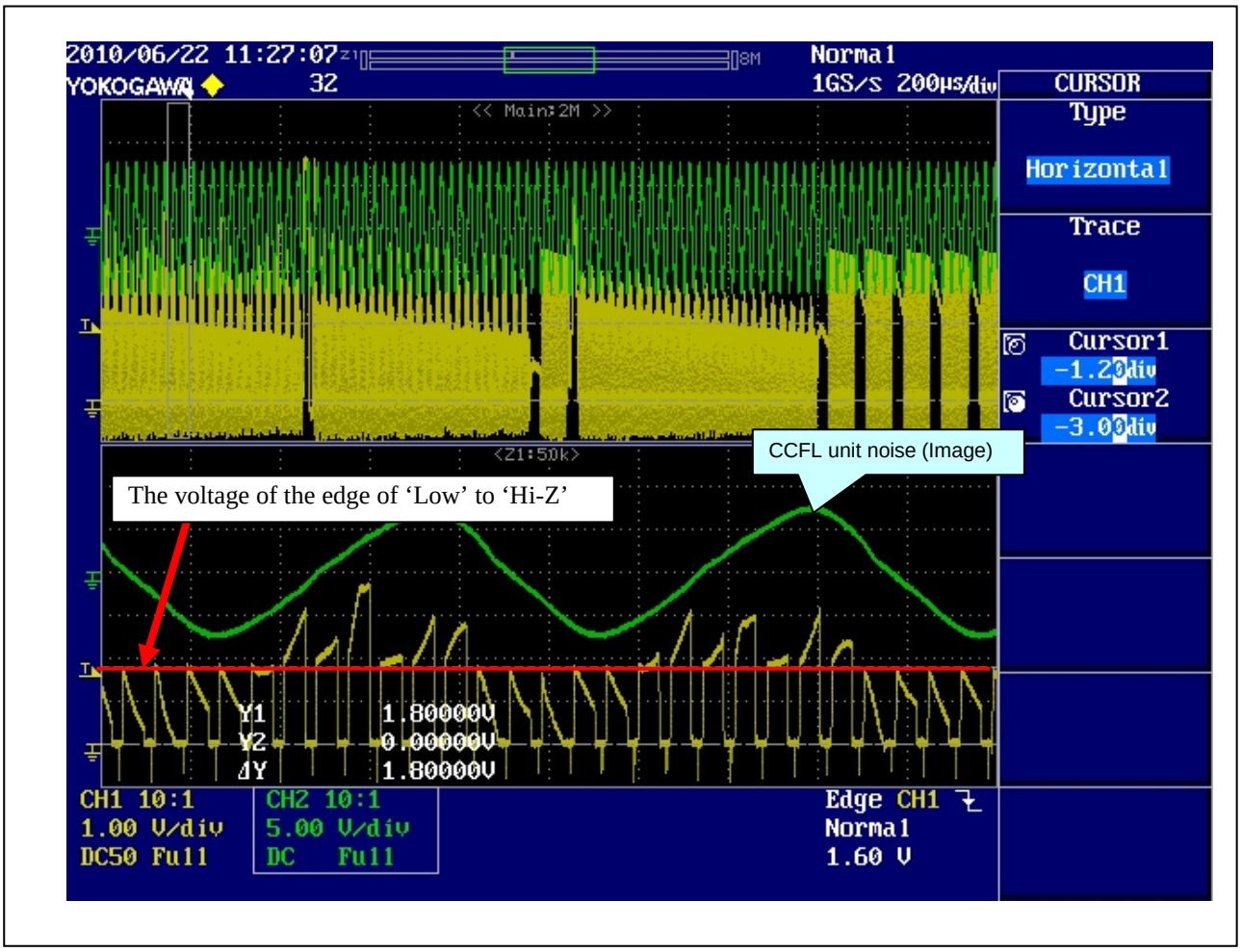
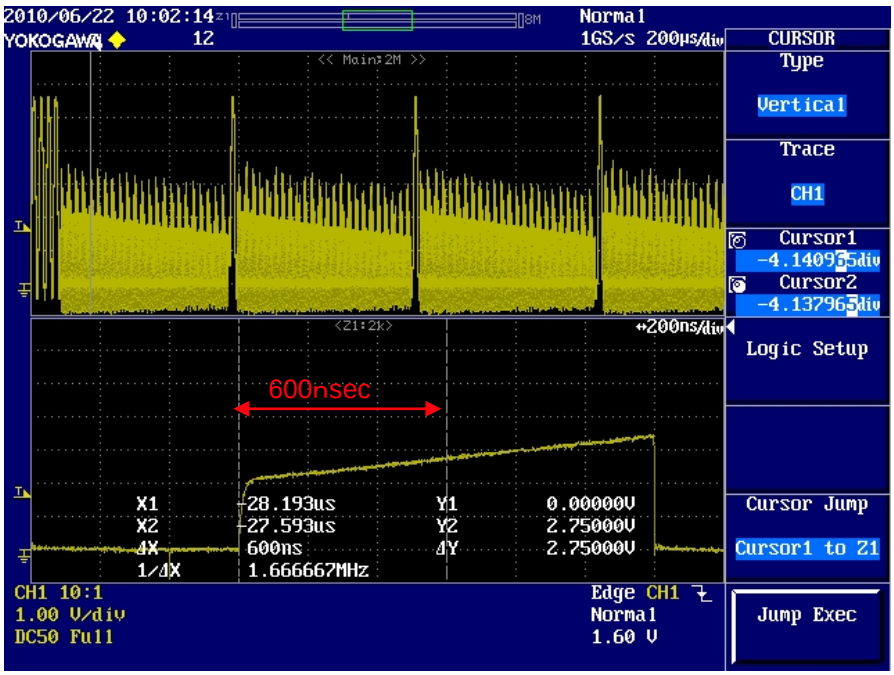


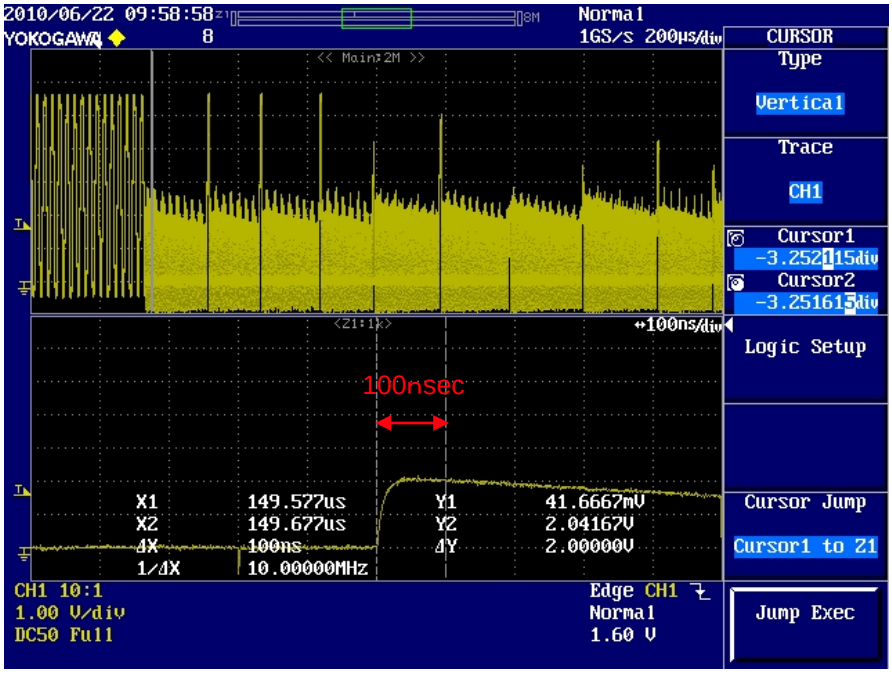
Figure 2.1-1 the waveform of the measurement (CHxA)

2.2 Optimization of the measurement timing

Figure 2.2-1 shows the example of optimization of the measurement timing(the time during the edge of ‘Low’ to ‘Hi-Z’ and judgment time of ‘High’ or ‘Low’) by SCU setting.



Before optimization; 600nSEC (from ‘Low’ to judgment timing)



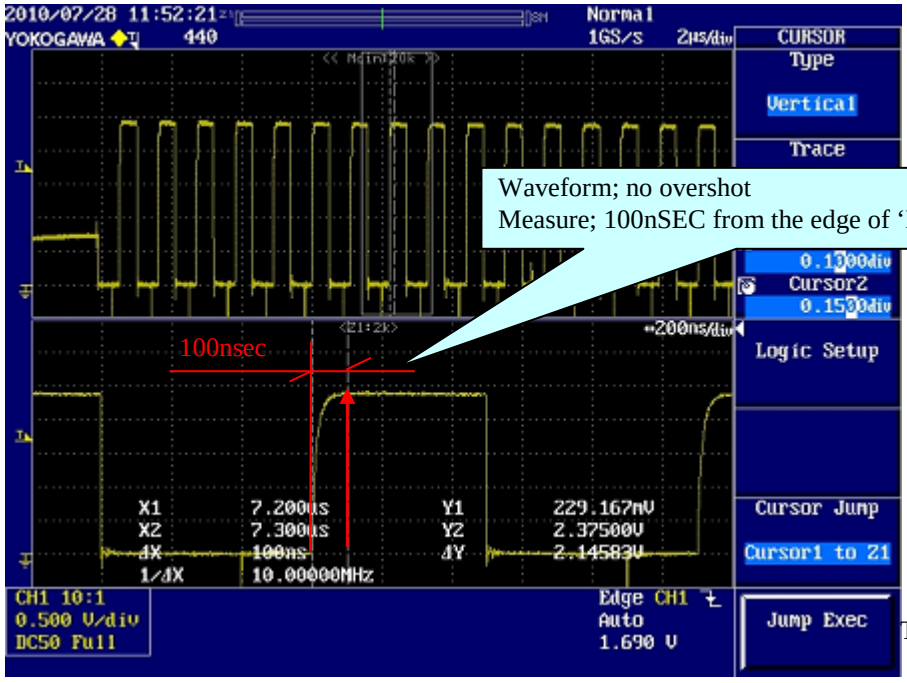
After optimization; 100nSEC (from ‘Low’ to judgment timing)

Figure 2.2-1 the example of optimization the measurement timing

2.3 Overshot problem

To reduce the noise influence, it is effective to judge ‘High’ or ‘Low’ just after the edge from ‘Low’ to ‘Hi-Z’. But in certain case of user application, the overshot is appeared in the waveform by the influence of parasitic capacitance, impedance of electrodes and wires, resistance of Rr and etc. It is important that the judgment of ‘High’ or ‘Low’ timing is set between “just after the edge from ‘Low’ to ‘Hi-Z’ “ and “the point that the overshot influence is minimum”. Please refer Figure 2.3-1 to understanding above.

Note; if the timing of judgment is on the overshot, the change value of touch or not is more decrease than the other timing.



The waveform of CHxA

The waveform of CHxA

Figure 2.3-1 the overshot influence and the best timing of judgment

2.4 The setting of the secondly counter

If the noise influence is large, the voltage of the measurement timing is unstable though the timing of judgment is adjusted as above. The unstable voltage also makes the measurement value being unstable. For such unstable voltage, it is possible that the measurement value is stable to set the secondly counter of SCU larger than normal condition.

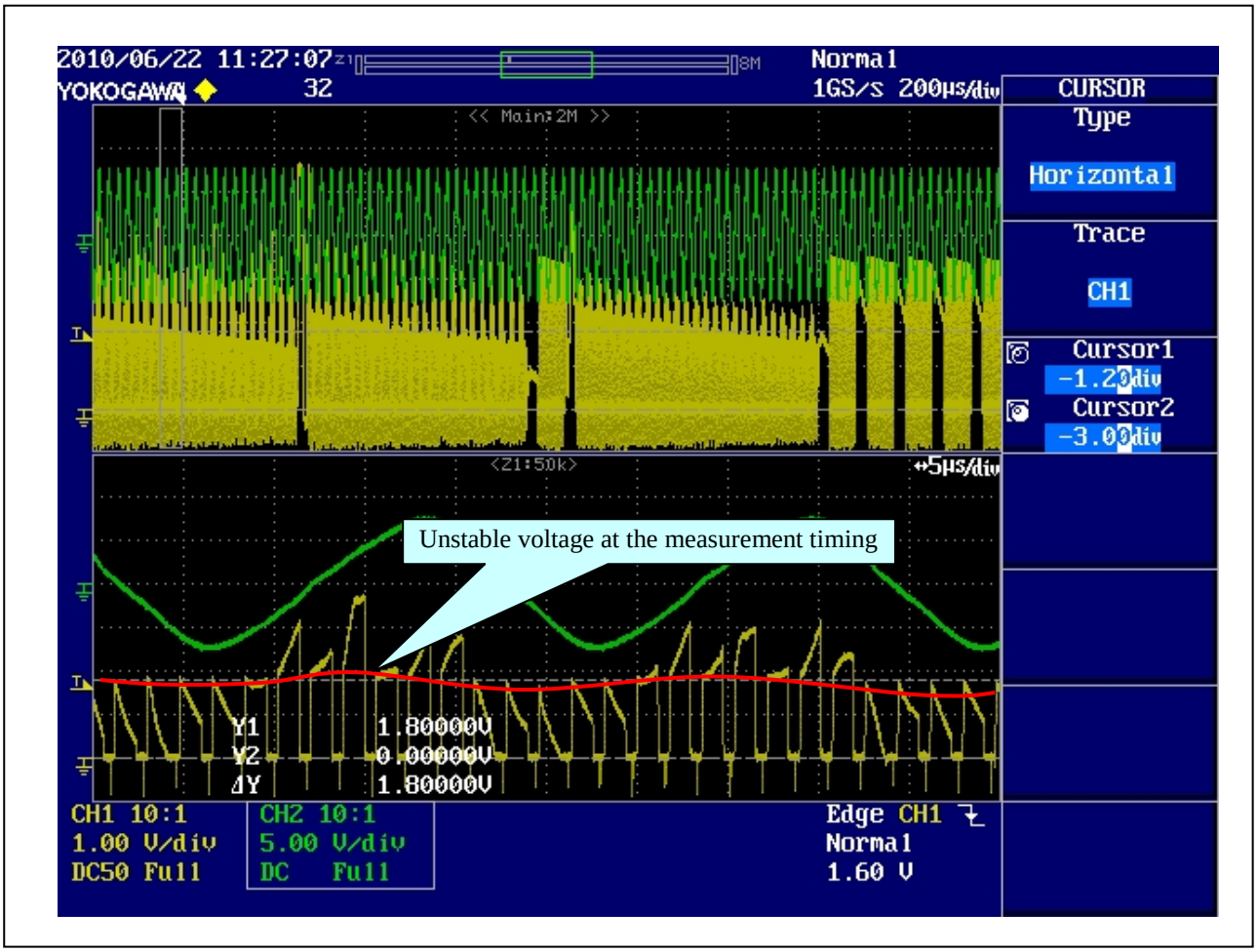


Figure 2.4-1 The unstable voltage of measurement point(CHxA)

Regarding the secondly counter setting, please refer the application note of “MW broadcasting noise immunity improvement by SCU (REJ05B1388-0100.doc)”

3. The setting of SCU resister

3.1 The status periods of measurement

Figure 3.1-1 shows the SCU status periods.
(Please refer R8C/33T group hardware manual to understand detail of it.)
We define the measure after 'Period 5' as 'Main measurement' and describe as follows.

Note; Please note there are 1cycle clock gaps between 'period 4' and 'period 5', after 'period 6' and end of 'Hi-Z' period.

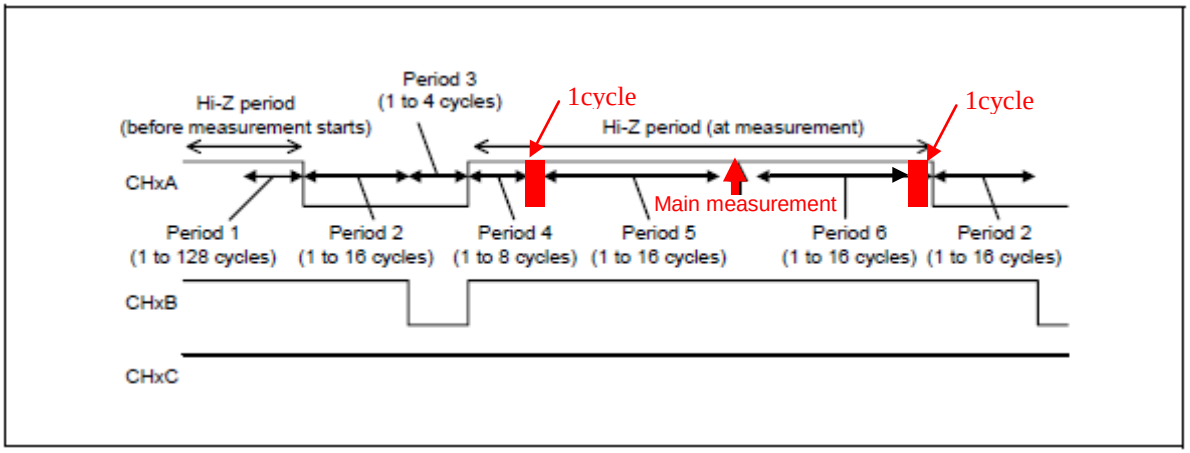


Figure 3.1-1 SCU status periods

3.2 The setting of SCU resister

'Period 4' and 'Period 5' are changed for the adjustment of measurement timing.
Formula 3.2-1 shows the time from the edge (of 'Low' to 'Hi-Z') to the measurement timing (judgment of 'H/L') .

Measurement timing = (Cycle numbers of 'period 4' + Cycle numbers of 'period 5' + 1 cycle)

Note; 1 cycle time is provided the SCU clock setting. (Ex. If SCU clock set 20MHz, 1cycle = 50nSEC)

Formula 3.2-1 the formula of measurement timing

Caution; For optimization of measurement timing, if you will change the SCU clock, please consider the charge/discharge cycle for capacitor 'CC' and measure the real waveform to check it.

3.3 The example of setting SCU resister for the noise immunity

The example of setting SCU resister for the noise immunity is shown as follows;

Resister Name	Define	Value	Remarks
SCUCR0	SCU Control Register 0	0x86	SCU clock = 20MHz
SCUMR	SCU Mode Register soft trriger	0x00	-
SCTCR0	SCU Timing Control Register 0 charge max	0x7F	Period 1 = 128cycle
SCTCR1	SCU Timing Control Register 1 Larea 2cyc	0x37	Period 2 = 8cycle,Period 3 = 4 cycle
SCTCR2	SCU Timing Control Register 2	0x08	Period 4 = 1cycle,Period 5 = skip
SCTCR3	SCU Timing Control Register 3	0x05	Period 6 = 6cycle
SCHCR	SCU Channel Control Register 22ch up-down scan	0x95	22ch up scan
SCSCSR	SCU Secondary Counter Set Register 7count	0x1F	Secondly counter = 32 times
SCUCR1	SCU Control Register 1	0x00	-

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	May.22.2013	—	Numbering change (Contents is as same as R01AN0160EJ0100)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
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