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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group

Operation of Serial I/O (transmission in clock-synchronous serial I/O mode)

1.0 Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosed functions

Item	Set-up		Item	Set-up	
Transfer clock source	○	Internal clock ($f_1 / f_8 / f_{32}$)	Transmission interrupt factor	○	Transmission buffer empty
		External clock (CLKi pin)			Transmission complete
CTS function	○	CTS function enabled	Output transfer clock to multiple pins (Note 1)	○	Not selected
		CTS function disabled			Selected
CLK polarity	○	Output transmission data at the falling edge of the transfer clock	Data logic select function (Note 2)	○	No reverse
		Output transmission data at the rising edge of the transfer clock	TxD, RxD I/O polarity reverse bit (Note 2)		Reverse
Transfer clock	○	LSB first		○	No reverse
		MSB first			Reverse

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1 CTS/RTS function can not be utilized. Set the UART1 CTS/RTS disable bit to "1".

Note 2: UART2 only.

2.0 Introduction

- Operation
- (1) Setting the transmit enable bit to "1" and writing transmission data to the UARTi transmit buffer register makes data transmissible status ready.
 - (2) When input to the $\overline{\text{CTS}}_i$ pin goes to "L" level, transmission starts (the $\overline{\text{CTS}}_i$ pin must be controlled on the reception side).
 - (3) In synchronization with the first falling edge of the transfer clock, transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the UARTi transmit interrupt request bit goes to "1". Also, the first bit of the transmission data is transmitted from the TxDi pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges.
 - (4) When transmission of 1-byte data is completed, the transmit register empty flag goes to "1", which indicates that transmission is completed. The transfer clock stops at "H" level.
 - (5) If the next transmission data is set in the UARTi transmit buffer register while transmission is in progress (before the eighth bit has been transmitted), the data is transmitted in succession.

Figure 1 shows the operation timing

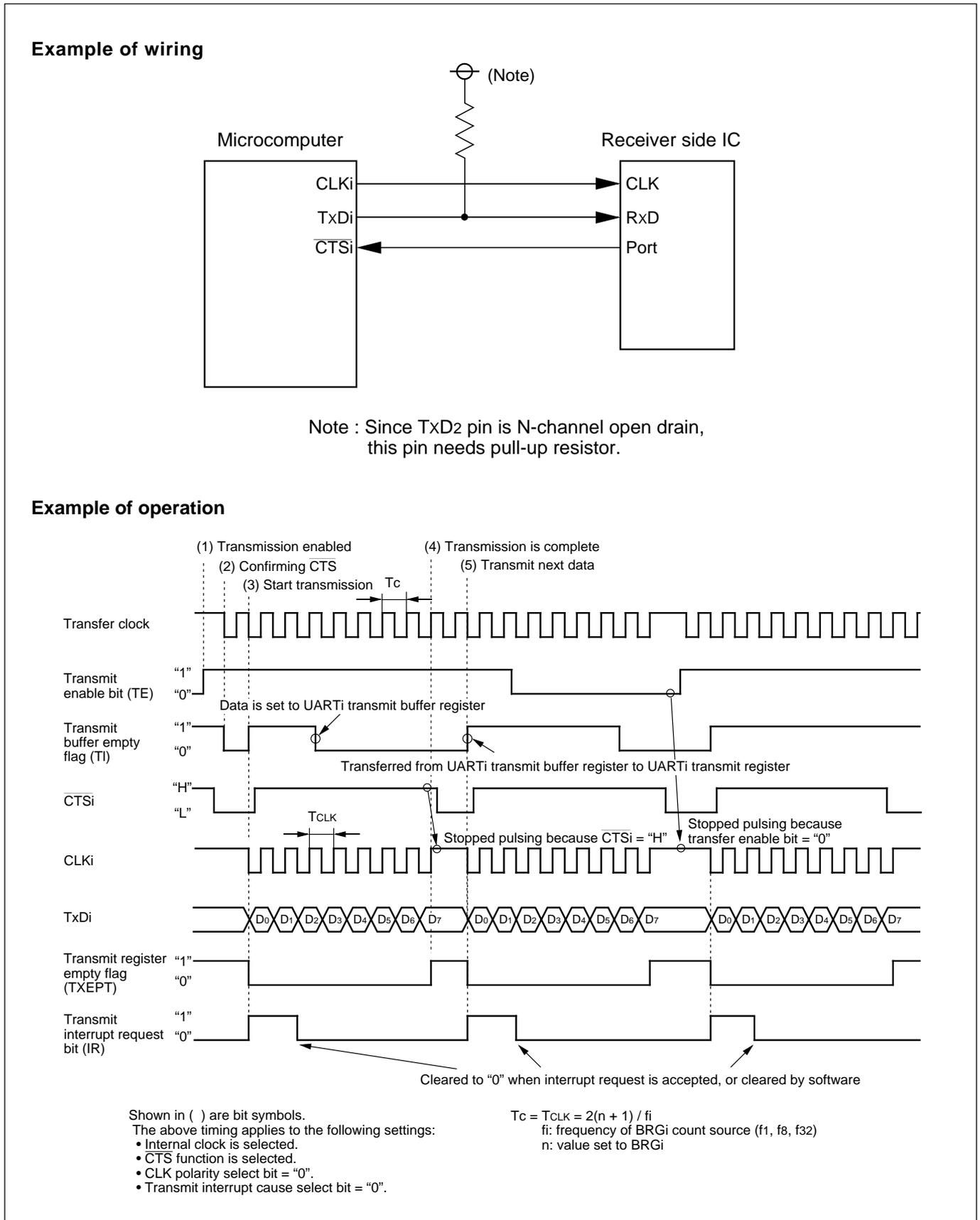
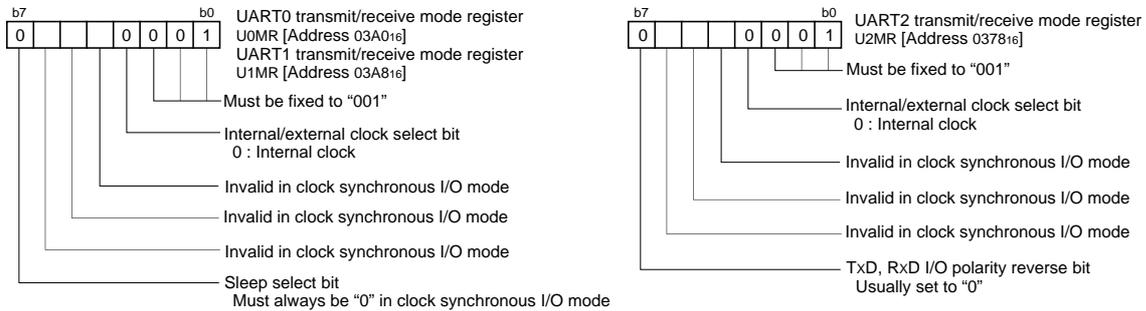


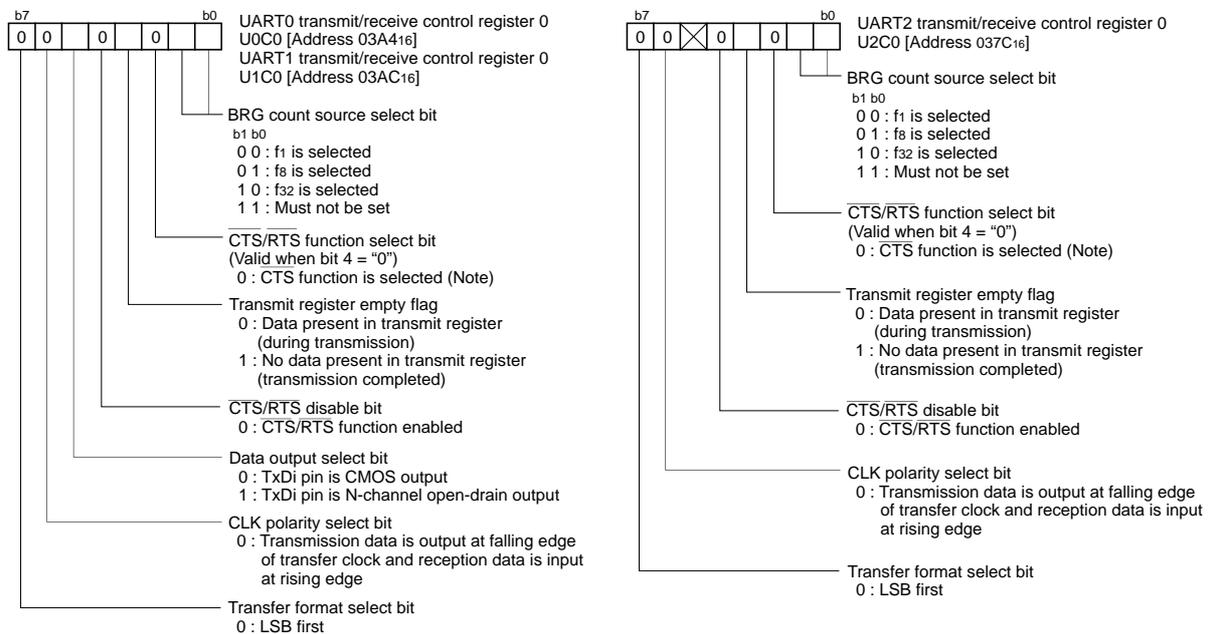
Figure 1. Operation timing of transmission in clock-synchronous serial I/O mode

3.0 Set-up procedure

Setting UART_i transmit/receive mode register (i=0 to 2)

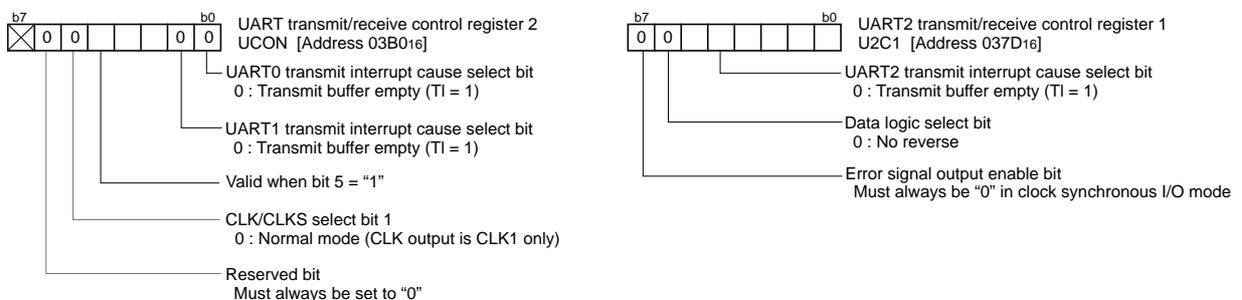


Setting UART_i transmit/receive control register 0 (i=0 to 2)



Note: Set the corresponding port direction register to "0".

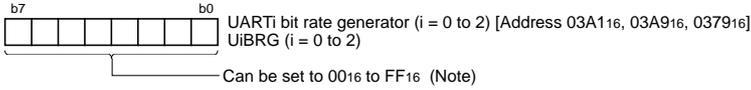
Setting UART transmit/receive control register 2 and UART2 transmit/receive control register 1



Continued to the next page

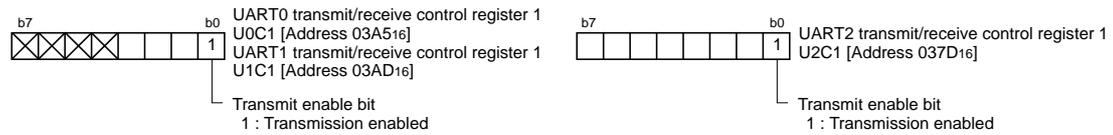
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Setting UARTi bit rate generator (i = 0 to 2)

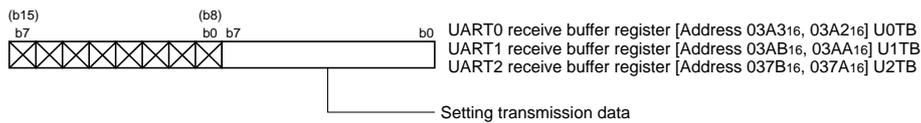


Note: Write to UARTi bit rate generator when transmission/reception is halted.

Transmission enabled

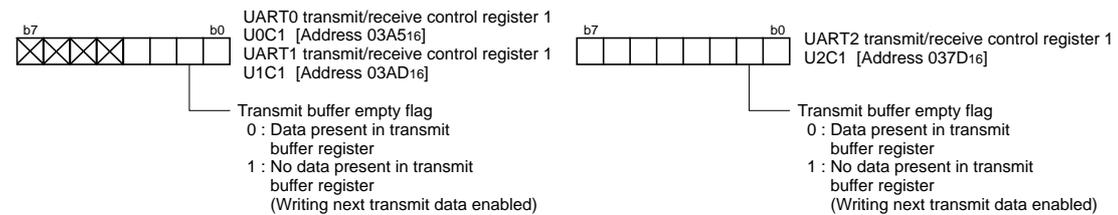


Writing transmit data

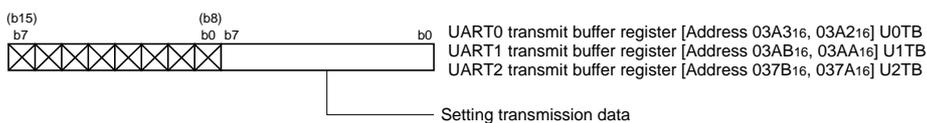


When CTS_i input level = "L"
Start transmission

Checking the status of UARTi transmit /receive control register (i = 0 to 2)



Writing next transmit data



Transmission is complete

4.0 Programming Code

```

;*****
;
; M16C/62A Program Collection
;
; FILE NAME : rjj05b0045_src.a30
; CPU      : M16C/62A Group
; FUNCTION : Operation of Serial I/O
;           (transmission in clock-synchronous serial I/O mode)
; HISTORY  : 2003.05.16 Ver 1.00
;
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;
;*****
;*****
;      Include
;*****
;      .LIST      OFF      ;Stops outputting lines to the assembler list file
;      .INCLUDE   sfr62a.inc ;Reads the file that defined SFR
;      .LIST      ON       ;Starts outputting lines to the assembler list file
;
;*****
;      Symbol definition
;*****
RAM_TOP      .EQU    00400H    ;Start address of RAM
RAM_END      .EQU    00FFFH    ;End address of RAM
ROM_TOP      .EQU    0F8000H   ;Start address of ROM
FIXED_VECT_TOP .EQU    0FFFFDCH ;Start address of fixed vector
;
;*****
;      Allocation of work RAM area
;*****
;      .SECTION   WORKRAM, DATA
;      .ORG      RAM_TOP
WORKRAM_TOP:
C_POWER      .EQU    3
C_DATA_SIZE  .EQU    (1<< C_POWER) ;Data size
v_Trans_data: .BLKB  C_DATA_SIZE   ;Area of send data for sample
WORKRAM_END:
;
;*****
;      Program area
;*****
;=====
;      Start up
;=====
;      .SECTION   PROGRAM, CODE ;Declares section name and section type
;      .ORG      ROM_TOP       ;Declares start address
RESET:
MOV.B        #03H, prcr        ;Removes protect
;                               ;Set processor mode registers 0 and 1
MOV.B        #00000000B, pm0    ; Single-chip mode
MOV.B        #00000000B, pm1    ; No expansion, No wait
;                               ;Set system clock control registers 0 and 1
MOV.B        #00001000B, cm0    ; Xcin-Xcout High
MOV.B        #00100000B, cm1    ; Xin-Xout High, Main clock is No divison
MOV.B        #00H, prcr         ;Protects all registers
;

```

```

; Clears WORKRAM area
MOV.W   #0, R0
MOV.W   #(RAM_END-RAM_TOP)/2, R3
MOV.W   #WORKRAM_TOP, A1
SSTR.W

; Makes transmission data for sample ( 1 to C_DATA_SIZE )
MOV.B   #1, R0L           ;1st data
MOV.W   #0, A0           ;Initialize offset address
MAKE_DATA:
;
MOV.B   R0L, v_Trans_data[A0] ;
ADD.B   #1, R0L           ;
ADD.W   #1, A0           ;
CMP.W   #C_DATA_SIZE, A0  ;
JLTU   MAKE_DATA        ;
;
;=====
;   Serial I/O (transmission in clock-synchronous serial I/O mode)
;=====
MOV.B   #00000001B, u0mr ;Setting UART0 transmit/receive mode register
;
;   ||| |+++-----;Must be fixed to "001"
;   ||| |+-----;Internal/external clock select bit (0:Internal clock)
;   +++-----;Invalid in clock synchronous I/O mode
;   +-----;Sleep select bit
;
;   (Must always be "0" in clock synchronous I/O mode)
MOV.B   #00001000B, u0c0 ;Setting UART0 transmit/receive control register 0
;
;   ||| |++-----;BRG count source select bit (00:f1 is selected)
;   ||| |+-----;CTS function is selected (Valid when bit 4="0") (Note)
;   ||| +-----;Transmit register empty flag
;   ||+-----;CTS/RTS disable bit (0:CTS/RTS function enabled)
;   |+-----;Data output select bit (0:TxDi pin is CMOS output)
;   +-----;CLK polarity select bit
;
;   (0:Transmission data is output at falling edge of
;   transfer clock and
;   reception data is input at rising edge)
;
;   +-----;Transfer format select bit (0:LSB first)
BCLR   pd6_0           ;(Note) Set the corresponding port direction register to "0"
MOV.B   #00000000B, ucon ;Setting UART transmit/receive control register 2
;
;   ||| |+-----;UART0 transmit interrupt cause select bit
;   ||| |           (0:Transmit buffer empty (TI=1) )
;   ||| +-----;UART1 transmit interrupt cause select
;   |+-----;Valid when bit 5="1"
;   |+-----;CLK/CLKS select bit 1 (0:Normal mode;CLK output is CLK1 only)
;   +-----;Reserved bit (Must always be set to "0")
MOV.B   #07H, u0brg    ;Setting UART0 bit rate generator (1MHz, @16MHz f1)
MOV.B   #00000001B, u0c1 ;UART0 transmit/receive control register 1
;
;   +-----;Transmission enabled
;
;=====
;   Main program
;=====
MOV.W   #0, A0           ;Initialize offset
WRITE_DATA:
MOV.B   v_Trans_data[A0], u0tb;Writing transmit data
;
WAIT_TRANS:
BTST   ti_u0c1           ;Checking the status of UART0 transmit buffer empty flag
JNC    WAIT_TRANS
;
PREPARE_NEXT_DATA:
ADD.W   #1, A0
AND.W   #(C_DATA_SIZE-1), A0
JNZ    WRITE_DATA
;

```

```

COMPLETE_TRANS:
    JMP     COMPLETE_TRANS
;
;=====
;    Dummy interrupt processing program
;=====
dummy:
    REIT
;
;*****
;    Setting of fixed vector
;*****
    .SECTION    F_VECT, ROMDATA
    .ORG        FIXED_VECT_TOP
;
    .LWORD     dummy    ;Undefined instruction interrupt vector
    .LWORD     dummy    ;Overflow (INT0 instruction) interrupt vector
    .LWORD     dummy    ;BRK instruction interrupt vector
    .LWORD     dummy    ;Address match interrupt vector
    .LWORD     dummy    ;Single-step interrupt vector
    .LWORD     dummy    ;Watchdog timer interrupt vector
    .LWORD     dummy    ;DBC interrupt vector
    .LWORD     dummy    ;NMI interrupt vector
    .LWORD     RESET    ;Sets reset vector
;
    .END

```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

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Data Sheet

M16C/62A group Rev. C.1

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User's Manual

M16C/62A group Rev. 1.0

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