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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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R8C/Tiny Series

General-purpose Program for Dividing BCD

1. Abstract

This program divides 8-digit BCD by using registers.

2. Introduction

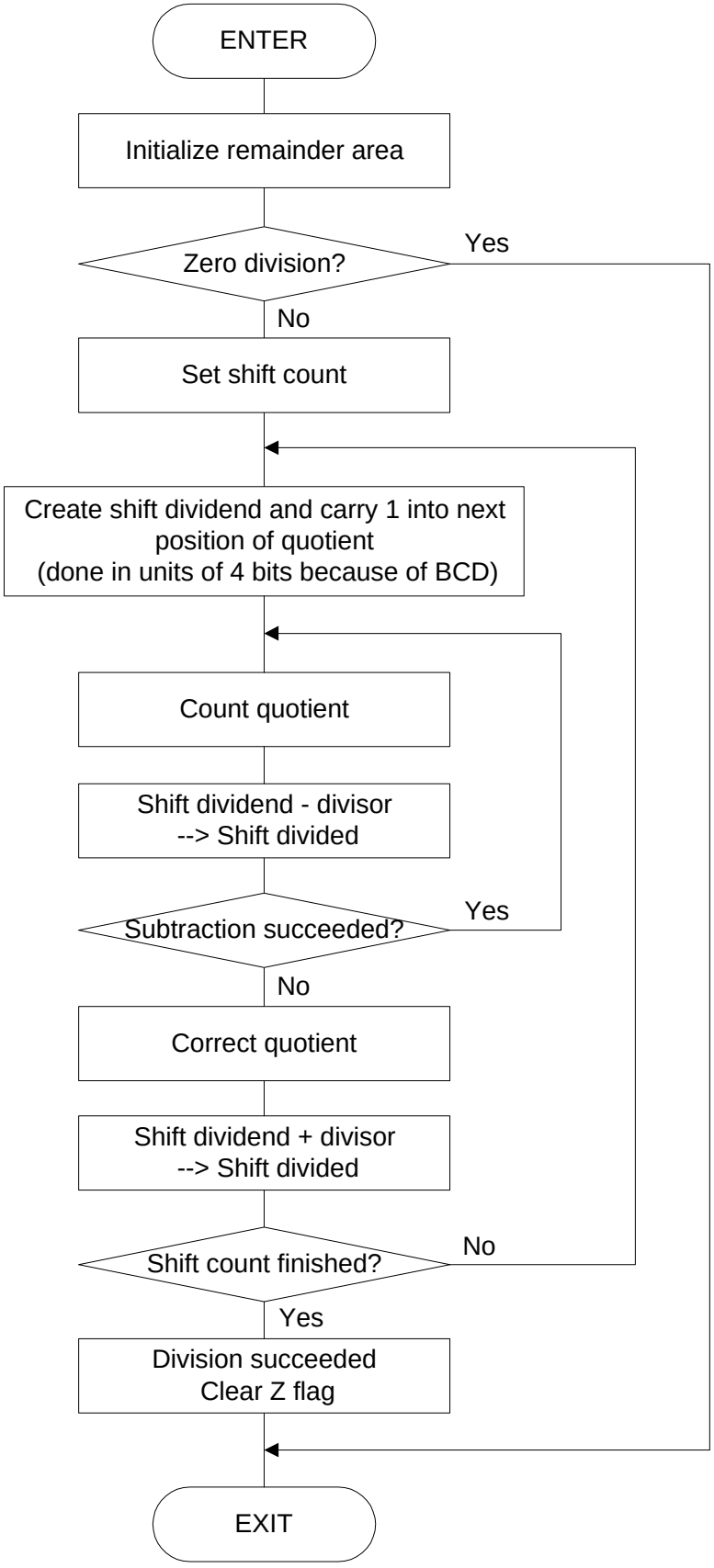
This program divides 8-digit BCD together by using registers. Set the dividend in A1 and A0 and the divisor in R3 and R1 beginning with the upper half, respectively. The quotient and the remainder are output to A1 and A0, and to R2 and R0, beginning with the upper half, respectively. The zero divide information is output to the Z flag.
In this program, data for BCD calculation is loaded from the dividend 4 high-order bits at a time to create the dividend to be operated on and the divisor count can be subtracted is counted to obtain the quotient. A carry deriving from the divide operation is shifted in units of 4 bits to the next high-order digit.

Z	Meaning
0	Quotient and remainder are valid.
1	Quotient and remainder are invalid because division by zero is attempted.

Subroutine name : BCD_DIVIDE8	ROM capacity : 67 bytes
Interrupt during execution : Accepted	Number of stacks used : 3 bytes

Register/memory	Input	Output	Usage condition
R0	-	Lower half of remainder	←
R1	Lower half of divisor	Does not change	←
R2	-	Upper half of remainder	←
R3	Upper half of divisor	Does not change	←
A0	Lower half of dividend	Lower half of quotient	←
A1	Upper half of dividend	Upper half of quotient	←
CNT	-	Indeterminate	Shift count
Z flag	-	Zero divide information	←
Usage precautions	CNT is allocated in a stack area by configuring a stack frame as a temporary variable area in the program. Therefore, the value of CNT when program execution is completed is indeterminate. The dividend is destroyed as a result of program execution.		

3. Flowchart


ENTER
Initialize remainder area
Zero division?
Yes
No
Set shift count
Create shift dividend and carry 1 into next position of quotient (done in units of 4 bits because of BCD)
Count quotient
Shift dividend - divisor --> Shift divided
Subtraction succeeded?
Yes
No
Correct quotient
Shift dividend + divisor --> Shift divided
Shift count finished?
No
Yes
Division succeeded Clear Z flag
EXIT

4. The example of a reference program

```
                .include apl.inc                        ; special page include file
;****************************************************************************************
;                                                                                       *
;    R8C Program Collection No. 17                                                     *
;    CPU          : R8C/Tiny                                                            *
;                                                                                       *
;****************************************************************************************
VromTOP         .EQU        00D000H                     ; 12Kbyte Flash version
FBcnst      .EQU        001000H                     ; Assumed FB register value
;========================================================================================
;    Title: Dividing 8-digit BCD
;    Outline: Divides 8-digit BCD using registers
;    Input:    ------------------------------>  Output:
;    R0 ( )                                    R0 (Lower half of remainder)
;    R1 (Lower half of divisor)                R1 (Lower half of divisor)
;    R2 ( )                                    R2 (Upper half of remainder)
;    R3 (Upper half of divisor)                R3 (Upper half of divisor)
;    A0 (Lower half of dividend)               A0 (Lower half of quotient)
;    A1 (Upper half of dividend)               A1 (Upper half of quotient)
;    Stack amount used: 3 bytes
;    Notes: A1A0 / R3R1
;            Zero division is returned by Z flag
;========================================================================================
            .SECTION    PROGRAM,CODE                ;
            .ORG        VromTOP                     ; ROM area
            .FB         FBcnst                  ; Sets provisional FB register value
BCD_DIVIDE8:                                    ;
;-------------------------------------------------------;
;    Declaration of temporary variables                 ;
;-------------------------------------------------------;
CNT             .EQU        -1                      ; Shift count counter
    ENTER #1                                    ; Sets stack frame
    MOV.W #0,R0                                 ; Initializes remainder area
    MOV.W #0,R2                                 ;
    CMP.W #0,R1                                 ;
    JNE         BCD_DIVIDE8_10                      ;
    CMP.W #0,R3                                 ;
    JEQ         BCD_DIVIDE8exit                     ; --> Zero division
BCD_DIVIDE8_10:                                 ;
    MOV.B #8,CNT[FB]                            ; Sets number of digits to be divided
BCD_DIVIDE8_20:                                 ;
    BSET    12,R2                               ; Specifies 4-bit carry
BCD_DIVIDE8_30:                                 ;
    SHL.W #1,A0                                 ; Pushes dividend and carries 1 in quotient
    ROLC.W  A1                                  ; Pushes dividend and carries 1 in quotient
    ROLC.W  R0                                  ; Creates dividend
    ROLC.W  R2                                  ;
    JNC         BCD_DIVIDE8_30                      ; --> 4-bit carry not completed
```

```
BCD_DIVIDE8_40:                                     ;
    INC.W   A0                                  ; Quotient + 1
    DSUB.W      R1,R0                               ; Subtraction by divisor
    XCHG.W      R2,R0                               ; Moves data
    XCHG.W      R3,R1                               ;
    DSBB.W      R1,R0                               ;
    XCHG.W      R2,R0                               ; Moves data
    XCHG.W      R3,R1                               ;
    JGEU    BCD_DIVIDE8_40                          ; --> Subtraction by divisor succeeded
    DEC.W  A0                                   ; Quotient corrected
    DADD.W      R1,R0                               ; Restored to original data because divisor subtraction failed
    XCHG.W      R2,R0                               ; Moves data
    XCHG.W      R3,R1                               ;
    DADC.W      R1,R0                               ;
    XCHG.W      R2,R0                               ; Moves data
    XCHG.W      R3,R1                               ;
    ADJNZ.B     #-1,CNT[FB],BCD_DIVIDE8_20              ; --> Executes next digit
    FCLR    Z                                   ; Division succeeded
BCD_DIVIDE8exit:                                    ;
    EXITD                                       ; Clears stack frame
;                                                   ;
            .END                                    ;
```

5. Reference

SOFTWARE MANUAL
R8C/Tiny Series SOFTWARE MANUAL
(Acquire the most current version from Renesas web-site)

6. Web-site and contact for support

Renesas Web-site

http://www.renesas.com

Contact for Renesas technical support

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REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	Dec 24, 2003	-	First edition issued

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