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April 1, 2003

M32C/83 Group

16-Bit PWM Output with the Single-Phase Waveform Output Mode, Intelligent I/O Group 0 and 1

1.0 Abstract

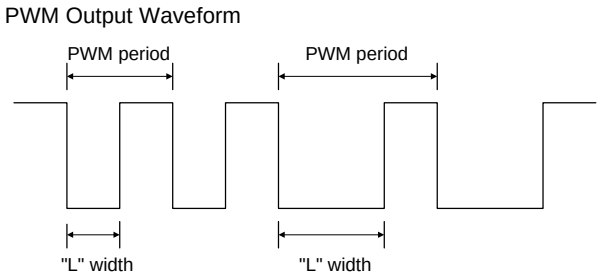
The application note shows a PWM output, variable period and duty, by using the waveform generation function of Intelligent I/O Group 0 and 1.

2.0 Introduction

The application in this document is applied to the M32C/83 Group microcomputer only.

3.0 Detailed Description

Intelligent I/O Group 0 (and also Group 1) is composed of one 16-bit Base Timer for free-run operation and eight 16-bit registers (representing Channel 0 to 7) for the time measurement and waveform generation functions. In this example, Channel 0 and Channel j (one of seven j = 1 to 7) define the period and low state of the PWM waveform respectively. The PWM waveform is output from pin OUTij when Group i and Channel j are used. When i = 0 is selected, j must be one of either j = 1,4 or 5. When i = 1, j must be one of either 1 –7.



When Group 0 is selected, up to three PWM waveform having the same period can be output. In this case, the low-state of each waveform can be controlled by each channel.

(1) Controlling the period and “low” width of the PWM

Channel 0 is used in the single-phase output mode of the waveform generation function. Base Timer is reset by matching the GiP00 register with the Base Timer. The PWM period can be obtained from:

$$\frac{1}{fBT} \times (n+2)$$

where:

n = Setting value for the GiP00 register

fBT = Clock frequency of the Base Timer

(2) “L” Width

Channel j is used in the single-phase output mode of the waveform generation function. The “L” width can be obtained from:

$$\frac{1}{fBT} \times m$$

Note: This equation is valid when the INV bit in the register GiP0CRj is set to “0” (output does not invert.)

where

m = Setting value for the GiP0j register

(3) PWM Period and ”L” width modification

The PWM period and “L” width can be modified by rewriting the GiP00 and GiPOj registers in the Channel 0 waveform generation interrupt.

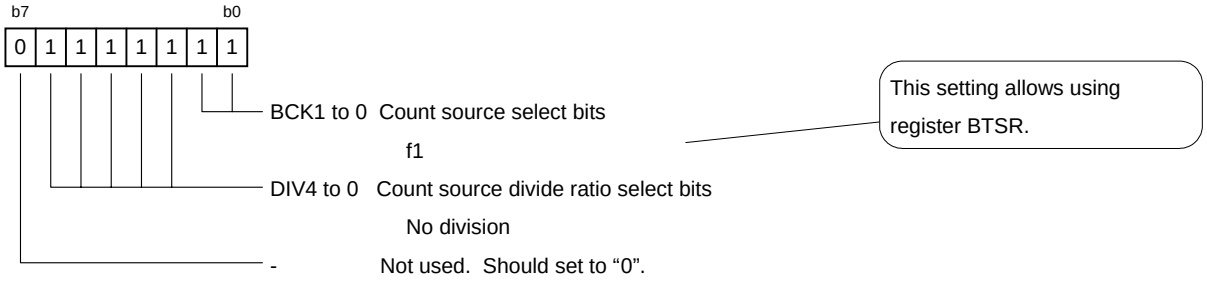
3.1 How to Set Up

This section provides setting procedures and setting values required to follow the examples in section *3.0 Detailed Description*. Refer to *the M32C/83 Group Datasheet* for more information of each register.

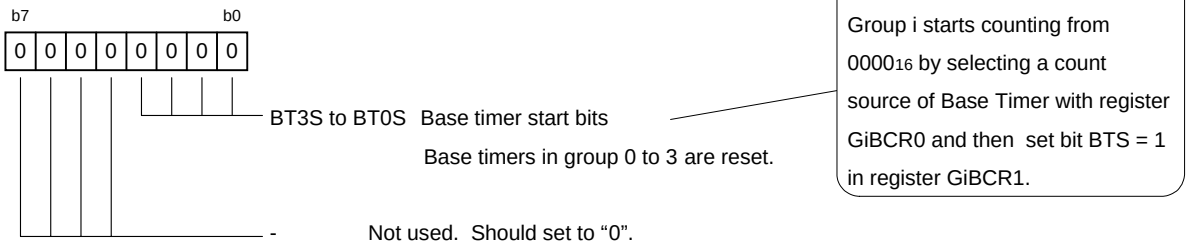
(1) Inhibiting an Interrupt

Set I flag = 0. Or set bits ILV2 -0 = 000_2 in register IIOkIC (k = 1 - 11) which the interrupt request of Intelligent I/O is assigned. Then proceed the following settings step by step.

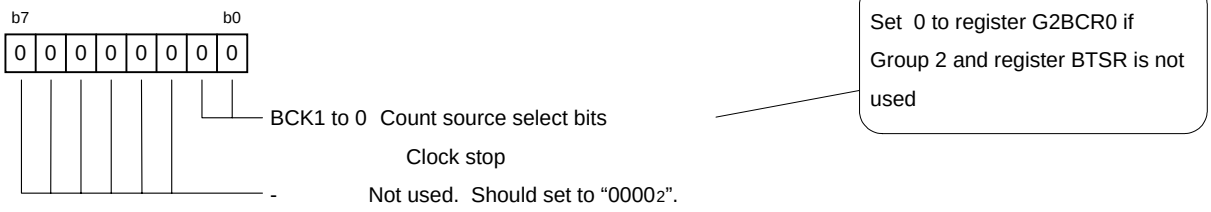
(2) G2BCR0 Register



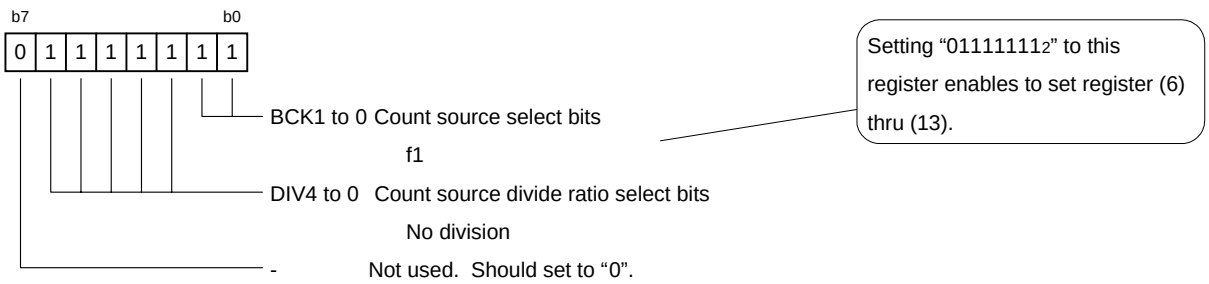
(3) BTSR Register



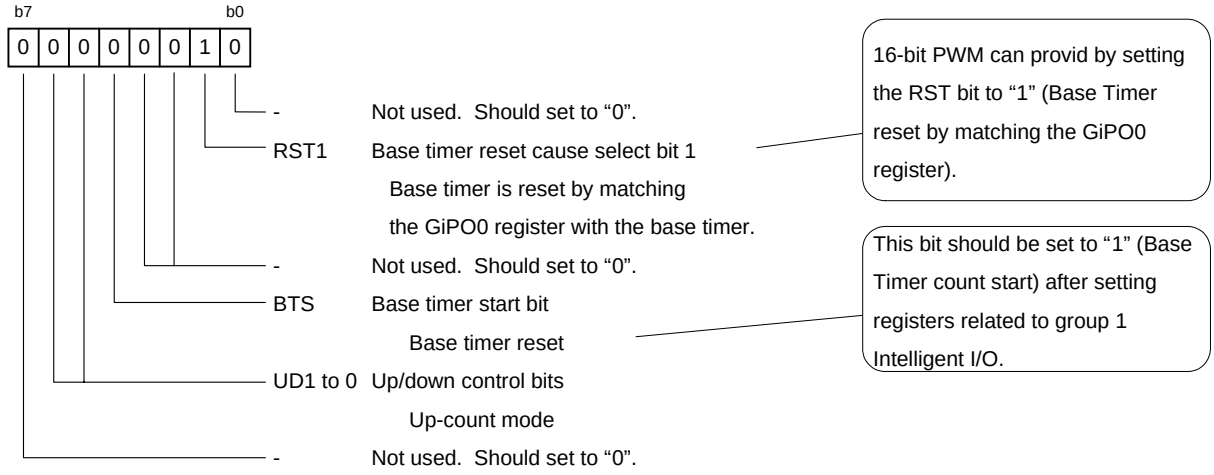
(4) G2BCR0 Register



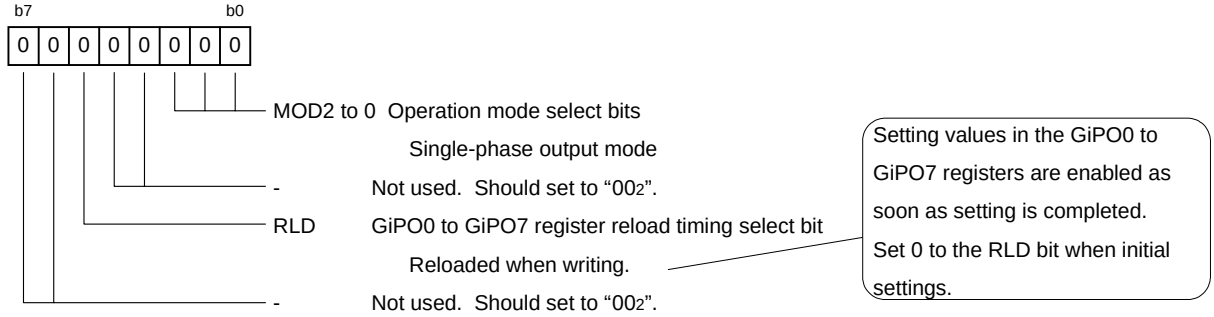
(5) GiBCR0 Register (i=0,1)



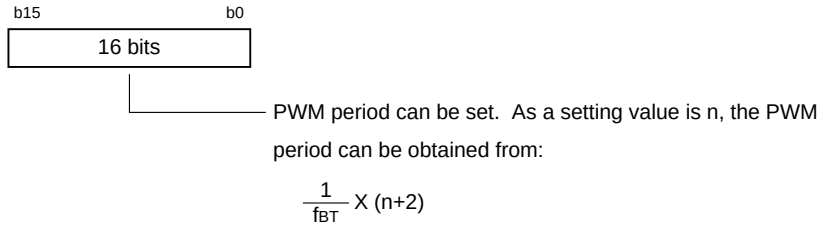
(6) GiBCR1 Register (i=0,1)



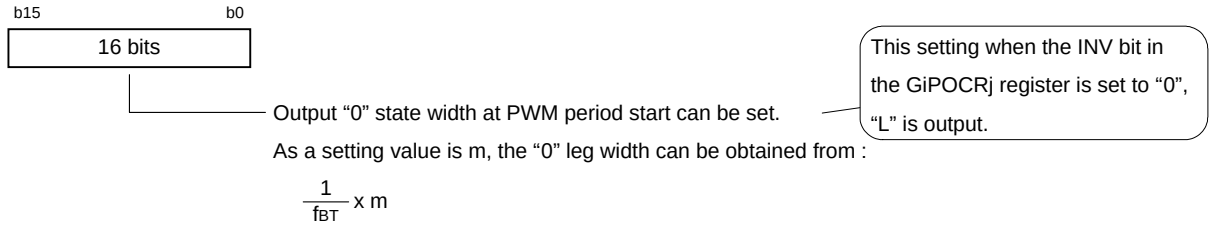
(7) GiPOCRj Registers (j=1,4,5 when i=0, j=1 to 7 when i=1)



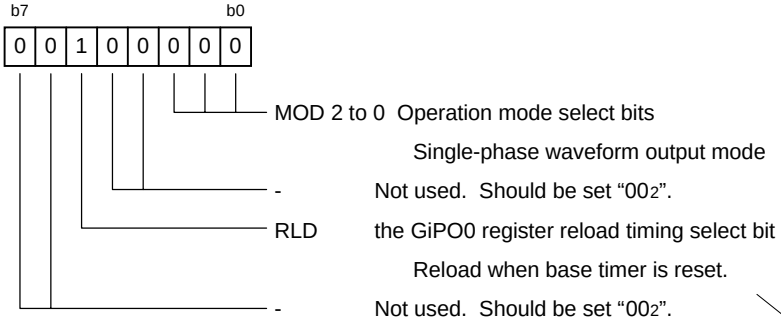
(8) GiPO0 Register (i=0,1)



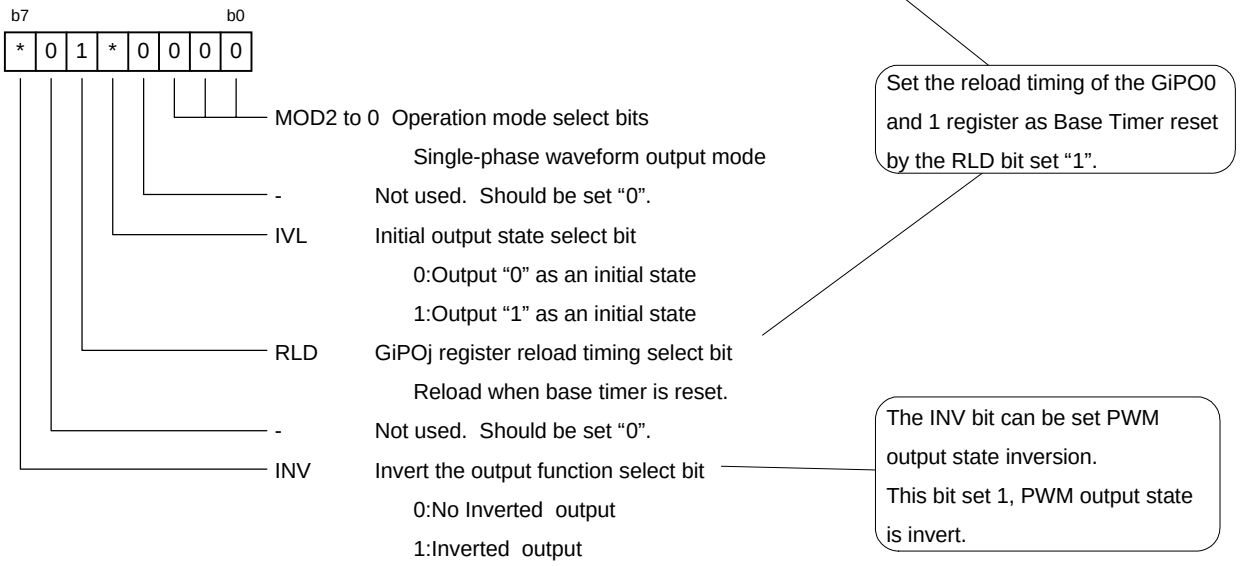
(9) GiPOj Register (j=1,4,5 when i=0, j=1 to 7 when i=1)



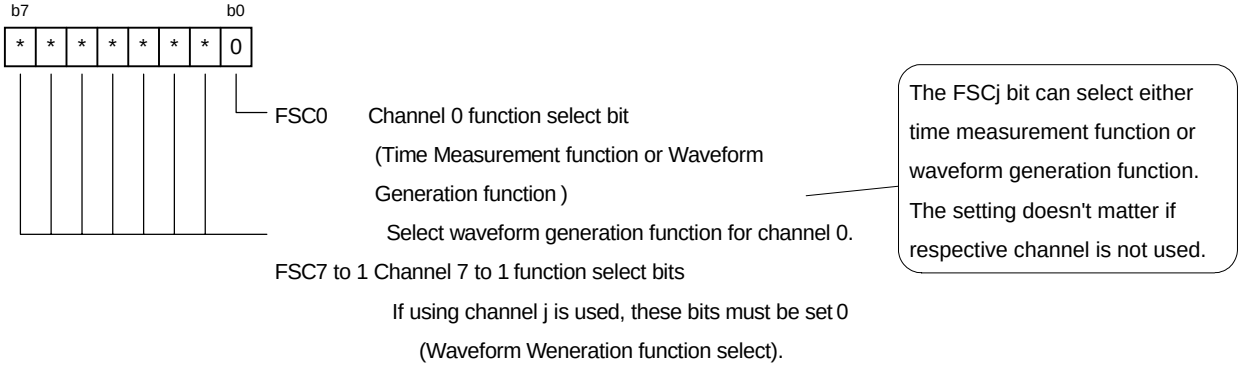
(10) GiPOCR0 Register(i=0, 1)



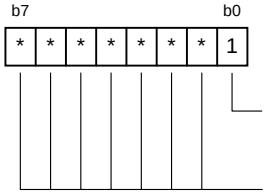
(11) GiPOCRj Register (j=1,4,5 when i=0, j=1 to 7 when i=1)



(12) GiFS Register(i=0,1)



(13) GiFE Register (i=0,1)

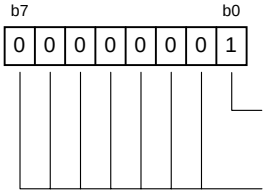


IFE0 Channel 0 function enable bit
Channel 0 function is activated.

IFE7 to 1 Channel 7 to 0 function enable bits
The IFEj bit should be set to "1" (channel j function activated) when using channel j.

Set 0 to the IFEj bit if the respective channel j is not used.

(14) IIOkIE Register (k=0 to 11)

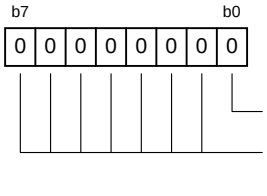


IRLT Interrupt request select bit
Interrupt request is used for an interrupt.

Bits 7 to 1 Interrupt enable bits 7 to 1
Should set to "0000000$_2$".

Do not set 1 to bit IRLT and bits 7 to 1 at the same time.

(15) IIOkIR Register (K=0 to 11)

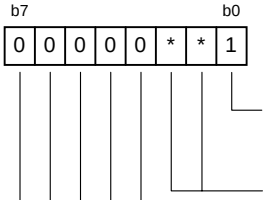


Not used. Should set to "0".

Interrupt request register is initialized.

00$_{16}$ must be set to the IIOkIR register.

(16) IIOkIE Register (k=0 to 11)



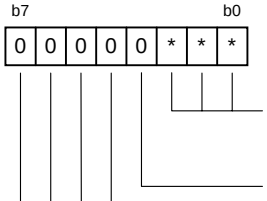
IRLT Interrupt request select bit
Interrupt request is used for an interrupt.

Bits 2 to 1 Interrupt enable bits 7 to 1
This is set the corresponding POij bit to "1".

- Not used. Should set to "00000$_2$".

Clear the interrupt request register bits of the unused interrupt by 0.

(17) IIOkIC Register (k=0 to 11)



ILVL2 to 0 Interrupt priority level select bits
Interrupt priority level can be selected.

IR Interrupt request bit
"No interrupt request" can be set.

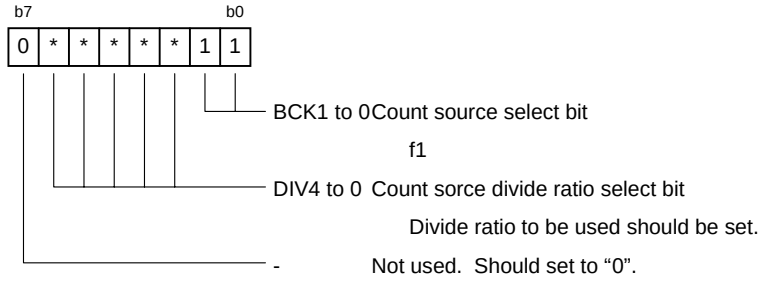
- Not used. Should set to "00000$_2$".

(18) PSC Register, PSLa(a=0 to 3) Register, PSb Register(b=0 to 9)

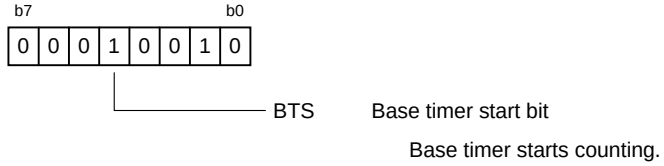
The OUTij pin function must be enable by setting these registers.

(19) Enable the Interrupt (I flag="1")

(20) GiBCR0 Register (i=0,1)



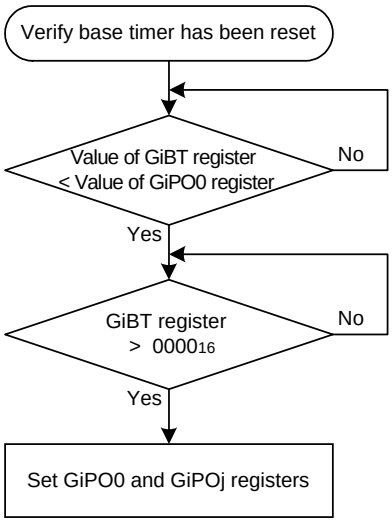
(21) GiBCR1 Register (i=0,1)



3.2 Precaution on Interrupts

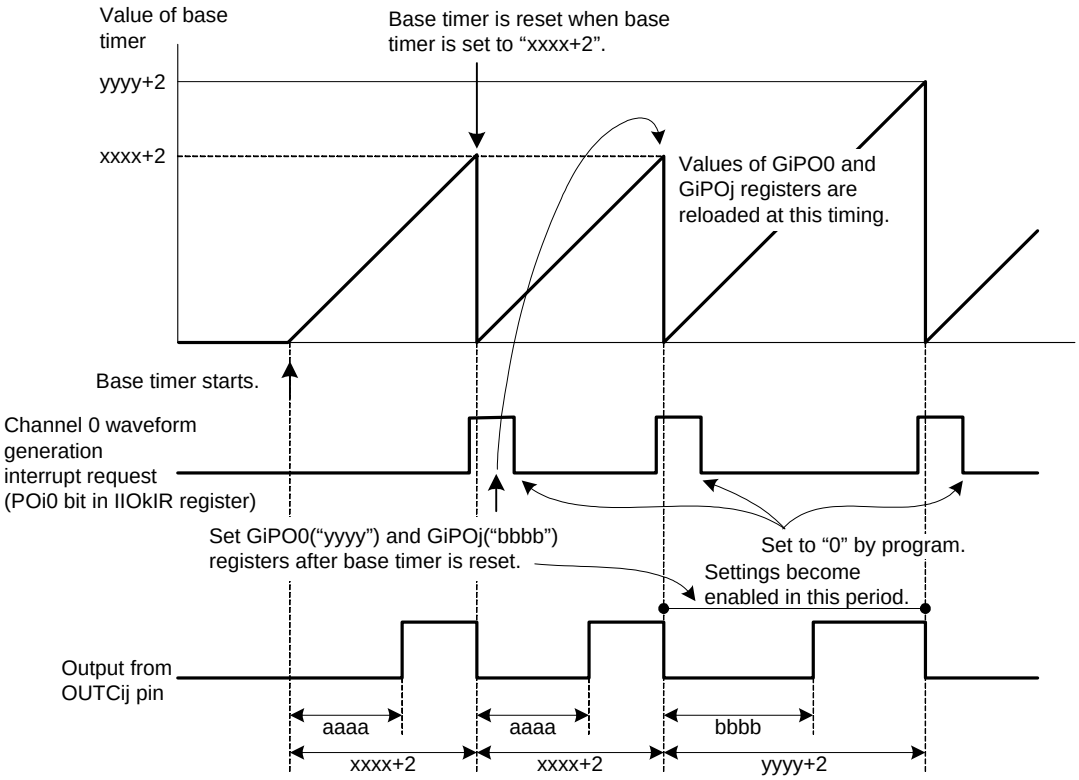
During the Intelligent I/O interrupt routine, the IIOkIR register corresponding to this interrupt should be set to "00_{16}" (initialized). If this setting is missing, the IR bit in the IIOkIC register is not set to "1" regardless of the intelligent I/O interrupt request. (No interrupt occurs.)

The GiPOO and GiPOj (j=1 to 7) registers should be set after reading the GiBT register and verifying that the Base Timer has been reset. (See the figure below.)



3.3. PWM Output Timing

The following timing diagram shows of the PWM output according to section 3.1 and 3.2.



Note: “xxxx” is an initial value of the GiPO0 register and “aaaa” is of the GiPOj register.

4.0 Sample Programming Code

```
/*****************************************************************************
/*          FILENAME: apmc_39.c                                              *
/*          Ver     : 1.00                                                   *
/*          CPU     : M32C/83                                                *
/*          FUNCTION: Intelligent I/O PWM Output                             *
/*---------------------------------------------------------------------------*
/*    Copyright (C) 2001 Mitsubishi Electric Corporation and                 *
/*    Mitsubishi Electric Semiconductor Application                          *
/*            Engineering Corporation                                        *
/*    All rights reserved.                                                   *
/*****************************************************************************/
/*          Port P7_6       : ch0
            Port P7_7       : ch1 PWM output
            Port P15_4      : ch4 PWM output
            Port P15_5      : ch5 PWM output*/
/************************************/
/*      Included file               */
/************************************/
#include <stdio.h>
#include "sfr83ver1.0.h"
/************************************/
/*      Function Difinition         */
/************************************/
void ch0_int();                         /* Interrupt function */
#pragma INTERRUPT ch0_int
void ch1_int();
#pragma INTERRUPT ch1_int
void ch4_int();
#pragma INTERRUPT ch4_int
void ch5_int();
#pragma INTERRUPT ch5_int
void main(void);                        /* main function */
/************************************/
/*      Main                        */
/************************************/
void main(){
        /* main clock set */
        prc0    = 1;                    /* Protection is off */
        mcd     = 0x12;                 /* Main clock:: no division */
        prc1    = 0;                    /* Protection is on */

        /* iio Group 0 initial set */
        g2bcr0  = 0x7f;
        btsr            = 0x00;         /* All Base Timer stops */
        g2bcr0  = 0x00;                 /* Group2 clock stops */
        g0bcr0  = 0x7f;                 /*b0,b1:    Count source: f1
                                          b2-b6:    Divide ratio of count source: no division */
        g0bcr1  = 0x02;                 /*b0:       No reset by synchronizing with Base Timer reset
                                          b1:       Reset by matching waveform generation register ch0
                                          b2:       No reset by "L " input to INT pin
                                          b4:       Base Timer stops
                                          b5,b6:    Up mode
                                          b7:       16-bit timer measurement/waveform generation functions */
```

```
        g0pocr0    = 0x00;
        g0pocr1    = 0x00;
        g0pocr4    = 0x00;
        g0pocr5    = 0x00;
        g0po0              = 1000;    /* Base Timer period */
        g0po1              = 250;     /* Ch1 period */
        g0po4              = 500;     /* Ch4 period */
        g0po5              = 750;     /* Ch5 period */
        g0pocr0    = 0x20;            /*b0-b2:    Single-phase waveform output mode
                                      b4:       Outputs “0” as an initial value
                                      b5:       Reloaded when Base Timer is reset */
        g0pocr1    = 0x20;            /*b0-b2:    Single-phase waveform output mode
                                      b4:       Outputs “0” as an initial value
                                      b5:       Reloaded when Base Timer is reset */
        g0pocr4    = 0x20;            /*b0-b2:    Single-phase waveform output mode
                                      b4:       Outputs “0” as an initial value
                                      b5:       Reloaded when Base Timer is reset */
        g0pocr5    = 0x20;            /*b0-b2:    Single-phase waveform output mode
                                      b4:       Outputs “0” as an initial value
                                      b5:       Reloaded when Base Timer is reset */
        g0fs       = 0x00;            /* Selects the waveform generation function */
        g0fe       = 0x33;            /* Operates functions in ch0, 1, 4, 5 */

        /* iio Group 0 interrupt initial set */
        /* ch0 */
        iio1ie     = 0x01;            /* Latches interrupt request */
        iio1ir     = 0x00;            /* Clears a flag for Interrupt request */
        iio1ie     = 0x03;            /* Enables corresponding interrupt from interrupt request flag */
        iio1ic     = 0x03;            /* Sets Interropt priority level */

        /* port set */
        psc        = 0x00;
        psl1       = 0x00;
        ps1        = 0x40;            /* Group 0 ch0 waveform output from P7_6 */
        ps1_7      = 1;               /* Group 0 ch1 waveform output from P7_7 */
        ps9_4      = 1;               /* Group 0 ch4 waveform output from P15_4 */
        ps9_5      = 1;               /* Group 0 ch5 waveform output from P15_5 */

        /* interrupt enable */
        _asm("fset i");

        g0bcr0     = 0x7f;            /* Divide ratio setting: no division */

        /* iio Group 0 Base Timer start */
        bts_g0bcr1 = 1;

        /* loop */
        while(1){}
}
```

```
/* interrupt */
/* --- interrupt ch0 --- */
void ch0_int()
{
        int     i;
        int     j;

        iio1ir          &= 0x00;        /* Clears interrupt request */

        do{
        }while(g0bt >= g0po0);

        do{
        }while(g0bt < 1);

        i       = g0po0;
        i       = i + 400;
        if(i >= 3000){
                i       = 1000;
        }
        g0po0           = i;            /* Changes Base Timer period */
        i =     i>>1;
        j =     i>>1;
        g0po1           = j;            /* Changes "L" width of OUTC01 output */
        g0po4           = i;            /* Changes "L" width of OUTC04 output */
        g0po5           = i + j;        /* Changes "L" width of OUTC05 output */

}

/*---------------------------------------------------------------------- End of program */
```

5.0 Example of How PWM is Output

In the below example, the PWM waveform are output from OUTC01 (P7$_7$), OUTC04 (P15$_4$) and OUTC05 (P15$_5$) pins when using the intelligent I/O Group 0.

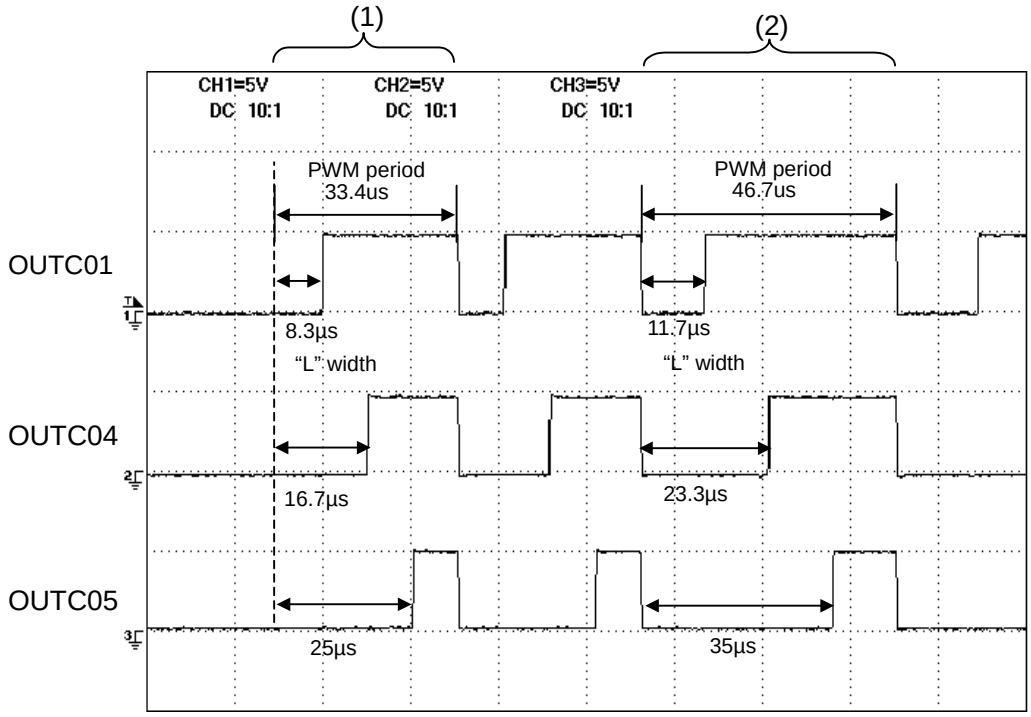
Conditions: Supply voltage = 5V

Main clock (X_{IN}) =30MHz

Base Timer operation clock (f_{BT}) = 30MHz

Item	Register	(1) in the below figure	(2) in the below figure
PWM period	G0PO0	Setting value n=1000 33.3ns × (1000+2) = 33.4µs	Setting value n=1400 33.3ns × (1400+2) =46.7µs
"L" width of OUTC01 pin output	G0PO1	Setting value m=250 33.3 ns × 250 = 8.3µs	Setting value m=350 33.3ns × 350 = 11.7µs
"L" width of OUTC04 pin output	G0PO4	Setting value m=500 33.3 ns × 500 =16.7µs	Setting value m=700 33.3ns × 700 = 23.3µs
"L" width of OUTC05 pin output	G0PO5	Setting value m=750 33.3 ns × 750 = 25.0 µs	Setting value m=1050 33.3ns × 1050 = 35.0µs

.



6.0 Reference

Data Sheet

M32C/83 Group Rev. B3

(Use the latest version on the web: http://www.infomicom.maec.co.jp/M16C/dsum/32c83dse.htm)

7.0 How to Contact Us

Mitsubishi MCU Technical Information:

http://www.infomicom.maec.co.jp/

Mitsubishi MCU Technical Support:

E-mail: support@apl.maec.co.jp

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