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Date: January 25, 2017

Introduction

Capacitance is commonly measured by forming an RC oscillating circuit using the capacitive element being measured, as shown in Figure 1. A logic inverter is used to sequentially charge and discharge the capacitor, and the oscillator's frequency is inversely proportional to the capacitance being measured. In order to measure the oscillator's frequency, the oscillator signal is fed a counter. The frequency is calculated based on the amount of time it takes to accumulate a fixed number of pulses.

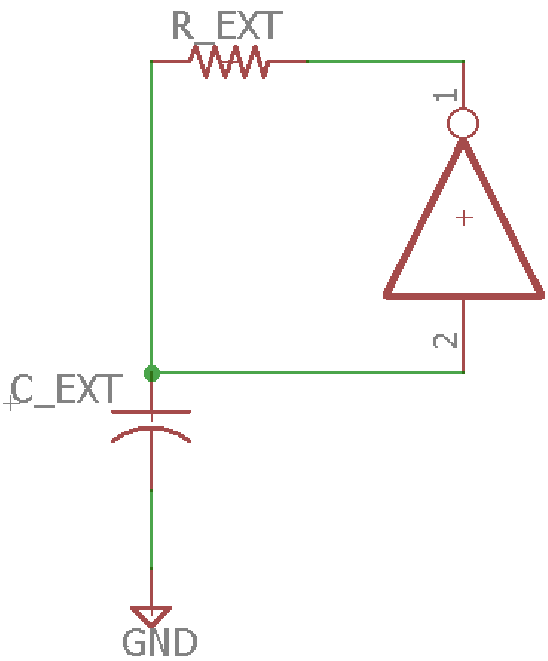

Figure 1. An RC oscillator circuit with inverter

There are limits to the range of frequencies that this arrangement can measure. The lowest measurable frequency is reached when the reference timer overflows before the pulse counter can overflow. The highest measurable frequency is reached when the reference timer ticks only once before the pulse counter overflows.

Nevertheless, since the RC oscillator frequency is also inversely proportional to the external resistance R, the range of measurable capacitance may be expanded by switching between multiple resistance values. For high capacitance, a lower value resistor can be used to keep the frequency above the lower frequency boundary. Likewise, for low capacitance, a higher value resistor can be used to keep the frequency below the upper frequency boundary. In this example case, five ranges of capacitance are implemented using five external resistors, as shown in Figure 2. Note that the inverter component could have been implemented inside the GreenPAK5; however, significant coupling between the system's input and output pins was observed, and so the capacitor voltage had to be buffered by an external inverter.

Table 1 lists the resistor values for each measurement range. For the most part, they are separated by a factor of 10. This ratio can be increased to widen the measurement ranges. Practically speaking, the lower limit on the resistor values is determined by the maximum current on each of the GreenPAK IC's output pins, and the upper limit on the resistor values is determined by the capacitor leakage current and inverter gate input leakage current.

Resistor	Value
R0	470Ω
R1	10kΩ
R2	100kΩ
R3	1MΩ
R4	10MΩ

Table 1. Resistor values used for each range of capacitance

Capacitance measurements can be resource-intensive for a microcontroller.

A counter is needed to accumulate pulses from the RC oscillator, and a reference timer is needed to measure the time needed to accumulate pulses. GPIO pins are required to manage the various external resistors used to implement multiple measurement ranges. The counter must be polled (or interrupt routines must be used) to catch the moment of its overflow. Using a GreenPAK IC can free all of these resources and automate all of the multi-range functionality.

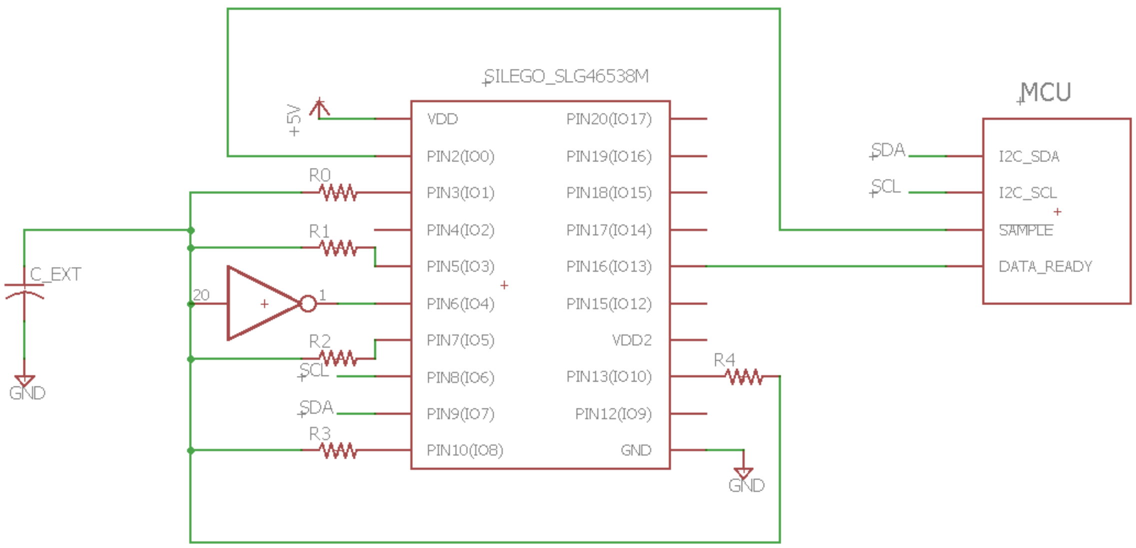

Figure 2. The RC oscillator with 5 ranges implemented with the GreenPAK SLG46538M

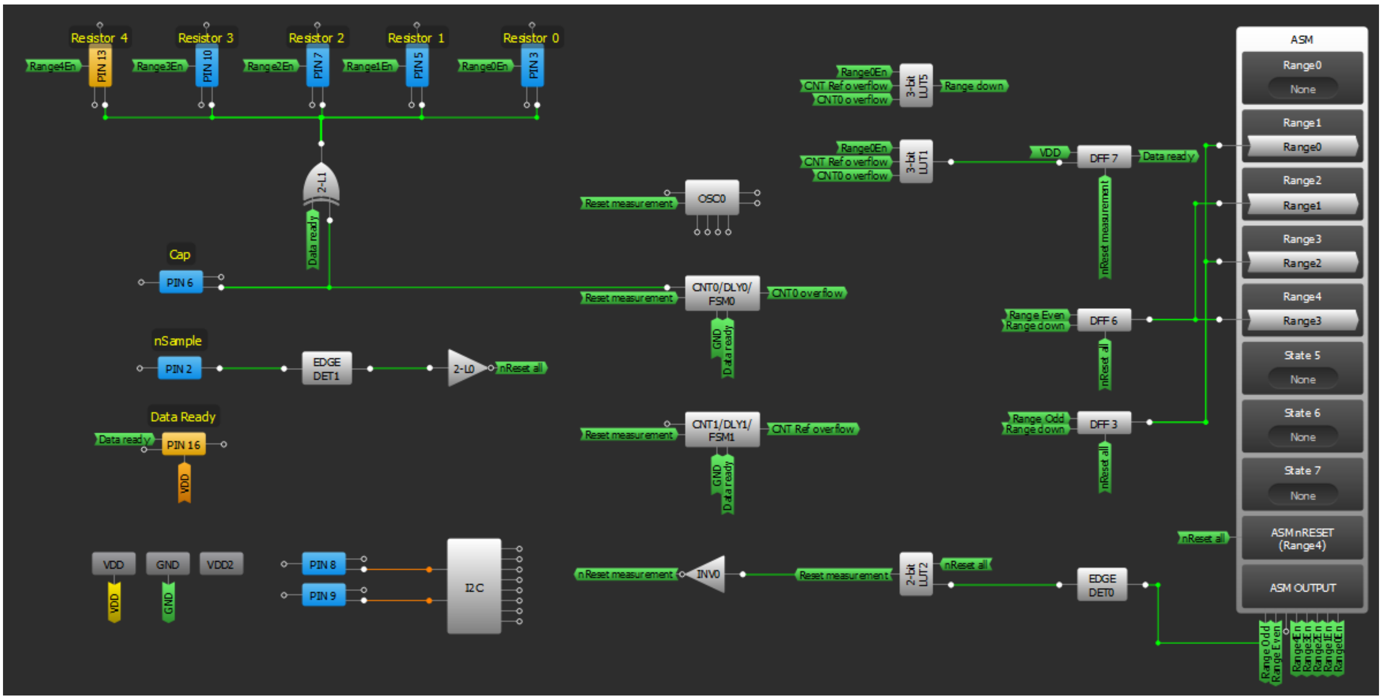

Figure 3. GreenPAK5 internal connections

Autoranging/Measurement Circuit

Figure 3 depicts the capacitance measurement and auto-ranging logic implemented inside the GreenPAK IC. At the heart of the internal circuitry are two counters: CNT_0, and CNT_1. CNT_0 is clocked by the external RC oscillator and accumulates *N* pulses before overflowing. CNT_1 is clocked by OSC_0 and increments at a fixed frequency (3.125kHz). Ideally, during a measurement, CNT_0 would overflow first, freezing CNT_1, whose contents could be read over the I2C bus and then used to calculate the external RC oscillator's frequency. If CNT_1 overflows before CNT_0, then the frequency of the external RC oscillator is too slow and may be increased by switching to a lower value resistor.

The asynchronous state machine is used to keep track of which resistor is being used in the external RC oscillator and activates/deactivates the appropriate GPIOs used to drive this oscillator. As shown in Figure 4 below, there are five states used, one for each measurement range. Each state activates an output pin corresponding to a different external resistor.

Flip flop DFF_7 is set when a valid measurement is taken. This is determined by 3-bit LUT_1, which monitors when CNT_0 overflows before CNT_1. DFF_7's output, "Data ready," freezes counters CNT_0 and CNT_1 as well as sets pin 16 to signal the microcontroller that measurement is complete. 3-bit LUT_5 monitors when CNT_1 overflows before CNT_0 and sets the signal "Range down." This signal is fed to the ASM to decrement the range/resistor selected.

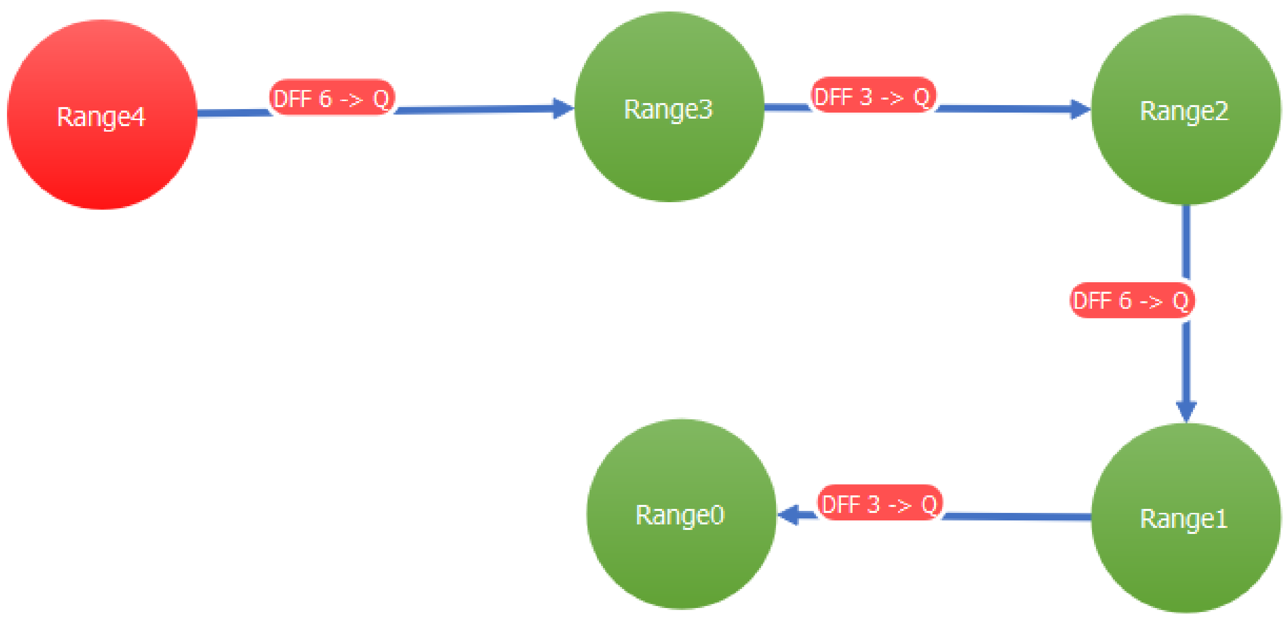

Figure 4. ASM state diagram

Without flip flops DFF_3 and DFF_6, the ASM could not be directly triggered by the signal "Range down" because the ASM is asynchronously level-triggered, not edge triggered. A digital high on "Range down" would sequentially trigger the transition from one range to another until the lowest range is reached. For example, when Range 4 decrements to Range 3, nothing will prevent the ASM from continuing to decrement the range all the way down to Range 0, since the "Range down" signal is still high. With DFF_3 and DFF_6, a positive edge on "Range down" triggers only a single transition from an even-numbered range to an odd-numbered range or vice-versa. No consecutive states share a common transition signal, since there is one signal for the odd states (DFF_3's output) and one signal for the even states (DFF_6's output).

Here is the sequence of events that occurs during a measurement:

- A negative edge is externally applied to pin 2, which momentarily brings the "nReset all" signal low, the "Reset measurement" signal high, and the "nReset measurement" signal low.
- This resets the ASM, CNT_0, CNT_1, DFF_7, DFF_3, DFF_6, and OSC_0. The ASM starts out in the "Range 4" state.
- "Data ready" goes low.
- With "Data ready" low, the 2-bit LUT_1 turns on the external RC oscillator.
- The counters begin to increment.
- If CNT_0 overflows before CNT_1:
  - A positive edge from 3-bit LUT_1 clocks DFF_7, setting the "Data ready" signal.
  - The "Data ready" signal freezes CNT_0 and CNT_1 and sets output pin 16 high to notify the microcontroller that data is available on the I2C bus.
  - The microcontroller can read the contents of CNT_1 and the current state of the ASM at any time after pin 16 is set.
- If CNT_1 overflows before CNT_0:
  - A positive edge from 3-bit LUT_5 clocks DFF_3 and DFF_6, which cause the ASM to change state and decrement the measurement range.
  - The ASM sets or resets the "Range odd" signal, and edge detect EDGE DET_0 momentarily activates the signal "Reset measurement," which resets counter CNT_0 and CNT_1.
- If CNT_1 overflows before CNT_0, and the ASM is in the state "Range 0":
  - A positive edge from 3-bit LUT_1 clocks DFF_7 as if a valid measurement was made, setting the "Data ready" signal.
  - As in the case when CNT_0 overflows before CNT_1, the "Data ready" signal freezes CNT_0 and CNT_1 and sets output pin 16 high to notify the microcontroller that data is available on the I2C bus.
  - The microcontroller can read the contents of CNT_1 and the current state of the ASM at any time after pin 16 is set.

Design Equations

The frequency of the external RC oscillator is determined by the resistor and capacitance, but also by the digital high/low thresholds. If a Schmitt trigger is used on the external inverter, then the frequency can be derived as:

$$I_{Cap} = C_{ext}\frac{dV_{Cap}}{dt} = \frac{V_{Cap}}{R_{ext}}$$

$$\frac{dV_{Cap}}{dt} = \frac{V_{Cap}}{C_{ext}R_{ext}} \quad \rightarrow \quad \frac{\Delta V_{Cap}}{\Delta t} \approx \frac{V_{Cap,avg}}{R_{ext}C_{ext}}$$

Δ Vcap = Net voltage change during one RC oscillator tick = 2 * digital high/low voltage gap

Δ t = Period of the RC oscillator

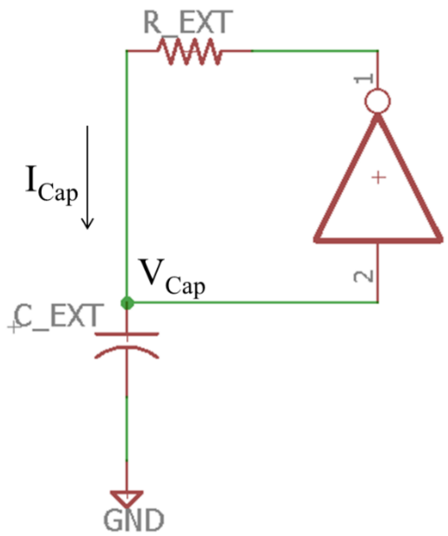

Figure 5. External RC oscillator, with capacitor current and voltage indicated

$$f_{RC} = \frac{1}{\Delta t} \approx \frac{V_{Cap,avg}}{\Delta V_{Cap} R_{ext} C_{ext}} = \frac{V_{DD}/2}{2\left(V_{Schmitt,high} - V_{Schmitt,low}\right) R_{ext} C_{ext}} = \frac{K}{R_{ext} C_{ext}}$$

f_{RC} = RC oscillator frequency

R_{ext} = RC resistor value

C_{ext} = RC capacitance value, the capacitance being measured

$V_{Schmitt,high}$ = Schmitt trigger digital high threshold

$V_{Schmitt,low}$ = Schmitt trigger digital low threshold

$V_{cap,avg}$ = Average capacitor voltage = V_{DD} / 2

K = proportionality constant = $\frac{V_{Cap,avg}}{2\left(V_{Schmitt,high} - V_{Schmitt,low}\right)}$

The relationship between the external capacitance to the CNT1 counted value is:

$$\frac{X_{CNT1}}{N_{CNT1}} = \frac{f_{CNT1}}{f_{RC}} \rightarrow X_{CNT1} = f_{CNT1} N_{CNT0} \frac{R_{ext} C_{ext}}{K}$$

X_{CNT1} = CNT_1 counted value accumulated during one period of CNT_0 + 1

f_{CNT1} = CNT_1 tick frequency = 3.124kHz

N_{CNT0} = CNT_0 maximum value (overflow/modulo value) + 1

The maximum capacitance measurable by any given range is:

$$C_{ext,max} = \frac{N_{CNT1} K}{N_{CNT0} f_{CNT1} R_{ext}}$$

$C_{ext,max}$ = maximum capacitance measurable by a range with external resistance R_{ext}

N_{CNT1} = CNT_1 maximum value (overflow value) + 1

Since $C_{ext,max}$ is proportional to N_{CNT1}, higher values of N_{CNT1} mean that higher capacitances can be measured. However, there is a tradeoff between higher measurable capacitance values and longer measurement acquisition times. Since the circuit starts out in the lowest of five capacitance ranges, CNT_1 must overflow four times to reach the highest measurement range, which means that the longest possible measurement acquisition time is:

$$t_{max} = (5\ ranges) \times \frac{N_{CNT1}}{f_{CNT1}}$$

$C_{ext,max}$ is inversely proportional to N_{CNT0}, which means that minimizing N_{CNT0} will increase the maximum measurable capacitance. However, jitter in the RC oscillator frequency means that a smaller group of ticks will have a greater percentage of variability than a larger group of ticks.

This is compounded by the fact that at the beginning of the measurement, the state of charge of the capacitor is unknown, making the length of the first tick variable (though the longer the time between measurements, the closer the capacitor voltage will be to 0V or V_{DD}). Overall, this means that accuracy is improved by increasing N_{CNT0}.

Finally, $C_{ext,max}$ is also bounded by the maximum capacitor charge/discharge current. The output pins of the SLG46538M can source at least 41mA and sink at least 14mA. Therefore, the highest frequency external resistor should not have a value below 5V/14mA = 360Ω.

Table 2 gives the maximum capacitance values measurable by each range.

Range	R_{ext}	$C_{ext,max}$
0	470Ω	130µF
1	10kΩ	6µF
2	100kΩ	600nF
3	1MΩ	60nF
4	10MΩ	6nF

Table 2: maximum capacitance measurable by each range

$V_{Schmitt,max}$ = 4.64, $V_{Schmitt,min}$ = 2.00, K = 0.47, N_{CNT1} = 3125, N_{CNT0} = 9

Measurement time = 1s/range

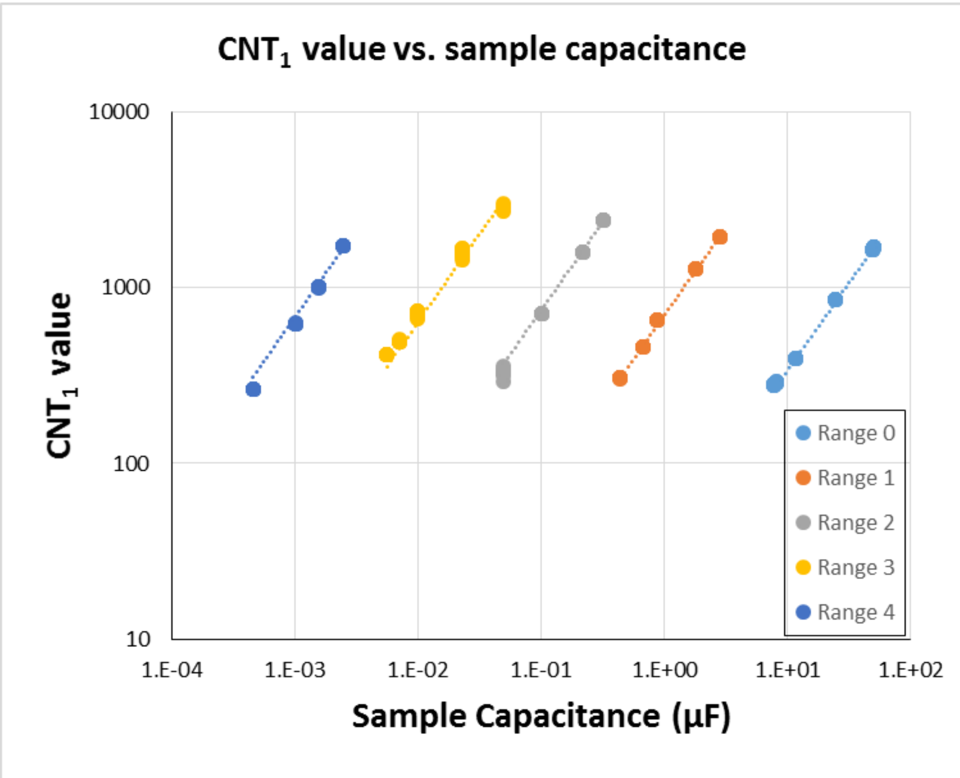

Figure 6. Autoranging capacitance meter test results

Results

Various discrete capacitors were measured using a multimeter and using the GreenPAK5 circuit. Figure 6 shows a graph of CNT_1 contents versus measured capacitance for each range. As expected, each range shows a linear relationship between the CNT_1 value and measured external capacitance.

For the microcontroller, measuring capacitance with this circuit is as simple as reading the contents of CNT_1 (registers 0xEE and 0xEF) and the states of the ASM outputs (register 0xF5) over the I2C bus. Given the states of the ASM outputs, the measurement range can be deduced, since the ASM outputs activate the pins connected to the external resistors.

Once the range and CNT_1 value are known, the capacitance can be calculated using the linear relationships depicted in Figure 5.

If the measurement range needs to be expanded, the microcontroller can change N_{CNT0} and N_{CNT1} (the maximum/overflow values of CNT_0 and CNT_1) by writing to registers 0xC5 through 0xC6 for CNT_0 and registers 0xC7 through 0xC8 for CNT_1.

Conclusion

This application note has demonstrated how to configure a GreenPAK5 mixed signal IC to build an auto-ranging capacitance meter. This frees several of the microcontroller’s resources, including several GPIO pins, a counter, a timer, compute cycles, and possibly some interrupt routines. It makes capacitance measurement as simple as reading values over an I2C bus.

Appendix A

2-bit LUT2/DFF/LATCH2

Type: LUT

IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1

2-bit LUT2 properties

3-bit LUT1/DFF/LATCH4

Type: LUT

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1

3-bit LUT1 properties

3-bit LUT5/8-bit CNT2/DLY2

Type: LUT

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

3-bit LUT5 properties

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