AN-1144



I2C IO Controllers 8-bit BUS

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Introduction

This app note is a corollary to another app note **AN-1090 Simple I2C IO Controllers with SLG46531V**. AN-1090 explains how to make I2C IO Controllers with separate input and output pins. However, this app note will explain how to setup an 8-bit bus controller which combines input pins with output pins. Refer to Figure 1 for the System Level View.

Digital Input/Output and OE

To combine inputs with outputs, each pin interfacing the bus is set to 'Digital Input/Output'. Only 9 GPIOs in the SLG46531V are 'Digital Input/Output' capable and we will be using 8 of those pins: PINs #19, 18, 16, 14, 13, 7, 5, 3. Each of these pins have an OE signal that toggles the mode. Set the properties as shown in Figure 3 and setup the matrix connections as shown in Figure 2.

Each output signal is controlled by an I2C Virtual Input. OE is controlled by 2-bit LUT0. The inputs to the 2-bit LUT0 are both gnd. Therefore, if the LUT is configured as in Figure 4a, then OE will be logic 1. If the LUT is configured as in Figure 4b, then OE will be logic 0. We will be using I2C to change the LUT configuration on the fly.

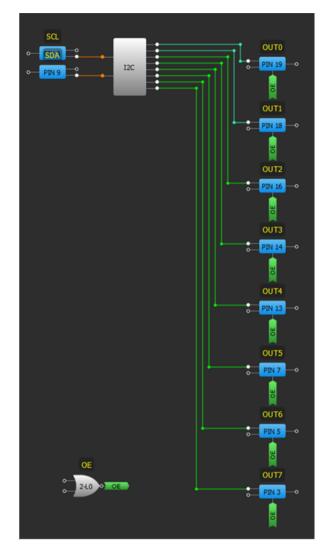


Figure 2. GreenPAK Design

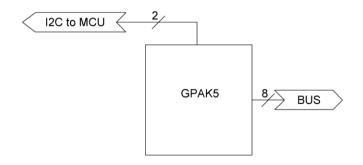


Figure 1. System Level View

I2C IO Controllers 8-bit BUS



Properties				×				
	P	PIN	19					
I/O select	ion:	Digital input/output 💌						
Input mod OE = 0	de:	Digital in without Sd 💌						
Output mode: OE = 1			1x open drain NMO! 💌					
Resistor:		FI	oating	Ŧ				
Resistor v	value:	F	oating	-				
	Info	rn	nation					
Electrical Spe	ecificatio	ns						
	1.8 V min/ma		5.0 V min/max					
V_IH (V)	1.060/	-	1.810/-	2.680/-				
V_IL (V)	-/0.760)	-/1.310	-/1.960				
V_OL (V)	-/0.009)	-/0.150	-/0.160				
I_OL (mA)	1.380/	-	7.310/-	10.820/-				
-	-/-		-/-	-/-				
-	-/-		-/-	-/-				
0 1		6	Ap	ply				

Figure 3. PIN Configuration

IN1	IN0	OUT
0	0	1
0	1	0
1	0	0
1	1	0

IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	0

Figure 4a. OE = 1

Figure 4b. OE =0

I2C Bus Write

To write the bus, the MCU must send 2 commands: first write to the I2C Virtual Inputs, then set OE = 1 by re-configuring 2-bit LUTO:

i) **W: I2C Virtual Inputs**, write to address 0xF4. Each bit corresponds to an I2C Virtual Input. The order from left to right is PINs #19, 18, 16, 14, 13, 7, 5 and 3.

0xF4	0	0	0	0	0	0	0	0
0xF4	1	1	1	1	1	1	1	1

ii) **W: 2-bit LUT0**, write to the second nibble of address 0x96 with the byte value 0x8. To mask the first nibble, read the byte and change only the latter four bits.

0x96	Х	Х	Х	Х	1	0	0	0
------	---	---	---	---	---	---	---	---

I2C Bus Read

To read from the bus, the MCU must send 2 commands: first set OE = 0 by reconfiguring 2-bit LUT0, then read from the GPIO Input Levels.

i) **W: 2-bit LUT0**, write to the second nibble of address 0x96 with the byte value 0x0. To mask the first nibble, read the byte and change only the latter four bits.

0x96	Х	Х	Х	Х	0	0	0	0	
------	---	---	---	---	---	---	---	---	--

ii) **R: Input levels**, read from address $0 \times F0$ and $0 \times F6$ the input levels of PIN#3, 5, 7 and PIN#13, 14, 16, 18, 19 respectively. Then parse the data based on bit location.

0XF0 X X	PIN3	Х	PIN5	Х	PIN7	Х
----------	------	---	------	---	------	---

0XF6	х	PIN13	PIN14	х	PIN16	0	PIN18	PIN19





Warning

The following warning can be ignored because 2bit LUT0 inputs are intentionally left static and the truth table will be re-configured through I2C.

Examples I2C Commands

The output of each example is shown in Figure 7 through 10, which are screenshots from the I2C Tool.

Time	Event	Rule	Note
14:27:21	🕕 Fail	2-bit LUT0/DFF/LATCH0: The truth table is configured incorrectly.	The truth table is configured so that all combinations of the inputs that are connected to the blocks, do not cause changes on the output.
14:27:21	🚸 Warning	2-bit LUT0/DFF/LATCH0: No input connected.	2-bit LUT0/DFF/LATCH0's input is not connected.

Figure 5. Warnings and Rules Checker

Emulation

Each Digital IO pin has a pull-up active-low button. Enable I2C Tools after Emulation.

<u>Syntax</u>: [is the start bit,] is the stop bit, and **SA** is the slave address with a r/w bit.

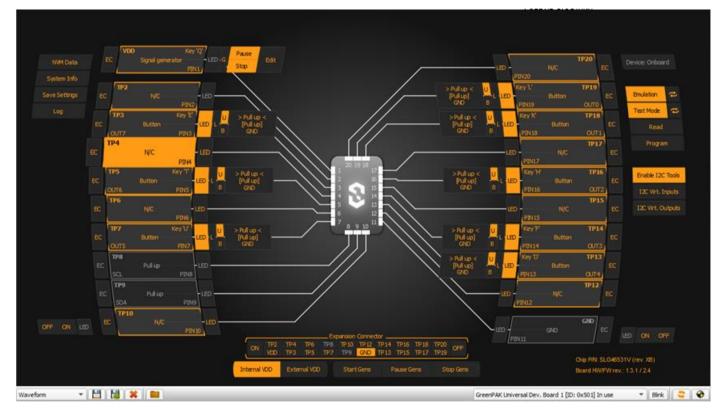


Figure 6. Emulator Configuration

I2C IO Controllers 8-bit BUS



i) I2C write to I2C Virtual Inputs the logic 0, 0, 0, 1, 0, 1, 1, 1.

[SA 0xF4, 0xE8 **]**

ii) I2C write 2-bit LUT0 configuration to 1, 0, 0, 0:

[SA 0x96 0x08 **]**

iii) I2C write 2-bit LUT0 configuration to 0, 0, 0, 0:

[SA 0x96 0x00 **]**

iv) I2C Read the input levels from PINs #7, 5 and 3 and also #19, 18, 16, 14 and 13:

[SA 0xF0 [0xSA read]

I2C Virt	tual Inputs		•	[14:29:57]: Read (device: 0x00) Address, hex Data, hex
	Outputs	Current value	New value	0xF4 0x00 [14:30:42]: Write (device: 0x00)
1	OUTO	0	0	Address, hex Data, hex 0xF4 0xE8
2	OUT1	0	0	
3	OUT2	0	0	
4	OUT3	1	1	
5	OUT4	0	0	
6	OUT5	1	1	
7	OUT6	1	1	
8	OUT7	1	1	

Figure 7. Example i

120		intua	Inputs									-	-			?	
oose	the	compone	ent:									Lo	g				
Reg	jister	s		-			12	2C	Virtua	l Inp	uts: ?)	X	2	xE9 xEA xEB	0x00 0x00 0x00 0x00	-
R	w	Byte, hex	Registers	c	Г	_	_	_							xEC xED xEE	0x00 0x00 0x00	
		0x94	[1191:1184]			F	2	W	Register	CL	irrent value	Nev	v value		XEF	0x00	
		0x95	[1199:1192]						1201		0		0		xF0 xF1	0x00 0x01	
		0x96	[1207:1200]	1					1202		0		0		xF2	0x00	
		0x97	[1215:1208]						1203		0		0		xF3 xF4	0x00 0xE8	
		0x98	[1223:1216]						1204		1		1		xF5 xF6	0x01 0x00	
		0x99	[1231:1224]						1205		0		0		xF0 xF7	0x00	
		0x9A	[1239:1232]						1206		0		0		xF8 xF9	0x9F 0x92	
		0x9B	[1247:1240]	1					1207		0		0	-	xFA	0x22	
		0x9C	[1255:1248]												xFB xFC	0x5A 0x1E	
		0x9D	[1263:1256]	1							OK		Cancel		xFD	0x0F	
		0x9E	[1271:1264]		L	-		_	-			_	_		xFE	0x00 0xA5	-
	_		Read		_		_	_		Write					Clear	•	





v) I2C write 2-bit LUT0 configuration to 0, 0, 0, 0:

[SA 0x96 0x00 **]**

vi) I2C Read the input levels from PINs #7, 5 and 3 and also #19, 18, 16, 14 and 13:

[SA 0xF0 [0xSA read]

[**SA** 0xF6 [0xSA read]

Conclusion

By the end of this app note, you should be able to make a GreenPAK Design and the I2C Commands. Unlike AN-1090, this design uses less GPIOs at the expense of more I2C commands.

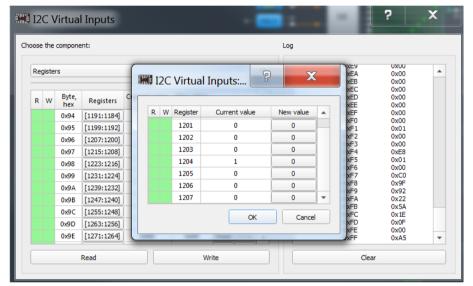


Figure 9. Example iii

er		ID	Block	Pin	Level
		2	PIN 3	OUT	1
PIN 16	^	4	PIN 5	OUT	1
PIN 17		6	PIN 7	OUT	1
Crystal OSC		49	PIN 13	OUT	1
V PIN 18		50	PIN 14	OUT	1
 PIN 19 		52	PIN 16	OUT	1
PIN 20		54	PIN 18	OUT	1
A CMP0		55	PIN 19	OUT	1
A CMP1					
A CMP2					
A CMP3					
P DLY					
POR					
VDD (PIN 1)	-	Last U	pdate: 14:56:47		

Figure 10. Example iv

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