GreenPAK Macro Circuit Design: Failsafe Watchdog

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Date: May 30, 2014

Introduction

The stability of the power supply voltage is an important factor in microprocessor based systems. With instability, the best case means a restart of the system is possible. But at worst case it may mean a failure/malfunction of the program that may cause some unexpected outcome. As a result, many manufacturers employ shutdown in their microcontrollers. There still are cases when that may be not enough. As a solution, there are specific IC's that can control the power supply and restart a system if necessary.

The H6006 (produced by EM Microelectronic-Marin SA) is an example of such an IC. It ensures the function of its' own power supply monitoring, microcontroller power supply monitoring (or input power stabilizer) and a "watch dog" function if necessary. Since the new version H6006 omits the "watch dog" function, there is need for an updated and full featured replacement. In the original H6006 datasheet one finds its functional schematic contains 4 comparator units.

In the process of this project development, the use of only two analog comparator units was achieved that allowed using a SLG46110V, and substantially decrease the cost of the final product. Moreover, significant power savings were achieved during this improvement.

H6006 chip review

Let's start the project review from the diagrams of the H6006 IC's operation. The convention and symbols used are shown in the Fig.1.

In Fig.2 we see the diagram of the IC function relative to the power supply, which is the similar to the diagram shown in the H6006 IC datasheet.

Here we see two thresholds: The first threshold – POR_LH, enables the IC functions when it is greater than 1.4V - 1.5V. The second threshold – POR_HL, disables the IC when it is less than 0.6V - 0.8V. As seen in the diagram, the power voltage level between those two thresholds does not cause disabling of IC functions.

The diagram of the microcontroller power supply monitoring behavior is shown in Fig.3. Three signals are important here. The first of them – VIN, is a signal which is being monitored. nSAVE and nRES – are signals of the system in response to the VIN signal changes. As can be seen in the diagram, there are three thresholds as part of VIN monitoring. VSH is a threshold of the VIN signal, and after it is reached, nSAVE output is set HIGH. After passing TO_time, the signal nRES is set to a HIGH level. After the voltage has fallen to the VSL level, the signal nSAVE is set LOW, which allows using it to dump the microcontroller settings and data before it restarts. Similarly, the signal nRES is set LOW when the voltage is decreased below the VRL level. It halts the microcontroller until the next HIGH level on the nRES output, as further operation with the low voltage may cause unexpected microcontroller outcomes. If the voltage decreases only to VSL level and does not drop lower than VRL, then only nSAVE signal is set LOW.

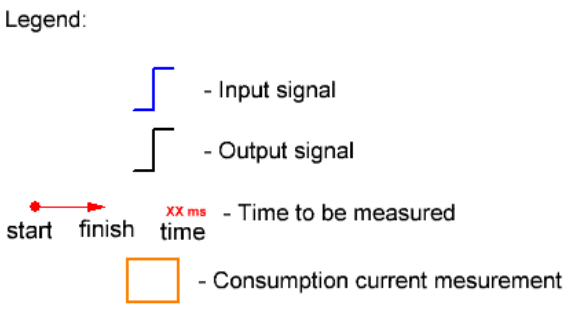

Figure 1. Convention and symbols

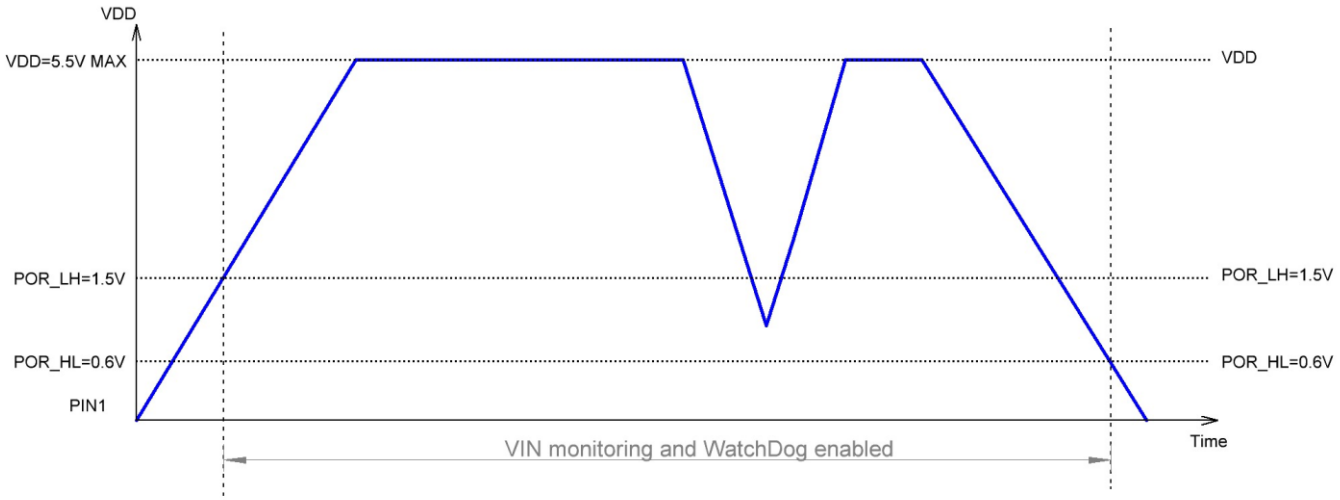

Figure 2. IC function relative to the power supply

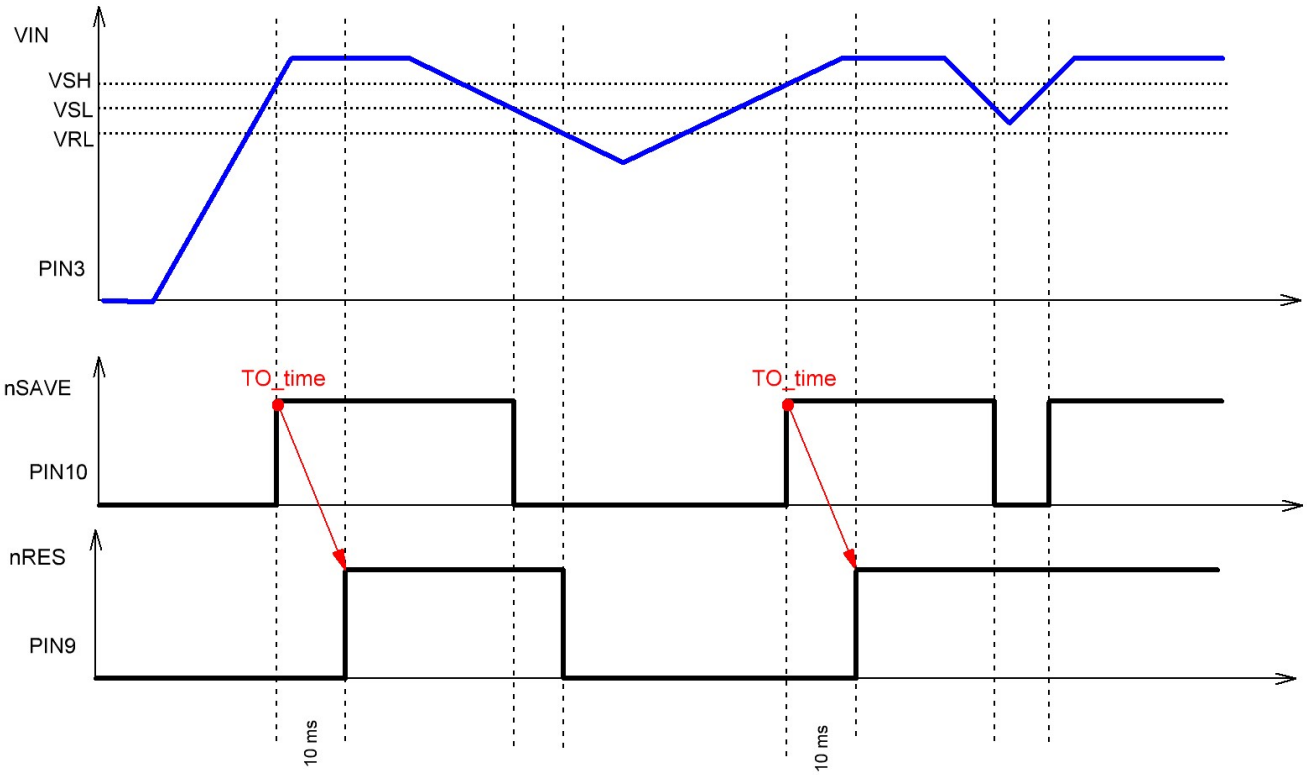

Figure 3. VIN monitoring

The diagram for the Watchdog function is presented in Fig.4. There are three signals: nTCL – input signal that conducts the operation of the Watchdog. For the system function in a normal mode, a falling edge should be asserted to this input with the maximum TO_time period (10 ms). In case a falling edge was not asserted during that time, it warns about an error in the operation of the microcontroller program and the output nTO is set LOW. If from the moment of the last falling edge being generated 2x TO_time pass (which is 20ms) the edge does not appear once more, then the nRES signal is set LOW.

Simultaneously, an nTO signal is set HIGH for TO_time.

The combined diagram for VIN Monitoring and Watchdog timer is presented in Fig.5.

As can be seen, after the threshold VSH on the input VIN is passed, the signal on the nSAVE output is set HIGH, and after the TO_time the nRES signal is also set HIGH. After TO_time from the moment that nRES was set HIGH, the nTO signal is set LOW (such dependence of nTO from nRES is observed only once after the VSH threshold on the VIN input is reached). If during 2x TO_time falling edge on the nTCL the input does not appear, then the nRES is set LOW making the level of the signal nTO HIGH for TO_time. When the falling edge arrives at the nTCL input, nRES and nTO signals immediately are set HIGH for 2TO_time and TO-time accordingly. But the falling edge on the nTCl postpones the switching LOW of these signals for the corresponding time.

If the nRES signal is LOW because of VIN Monitoring, then nTO is HIGH regardless other signals (see diagram).

Circuit Design

We have just reviewed diagrams similar to the H6006 IC operation to get acquainted with this overall objective. Now let's translate this design objective to the SLG46110V IC.

The project design is shown in Fig.6. The first function is VDD Monitoring. This is implemented by the POR cell, which already contains built-in circuitry to control most of the IC elements. Additionally, two comparators and nSAVE output were connected to the POR cell.

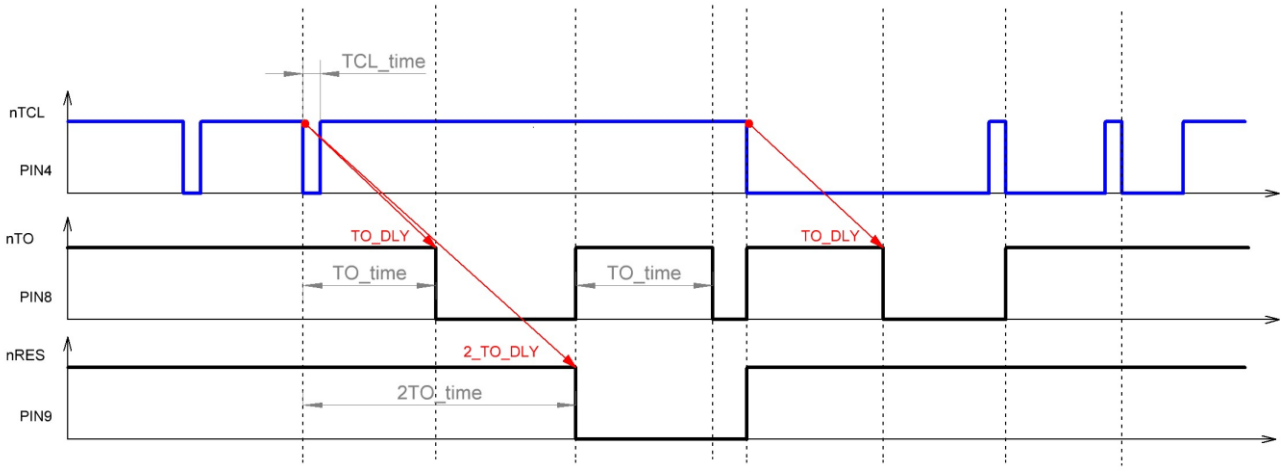

Figure 4. WatchDog function

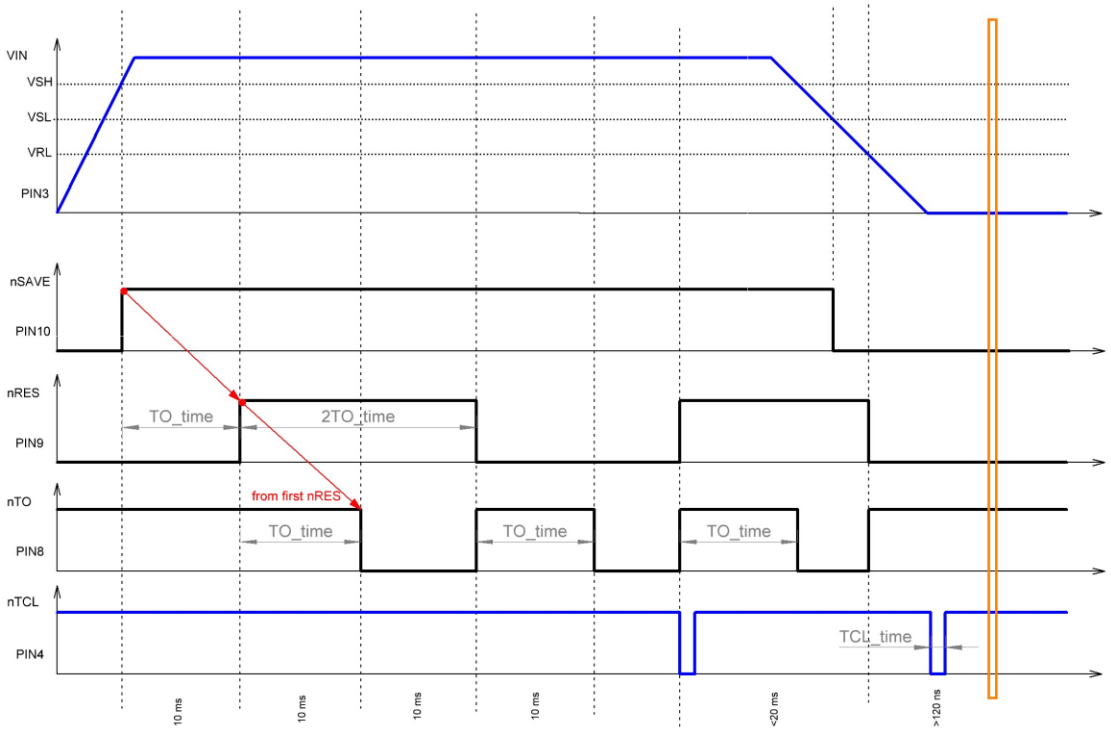

Figure 5. Combined diagram for VIN Monitoring and WatchDog timer

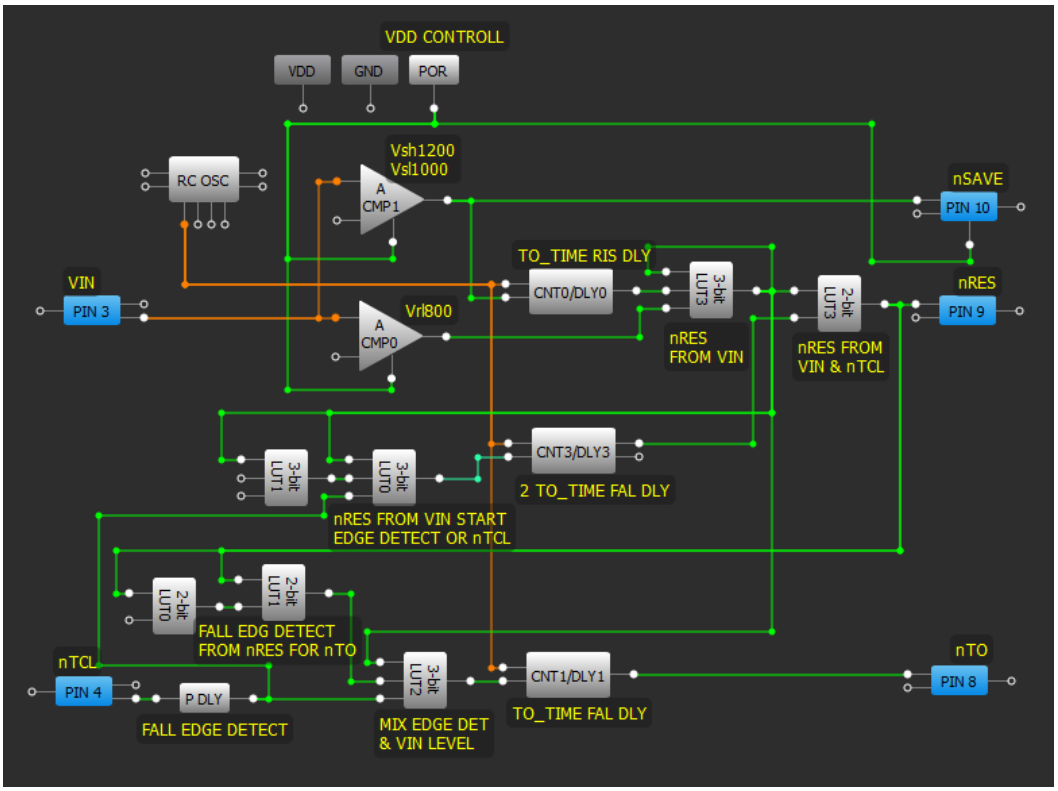

Figure 6. This project design

ACMP0 and ACMP1 are the main elements for the realization of the VIN Monitoring function.

With the features available in the SLG46110V IC such as comparators with hysteresis, it was possible to implement the scheme using only two comparators (there are actually four of them available in the IC). ACMP0 gives us the VRL threshold of 800mV level and ACMP1 provides two thresholds 1000mV (VSL) and 1200mV (VSH). Practically, the comparator ACMP1 immediately implements the nSAVE output function and is the simplest part of this design. The fact that many components have common reverse connections and commonly influence each other will ease the understanding of the rest of the scheme. Let's continue to examine from nRES output. Both comparators, CNT/DLY0 delay and three-bit LUT3 are used to implement VIN monitoring for the nRES output. After the system starts, the output of 3-bit LUT3 is LOW and feeds its IN2 input. Owing to that the feedback is created. If IN2 is LOW then the HIGH level will be set on the output of the 3-bit LUT3 cell only when the VIN signal level crosses VSH, the HIGH level will appear on the output of the ACMP1 comparator and the delay that delays the rising edge will pass it to the input IN1 of the 3-bit LUT3 after TO_time. Simultaneously, on the IN2 input of 3-bit LUT3 the HIGH level is set owing to the feedback. It will block the IN2 input and allow setting the LOW level on the output only if IN0 is LOW which is possible only when the VIN voltage is lower than VRL. Such behavior completely satisfies the diagram shown in Fig.3. But as shown in Fig.5 the nTCL input also influences nRES. Therefore the 2-bit LUT3 is used to combine two functions. This is how it works: When the HIGH level from 3-bit LUT3 reaches IN1 input of 2-bit LUT3 it allows the signal to change the output of 2-bit LUT3 based on the IN0 input.

DLY3 cell functions as the falling edge delay and sets the output of 2-bit LUT3 HIGH for the time of 2x TO_time if pulse from either nTCL falling edge detector (PDLY) or from nRES rising edge detector generated by 3-bit LUT1 and 3-bit LUT0 arrives at its input.

Besides the functioning as an edge detector, 3LUT0 also fulfills the function of OR gate for nTCL edge detector. In such case we receive nRES signal on the output that satisfies the diagram shown in Fig.5.

Now let's examine the part of the scheme that is responsible for the Watchdog function. We will start from its nTO output. The CNT/DLY1 triggers by a falling edge and sets HIGH the nTO output for the time of TO_time after the pulse from the 3-bit LUT2 appears on its input. 3-bit LUT2 operates as an OR gate. When IN2 input is LOW (which means that VIN voltage has not reached VHS or fell lower than VRL on the input), the 3-bit LUT2 will be HIGH and all other inputs will be ignored. When IN2 input is set HIGH, the change of output state as a result of changes on two other inputs will be allowed. In this case we will get a signal on the nTO output that completely coincides with the diagram shown in Fig.5.

Diagrams that were received during verification and testing of the SLG46110V, are presented in the Appendix 1 along with comments. They completely correspond to the previously mentioned diagrams of H6006 IC operation.

The project configuration may be found in Appendix 2.

How to lose some "additional kilowatts"

Despite the humorous title, the issue of power savings is very important. Analog comparator blocks tend to consume more power than any other block in this design. The orange rectangle in Fig.5 shows a region of quiescent current.

The current was 75uA at VDD voltage 5V. H6006 datasheet indicates that 50uA is typically consumed. Therefore research was conducted to find the solutions to decrease the current. In this process the option of periodic powerdown of comparators was not adopted since a sudden voltage drop might be missed and then cause an error in the operation of microprocessor system.

A more elegant solution is as follows: Since comparators are main energy consumers it is necessary to find a solution how and when to switch them on and off. The scheme with a new, low power design is represented in Fig.7 (external components connection is shown in Appendix 5 scheme a). Two new inputs CMPL and CMPH and also new cells: 2-bit LUT2, 3-bit LUT4 and 4-bit LUT0 appear here.

CMPL and CMPH are low voltage digital inputs that practically add two additional thresholds to the VIN Monitoring shown in diagram in Fig.3. With the help of external threshold voltage dividers on these inputs set lower than VRL and higher than VHS, the range of comparator operation stays inside the CMPL-CMPH voltage range.

Let's examine how new elements in the scheme function. The output of 2-bit LUT2 is set HIGH when the voltage on VIN is between CMPL and CMPH thresholds. In other cases its output is LOW. This HIGH level turns on the comparators. As the CMPH threshold is not reached yet at that moment, the LOW level on the IN0 input of 3-bit LUT4 and 4-bit LUT0 allows comparator outputs to propagate. When the voltage level crosses the CMPH threshold then a HIGH level is sent to 3-bit LUT4 and 4-bit LUT0 outputs.

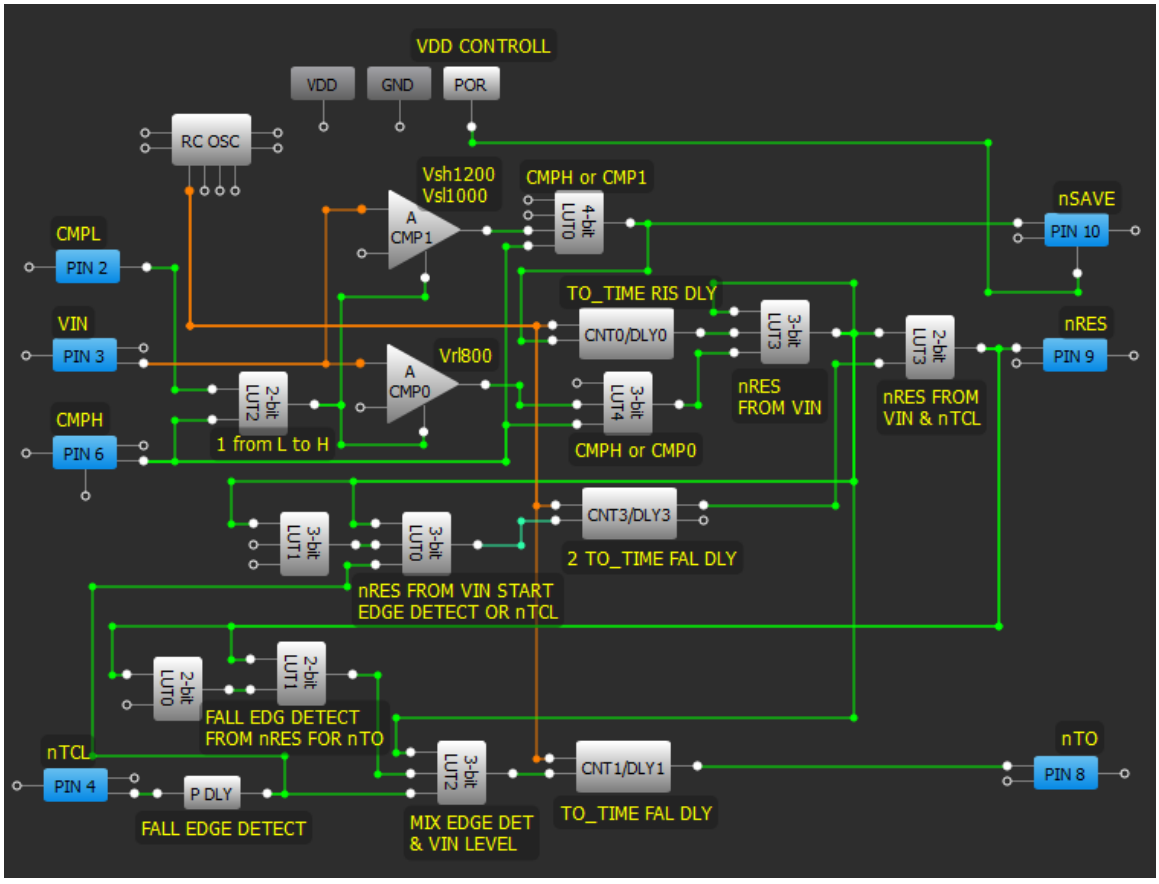

Figure 7. The low power design

When the comparators are switched off, which is most of the time, the IC consumes only 0.76uA.

When the comparators are fully powered up the current is 75uA. As the IC mostly has normal voltage on VIN, this design architecture allows significant current savings which is important for devices with battery powered or mobile devices.

Waveforms with the relevant comments for this improvement can be found in Appendix 3 and project configuration in the Appendix 4. Typical application Circuit of SLG46110V Failsafe Watchdog IC can be also found in Appendix 5.

Conclusion

This IC can be used as a replacement of the H6006 IC. The SLG46110V completely duplicates the functions of H6006, and it also provides Monitoring and/or as Watchdog features. Significant advantages of the SLG46110V are its much lower power consumption, the flexibility of customizing timing parameters, and availability other configurable circuit resources to include even more functions.

Appendix 1

Functionality Waveforms for Design 1:

- Channel 1 (yellow/top line) – PIN#1 (VDD)
- Channel 2 (light blue/2nd line) – PIN#3 (VIN)
- D0 – PIN#10 (nSAVE)
- D1 – PIN#9 (nRES)
- D2 – PIN#8 (nTO)
- D3 – PIN#4 (nTCL)

1.1. Behavior: VDD Monitoring

V1 is a value of POR ON threshold level and V2 is POR OFF threshold level. In this range VIN Monitoring and Watchdog are enabled (if VDD exceeds V1 on rising edge but does not exceed V2 on falling edge).

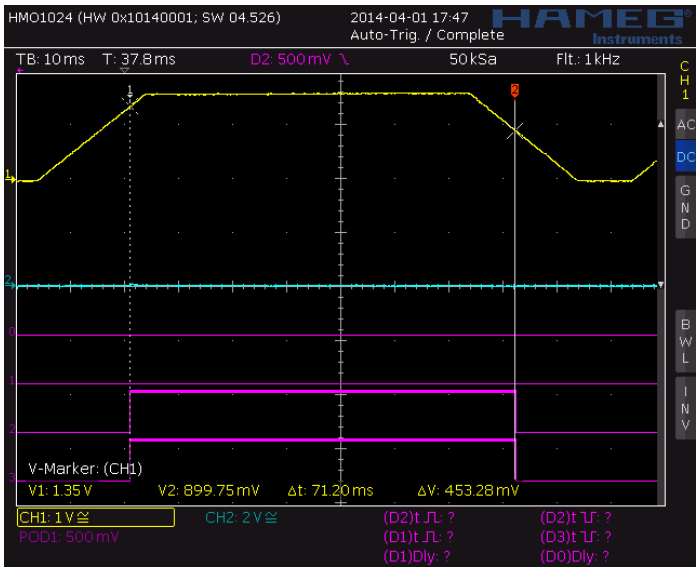

Figure 1.1. Voltage Reaction: VDD Monitoring

1.2. Combined Voltage and Timer Behavior: nSAVE function

Vsh=V1 (Vsh is an upper threshold of Vin voltage which is monitored for nSAVE function). Vsl=V2 (Vsl is a lower threshold of Vin voltage for nSAVE function). In the range from Vsh to Vsl nSAVE output is HIGH.

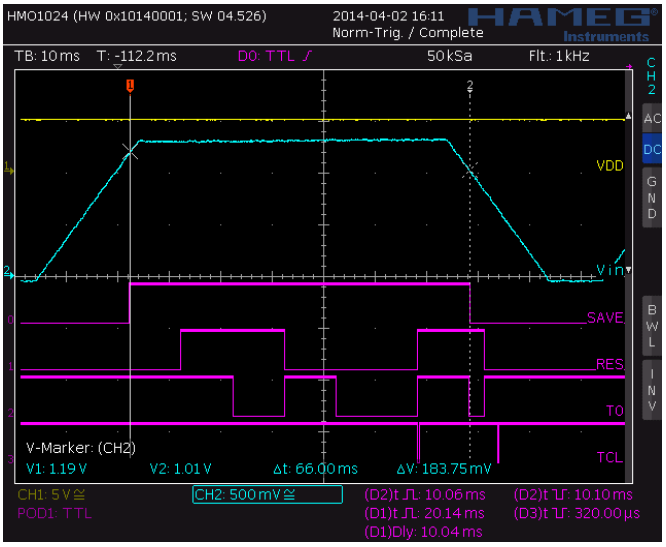

Figure 1.2. Combined Voltage and Timer behavior: nSAVE function

1.3. Combined Voltage and Timer Behavior: nRES function

nRES becomes active (HIGH) after TO_time (10mS) after nSAVE output also becomes active (HIGH). If there is no LOW pulse on nTCL input, nRES will go LOW (become inactive) after two TO_time times. Otherwise nRES will remain active.

Vrl=V2 (Vrl is a lower threshold of Vin voltage used for nRES function). nTO output will go LOW after TO_time when nRES becomes active (HIGH) and there no falling edge on nTCL input. nTO will go back HIGH for TO_time if nRES becomes inactive (LOW). Also nTO output is HIGH if Vin has not crossed above Vsh threshold and after Vin goes below Vrl threshold.

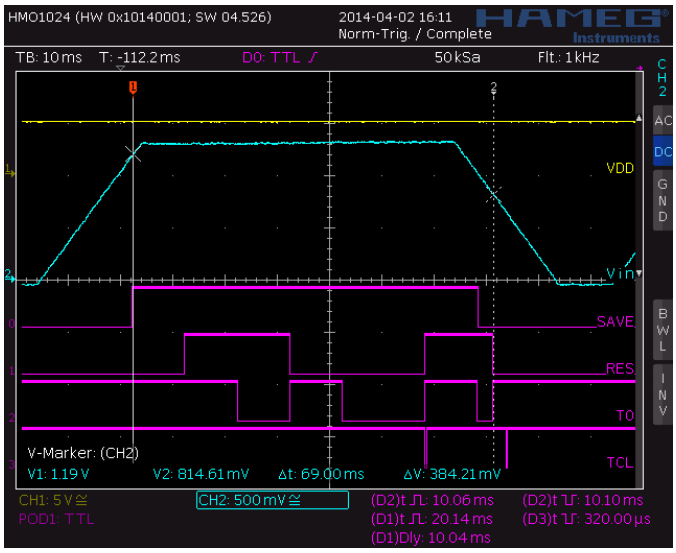

Figure 1.3. Combined Voltage and Timer Behavior: nRES function

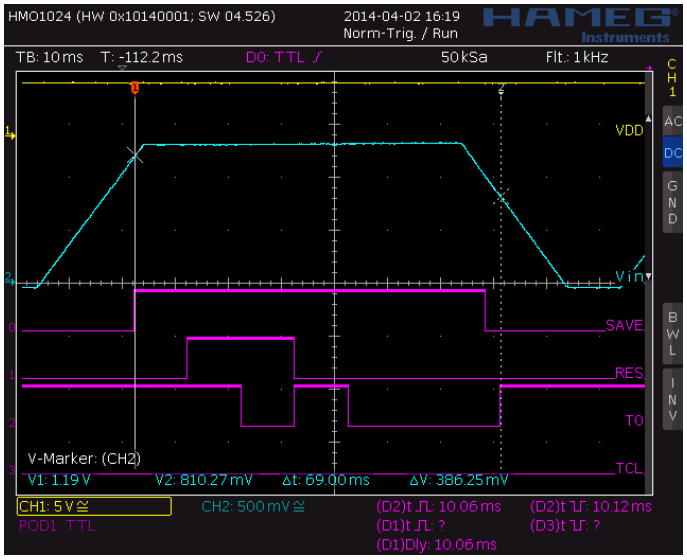

Figure 1.4. Combined Voltage and Timer Behavior: nTCL is stopped

1.5. Only Voltage Behavior: WatchDog not used

WatchDog is looped. nTO output is connected to the nTCL input. Below are zoomed WatchDog operating pulses. Apparently, they don't influence the VIN Monitoring operation.

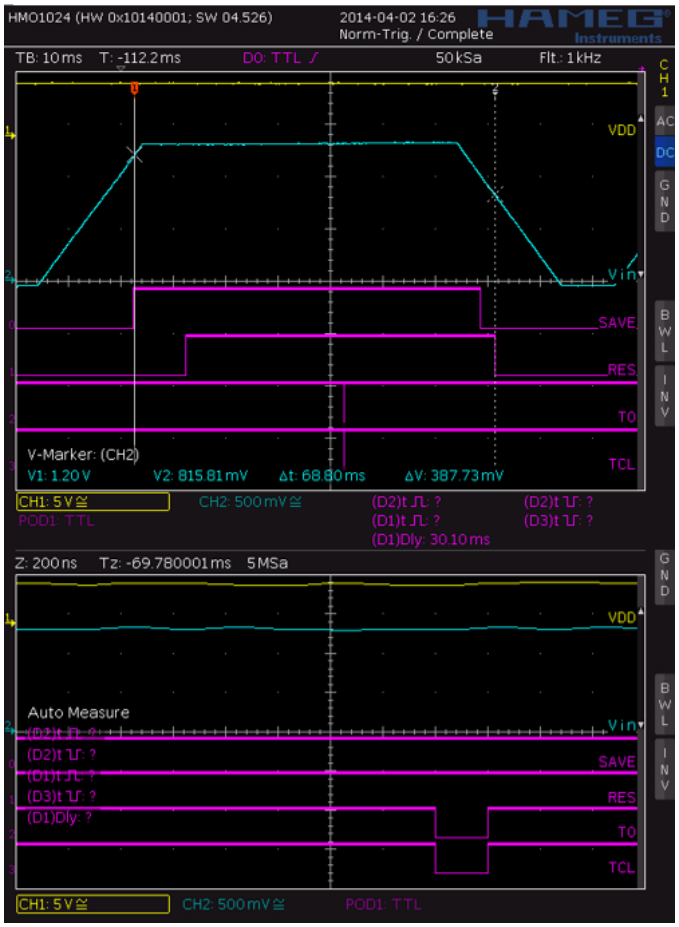

Figure 1.5. Only Voltage Behavior: WatchDog not used

1.6. Timer Only Behavior: VIN Monitoring not used

WatchDog doesn't operate if VIN Voltage is LOW. For it could operate without VIN monitoring function, VIN input should be connected to VDD.

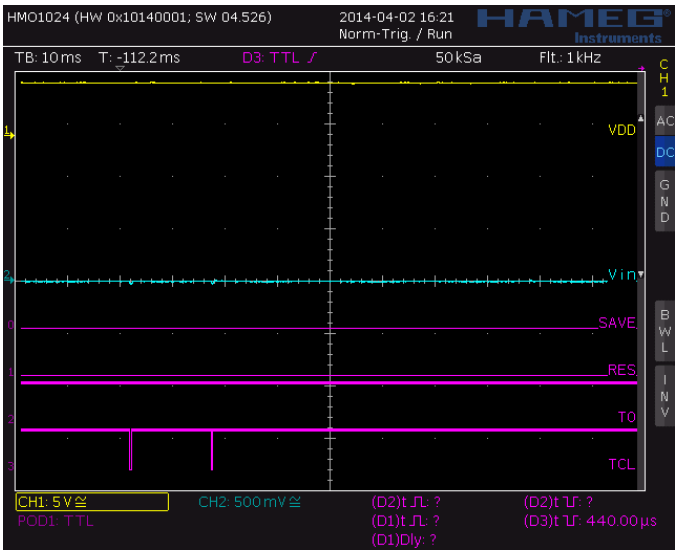

Figure 1.6. Timer Only Behavior: VIN Monitoring not used

Appendix 2

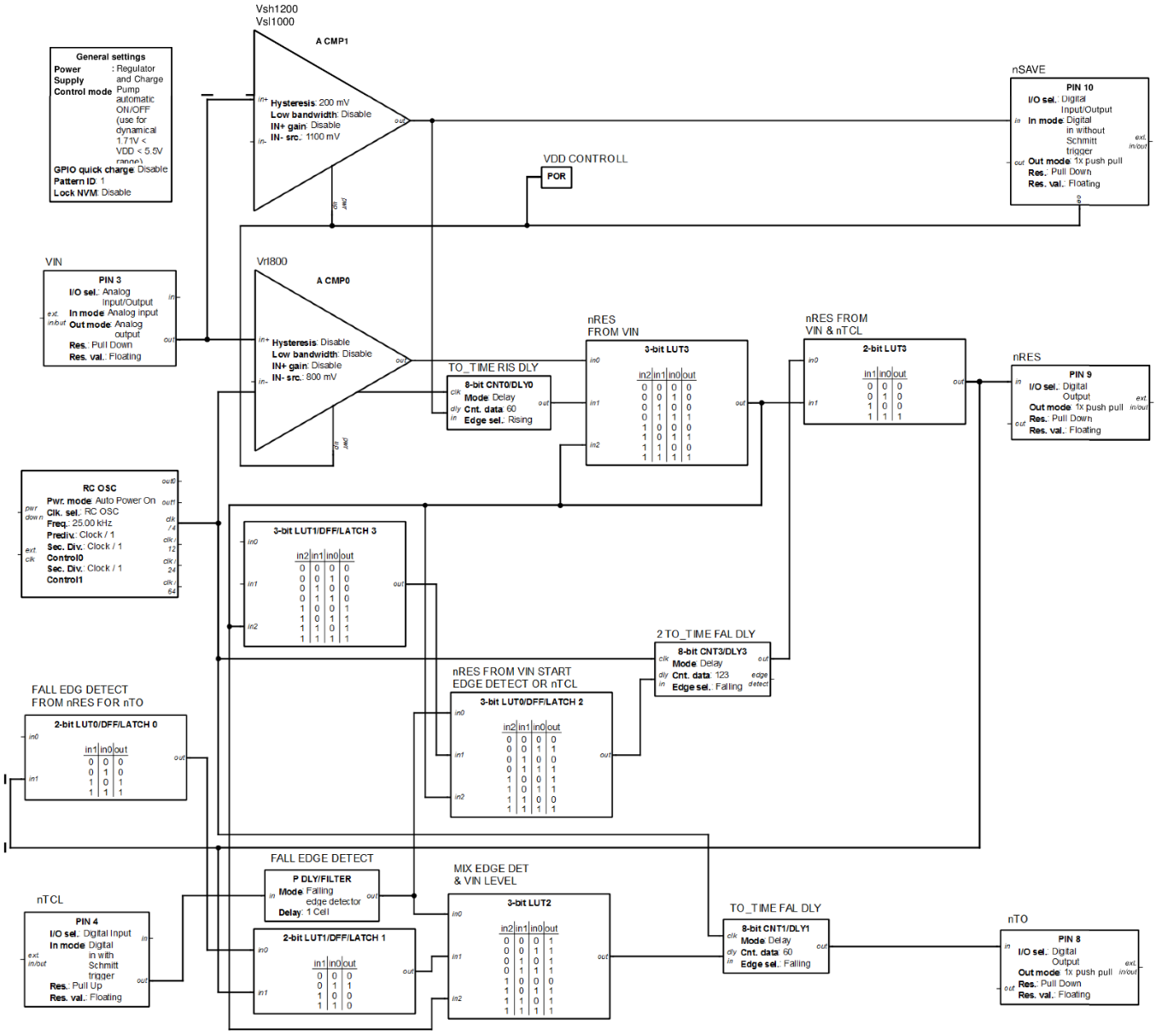

Figure 2.1. Internal Configuration of the IC for Design 1

Appendix 3

Additional functionality Waveforms for Design 2.

- Channel 1 (yellow/top line) – PIN#1 (VDD)
- Channel 2 (light blue/2nd line) – PIN#3 (VIN)
- D0 – PIN#10 (nSAVE)
- D1 – PIN#9 (nRES)
- D2 – PIN#8 (nTO)
- D3 – PIN#4 (nTCL)
- D4 – PIN#6 (CMPH)
- D5 – PIN#2 (CMPL)

3.1. Combined Voltage and Timer Behavior: CMPH and CMPL Functions

If CMPH and CMPL inputs are LOW (if voltage on Vin input is lower than the CMPL threshold and lower than thresholds of comparators) then the IC doesn't react to changes on the remaining inputs.

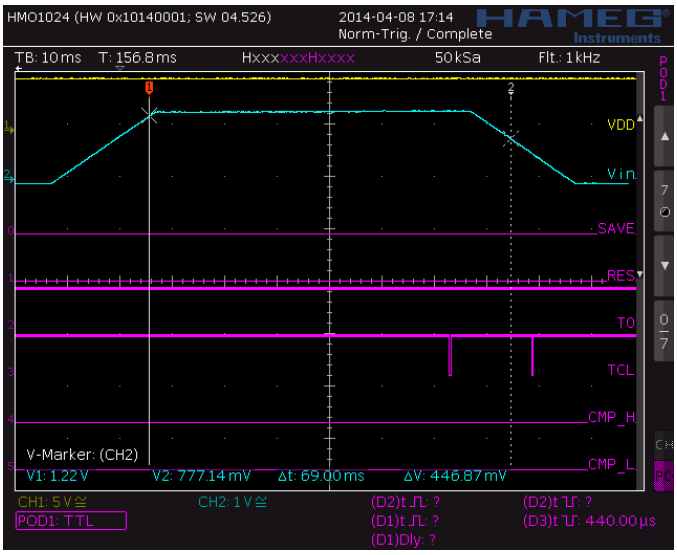

Figure 3.1. Combined Voltage and Timer Behavior: CMPH and CMPL Functions

3.2. Combined Voltage and Timer Reaction: CMPH and CMPL Functions

If CMPH is LOW and CMPL input is HIGH (if voltage on Vin input is higher than the CMPL threshold but lower than the CMPH threshold) then comparators are turned on and react to voltage variations on VIN input.

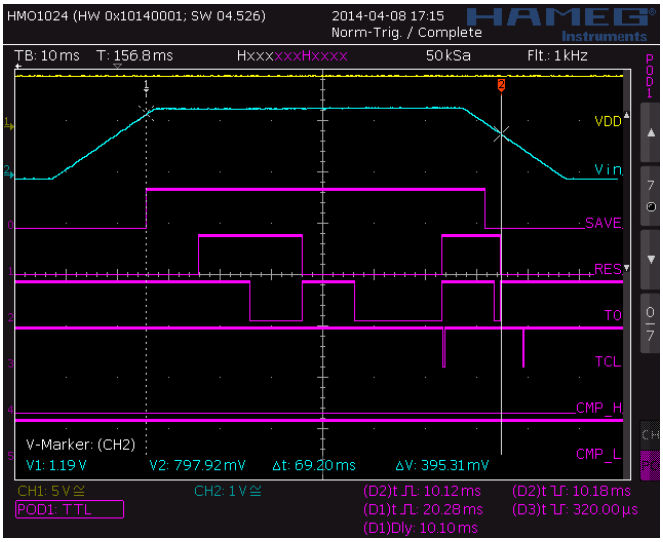

Figure 3.2. Combined Voltage and Timer Behavior: CMPH and CMPL Functions

3.3. Combined Voltage and Timer Reaction: CMPH and CMPL Functions

If CMPH and CMPL inputs are HIGH (if voltage on Vin input is higher than the CMPH threshold and higher than thresholds of comparators) then comparators are switched off and chip reacts only to WatchDog input.

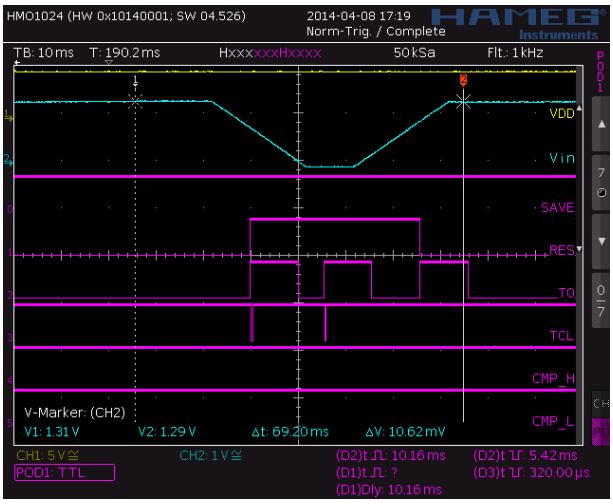

Figure 3.3. Combined Voltage and Timer Behavior: CMPH and CMPL Functions

Appendix 4

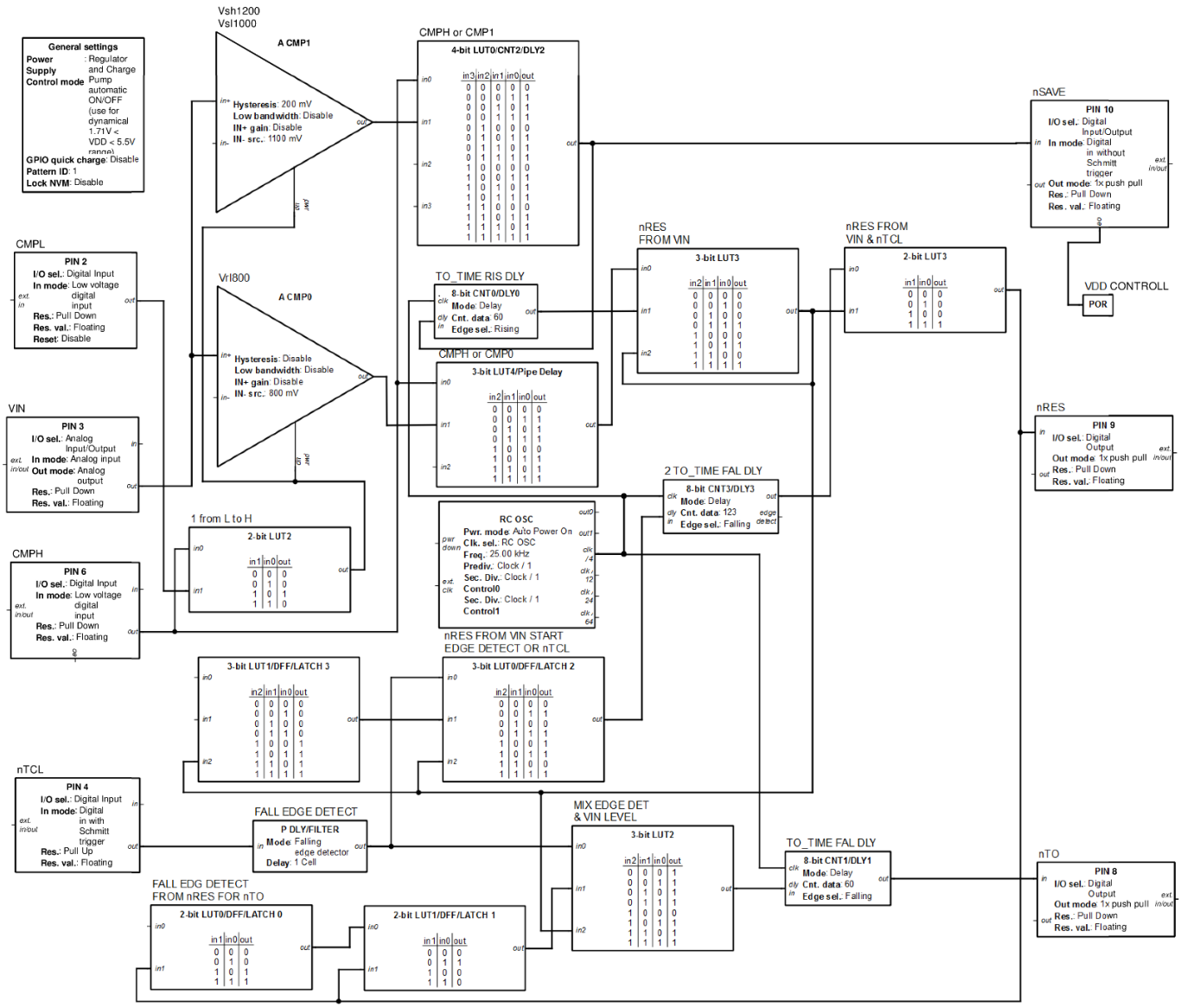

Figure 4.1. Internal configuration of the IC for Design 2

Appendix 5

Typical Application Circuit.

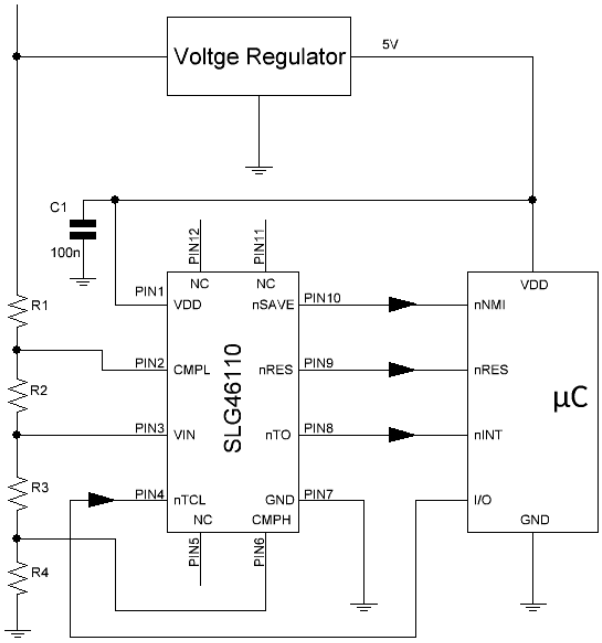

Figure 5.1. All functions are used

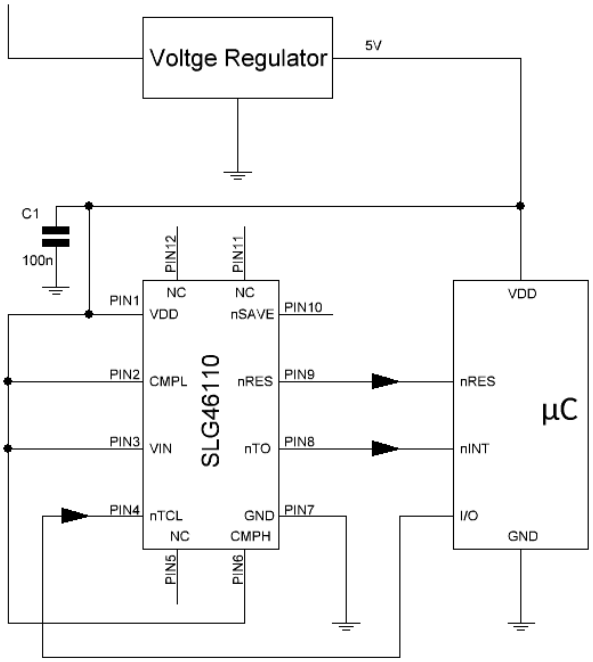

Figure 5.2. WatchDog is used, VIN Monitoring is disabled

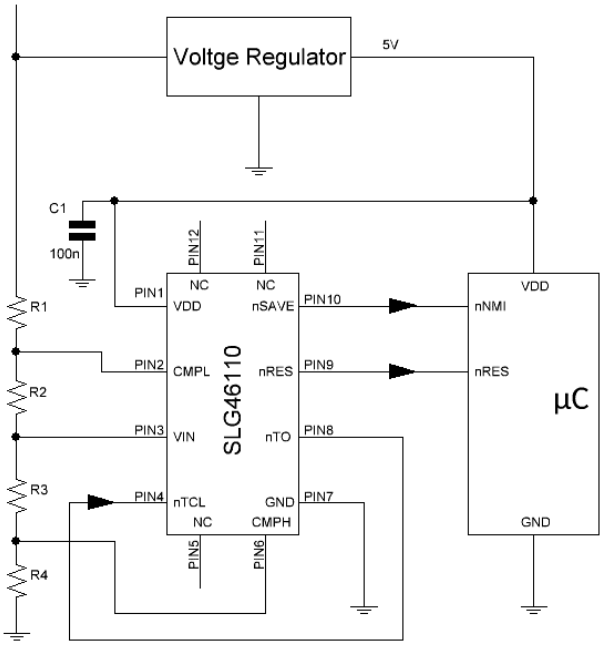

Figure 5.3. VIN Monitoring is used, WatchDog is disabled

R1-R4 resistors should be selected such to provide the appropriate actuation voltages of comparators and enough voltage distance between thresholds of comparators and CMPH/CMPL thresholds.

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