

White Paper

Putting Safety into Li-ion Battery Packs

November 2020

Abstract

The power FET is an essential safety function in a battery management system (BMS). The main purpose of the power FET is to isolate the battery pack from either a load or a charger in errant conditions. This white paper discusses the detection blocks and how they apply to the state of the power FETs to ensure safe operation of lithium ion (Li-ion) battery packs.

The power FET functional block seems straightforward: turn on the FET when a charger or load is connected; turn off the FET if anything goes wrong. Proper functionality of the power FETs requires the designer to understand the load conditions, the battery pack limitations and to have an understanding of the functional block circuitry.

In a BMS, the power FETs are controlled by cell voltage, pack current, temperature, load and charge monitor comparisons. The functional block is constructed in one of three ways within the system: (1) through discrete components, which requires additional board space and the designer has to have an in-depth knowledge of each sub block. (2) A power FET IC that integrates most of the sub functional blocks and is useful as a companion IC to a multi-cell monitor/balancer. A power FET IC is useful in high cell count applications (> 16 cells) such as solar farms and smart grids. (3) The power FET functional block is found in a fully integrated BMS IC such as the ISL94202, ISL94203 and the ISL94208. Each approach has roughly the same functionality and this white paper explains the inner functionally of each sub block and design considerations for different applications.



Figure 1: A simplified diagram of the circuitry required in deciding whether to turn on or off the power FETs

Consider the circuit configuration in Figure 1. The system is a high side series FET configuration that is connected to a motor. The power FET's ON state is dependent on the cell voltages of a battery pack, the charge and discharge current, the temperature and the state of the monitor pin. Any faults reported by the sub blocks results in one or both FETs turning OFF.

Vcell Detection

 V_{cell} detection without cell balancing considerations is a voltage measurement that is monitored for over voltage, under voltage and open cell conditions. The under voltage condition is important in detecting pack empty situations to protect the cells from dropping out of the active region. A lithium ion cell has a voltage active region between 2.5V and 4.2V. The active region for a lithium polymer cell is 2.5V to 3.6V. The bounded voltage of the cell sets the full and empty cell limit based on chemistry and design. Charging the cell beyond the upper voltage limit is restricted and may cause damage to the cell. Most BMS ICs continually monitor for over voltage and under voltage conditions independent of battery charge state.

After all the cells in the pack have been measured, it is useful to report the overall voltage difference between the strongest cell and the weakest cells. A large differential pack voltage screens for an open cell or open wire event. Most systems have an open wire test that determines with certainty that the wire between the measurement system and the cell is connected. Open wire tests are not as frequent as cell voltage reads, and the cell differential calculation can be an early indicator of trouble with the system.

An open cell occurs when a cell opens internally or an external connection is broken. The event can be slow or abrupt. Possible causes of an open cell are from aging, a poorly manufactured cell or prolonged operation in harsh environments. A broken external connection is usually the result of a poorly constructed battery pack.

False positives for the maximum differential cell voltage can occur when a substantial in-rush current is sourced by the battery pack when connecting to a load. The in-rush current multiplied by the mismatch in cell impedance results in a substantial mismatch in cell voltage. Some chips have a delay before reporting the event while others do not.

Current Detection

Most battery systems that measure current have three current comparators; discharge short circuit (DSC), discharge over current (DOC) and charge over current (COC). Each comparator feeds into a delay allowing the current to be greater than the limit for a period of time before action is taken.

Loads are less controlled than chargers and fast action current discharge detection is needed to shut off the power FETs before damaging the battery or the power FETs themselves. Tens to hundreds of microsecond delay is common for a DSC event to turn off the power FETs. The DSC delay consists of a timed delay, and the time it takes for the power FET to turn OFF. An off power FET is when the gate and source are connected together through an isolation resistor(s). The resistor and gate capacitance creates an RC circuit that sets the turn OFF time of the FET.

There are many considerations when setting the overall DSC off time delay. The DSC off time is bounded by the time to damage the battery and the circuitry versus allowing the in-rush current to pass when a load starts up or is connected. The DSC off time has to be balanced with the off time of the FET. Turning off the FET too quickly results in large voltage transients at the cell measurement pins. The pins closest to the power FETs are most susceptible to large voltage transients. The transients are a result of inductive energy stored in the trace between the power FET and the battery not having anywhere to dissipate its energy when the battery pack is abruptly disconnected from the load. The inductive energy dissipates into an open load until the voltage rises enough to activate the ESD diodes of the connected circuitry. If there is enough energy, the part can be electrically overstressed. The amount of energy stored in the trace is a product of the inductance of the trace and the current sourcing to the load. The trace has the most energy in discharge short circuit conditions. Filtering at the cell

voltage pins helps reduce the likelihood of an EOS event. Always keep traces as short as needed and maximize the width of the trace. Care should be taken on the size and length of the cable between load and power FET. This is another area high voltage transients can occur.

Increasing the isolation resistor value between the gate of the FET and the FET control pin reduces the magnitude of the voltage transient by increasing the turn off time of the FET. This also results in an increase in power FET turn on time via the RC time constant with the FET capacitance. Note that the isolation resistor is common to both events.

Turning off the power FET too slowly results in power FET damage or a brown out condition. Most power FET datasheets have a typical curve that plots FET current versus V_{DS} and time duration, as shown in Figure 2. Consider a 20V battery pack having a short circuit current of 100A. The graph below shows that the FET can survive 1ms in this condition.



Figure 2: The turn off time of the FET should be within the safe operating area of the power FET

It is common that the DSC limit is balanced with the duration of the in-rush current. The in-rush current can be as large as 100 or more times the operating current. Figure 3 is an example of an in-rush transient. The in-rush current peak is 270A. The operational current draw is 8A. If the in-rush current is allowed to trip the DSC limit, the FETs will toggle between on and off conditions.



Figure 3: In-rush currents can inadvertently trip discharge short circuit limit

Figure 4 is the resultant pack voltage drop when the in-rush current of Figure 3 is sourced to the cells. Figure 4 shows the importance of using low impedance cells and connections between cells. The in-rush current causes the pack voltage to drop by 10.8V. The magnitude of the in-rush current is lowered by increasing the isolation resistance (R_{iso1} and R_{iso2}) of the power FET. An increase in isolation resistance increases the duration of the in-rush current event.



Figure 4: The voltage drop at pack level when the in-rush current in Figure 3 is sourced by the pack

The discharge over current limit and delay is a secondary limit that screens for a damaged load or system (walking wounded) or a wrong load connected to the battery pack. The presence of the DOC condition can be considerably longer and has fewer considerations than the DSC.

The charge over current limit prevents over charging of the battery and wrong chargers from charging the battery pack. The COC delay allows for short duration of unregulated charge to pass to the battery. Figure 5 shows the load profile of a scooter. The motor is charging the battery when the current is negative. The regenerative current from the motor can be substantially larger than the charging current. The COC limit is set close to the charger's current to prevent the battery from being charged by the wrong charger. Most regenerative currents are short in duration. In Figure 5, the regenerative current recorded after 250s is the scooter rolling down a hill. The

regenerative current around 280s is the scooter coasting to a stop. The charging current for this battery pack is 2A.



Figure 5: The load profile of a scooter

There are many factors that go into setting the charge current. The major factor is the charge acceptance of the cells themselves. Other factors are charge time, cell heating and battery aging in setting the charge current.

Temperature Detection

The primary reason to detect cell temperature is to ensure that the battery does not reach a thermal runaway condition. Conditions that can cause thermal runaway are a cell overcharging, a short to the battery pack, or internal shorts in the cell themselves. Some chemistries are more susceptible than others to thermal runaway.

Besides thermal runaway detection, thermal detection is used to determine if a battery is safe to charge or discharge. Most lithium batteries have a recommended charge/discharge temperature range as shown in Figure 6. In applications such as laptops, it may be necessary to charge in the discharge only regions of Figure 6. JEITA is a standard for charging lithium cells. The standard calls for a reduction of charging current in temperature regions where the cell is less stable or less able to accept charge. Figure 7 is an example of a JEITA charging standard. For most applications, the profile in Figure 6 is sufficient and simple to implement.



Figure 6: The acceptable charge/discharge temperature regions for Lithium batteries



Figure 7: Charging is possible in extreme temperature regions but it becomes more complicated

Conclusion

For standalone BMS ICs, it is important to understand their functional blocks and what the power FETs do in the operational region. Some ICs allow for charging by keeping on both charge FETs (CFETS) and discharge FETs (DFETs). Other ICs turn off CFET. A CFET should never be off in a series power FET configuration when operating in the discharge only region of the cell temperature profile. Operating a load while CFET is off allows current to pass through the body diode of the CFET. This increases the power dissipated by the FET, resulting in an increase in FET temperature. If action is not taken to remove the heat from the FET, either through layout or by using a heat sink, the component could be damaged. A CFET that is off while operating in a series configuration also reduces the power to load affecting application performance.

In most small to mid-sized packs, two thermistors are used to monitor temperature. One of the thermistors is placed in the center of the pack where the temperature is higher due to the insulation from the cells. Because of the higher operating temperatures, these cells age faster. The placement of the second thermistor is on the outside of the pack, which is a good measurement of ambient temperature. Proper temperature detection protects the battery against thermal runaway and ensures it is safe to charge or discharge.

Next Steps

- Product Information
 - ISL94202 standalone battery pack monitor
 - ISL94216 battery front end
 - ISL94208 battery management analog front end
- Watch how a battery pack monitor protects Li-ion batteries
- Order free IC samples

© 2020 Renesas Electronics Corporation or its affiliated companies (Renesas). All rights reserved. All trademarks and trade names are those of their respective owners. Renesas believes the information herein was accurate when given but assumes no risk as to its quality or use. All information is provided as-is without warranties of any kind, whether express, implied, statutory, or arising from course of dealing, usage, or trade practice, including without limitation as to merchantability, fitness for a particular purpose, or non-infringement. Renesas shall not be liable for any direct, indirect, special, consequential, incidental, or other damages whatsoever, arising from use of or reliance on the information herein, even if advised of the possibility of such damages. Renesas reserves the right, without notice, to discontinue products or make changes to the design or specifications of its products or other information herein. All contents are protected by U.S. and international copyright laws. Except as specifically permitted herein, no portion of this material may be reproduced in any form, or by any means, without prior written permission from Renesas. Visitors or users are not permitted to modify, distribute, publish, transmit or create derivative works of any of this material for any public or commercial purposes.