[Notes] RX Family Board Support Package Module Using Firmware Integration Technology Rev.6.20

R20TS0715EJ0100
Rev.1.00
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Outline

When using the product in the title, note the following point.

1. Selecting the PLL circuit as the CLKOUT pin's output clock source in the RX140 CLKOUT output function.

1. Selecting the PLL circuit as the CLKOUT pin's output clock source in the RX140 CLKOUT output function

1.1 Applicable Products

(1) Board Support Package Module Using Firmware Integration Technology (BSP FIT Module)

The applicable revision and document are as follows.

Table 1.1 BSP FIT Module applicable product

Revision	Document number
Rev.6.20	R01AN1685EJ0620

1.2 Applicable Devices

- RX140 group

1.3 Details

The oscillation of the PLL circuit is not executed properly under certain conditions.

If an option other than the PLL circuit is selected as the clock source (BSP_CFG_CLOCK_SOURCE) and the PLL circuit as the CLKOUT pin's output clock source (BSP_CFG_CLKOUT_SOURCE), the oscillation of the PLL circuit is disabled. Therefore, the CLKOUT pin does not output the PLL clock.

1.4 Conditions

The problem arises if the following conditions are met.

(1) RX140 is selected for the device.

(2) In Smart Configurator, an option other than the PLL circuit is selected as the clock source (BSP_CFG_CLOCK_SOURCE ≠ 4), and the PLL circuit as the CLKOUT clock source (BSP_CFG_CLKOUT_SOURCE = 4). Check the checkbox of the CLKOUT pin output and start generating codes.

1.5 Workaround

Refer to the following and modify mcu¥rx140¥mcu_clocks.c as shown in red.

clock_source_select() (L546 to L564)

Before modification

```
#if BSP_CFG_CLOCK_SOURCE == 4
    /* PLL is chosen. Start it operating if it is not already. Must start main clock as well since PLL
uses it. */


    /* Set PLL Input Divisor. */
    SYSTEM.PLLCR.BIT.PLIDIV = BSP_CFG_PLL_DIV >> 1;


    /* Set PLL Multiplier. */
    SYSTEM.PLLCR.BIT.STC = (BSP_CFG_PLL_MUL * 2) - 1;


    /* Set the PLL to operating. */
    SYSTEM.PLLCR2.BYTE = 0x00;


    /* WAIT_LOOP */
    while (0 == SYSTEM.OSCOVFSR.BIT.PLOVF)
    {
        /* Make sure clock has stabilized. */
        R_BSP_NOP();
    }
#endif
```

After modification

```
#if BSP_PRV_PLL_CLK_OPERATING == 1
    /* PLL is chosen. Start it operating if it is not already. Must start main clock as well since PLL uses it. */


    /* Set PLL Input Divisor. */
    SYSTEM.PLLCR.BIT.PLIDIV = BSP_CFG_PLL_DIV >> 1;


    /* Set PLL Multiplier. */
    SYSTEM.PLLCR.BIT.STC = (BSP_CFG_PLL_MUL * 2) - 1;


    /* Set the PLL to operating. */
    SYSTEM.PLLCR2.BYTE = 0x00;


    /* WAIT_LOOP */
    while (0 == SYSTEM.OSCOVFSR.BIT.PLOVF)
    {
        /* Make sure clock has stabilized. */
        R_BSP_NOP();
    }
#endif
```

1.6 Schedule for Fixing the Problem

The problem is fixed in BSP Rev.6.21 (document number: R01AN1685EJ0621).

Update your product to BSP Rev.6.21.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct.01.21	-	First edition issued

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